



0.5dB LSB GaAs MMIC 6-BIT DIGITAL SERIAL CONTROL ATTENUATOR MODULE, DC - 13 GHz



Typical Applications

The HMC-C018 is ideal for:

- Telecom Infrastructure
- Military Radio, Radar & ECM
- Space Systems
- Test Instrumentation

Functional Diagram



Features

0.5 dB LSB Steps to 31.5 dB CMOS Compatible Serial Data Interface Typical Bit Error: ±0.3 dB Hermetically Sealed Module Field Replaceable SMA Connectors -55 °C to +85 °C Operating Temperature

General Description

The HMC-C018 is a DC to 13 GHz 6-bit GaAs IC Digital Serial Control Attenuator housed in a miniature hermetic module. This wideband attenuator features 3.6 dB typical insertion loss, +38 dBm input IP3, and bit values of 0.5 (LSB), 1, 2, 4, 8, and 16 dB for a total attenuation of 31.5 dB. Attenuation accuracy is excellent with \pm 0.3 dB typical step error. A six bit CMOS compatible serial control word is used to select each attenuation state and a single Vdc bias of -5V allows operation at frequencies down to DC. Removable SMA connectors can be detached to allow direct connection of the module's I/O pins to a microstrip or coplanar circuit.

Electrical Specifications, $T_{A} = +25 \text{ °C}$, with Vdc = -5V and 0/+5V CMOS Control

Parameter		Frequency (GHz)	Min.	Тур.	Max.	Units
Insertion Loss		DC - 4.0 GHz 4.0 - 8.0 GHz 8.0 - 13 .0 GHz		3.2 3.6 5.0	3.7 4.1 6.0	dB dB dB
Attenuation Range		DC - 13.0 GHz		31.5		dB
Return Loss (RF1 & RF2, All Atten. States)		DC - 8.0 GHz 8.0 - 13.0 GHz		15 10		dB dB
Attenuation Accuracy: (Referenced to Insertion Loss) All States 0.5 - 27.5 dB 28.0 - 31.5 dB All States		DC - 3.0 GHz 3.0 - 10.0 GHz 3.0 - 10.0 GHz 10.0 - 13.0 GHz	± (0.2 + 3% of Atten. Setting) Max ± (0.4 + 3% of Atten. Setting) Max ± (0.5 + 6% of Atten. Setting) Max ± (0.6 + 6% of Atten. Setting) Max		dB dB dB dB	
Input Power for 0.1 dB Compression		1.0 - 13.0 GHz		22		dBm
Input Third Order Intercept Point (Two-Tone Input Power= 0 dBm Each Tone)	REF State All Other States	1.0 - 13.0 GHz		46 32		dBm dBm
Switching Characteristics		DC - 13.0 GHz				
tRISE, tFALL (10/90% RF) tON/tOFF (50% CTL to 10/90% RF)				600 700		ns ns

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Insertion Loss



Normalized Attenuation

(Only Major States are Shown)







Return Loss RF1, RF2

(Only Major States are Shown)



Bit Error vs. Attenuation State



Relative Phase vs. Frequency

(Only Major States are Shown)



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Worst Case Step Error Between Successive Attenuation States

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Bias Voltage & Current

VDC Range= -5.0 Vdc ± 10%				
VDC Idc (Typ.) Idc (Max.) (mA) (mA)				
-5.0	5	9		

Serial Input Truth Table

Latch Enable	Shift Clock	Reset	Function
Х	Х	L	Shift register cleared
Х	\uparrow	Н	Shift register clocked
Ŷ	х	н	Contents of shift register transferred to Digital Attenuator

Absolute Maximum Ratings

Digital Inputs (Reset, Shift Clock, Latch Enable & Serial Input)	-0.5V to +5.5V
Bias Voltage (VDC)	-7.0 Vdc
Storage Temperature	-65 to + 150 °C
Operating Temperature	-55 to +85 °C
RF Input Power (0.5 - 13.0 GHz)	+25 dBm



ELECTROSTATIC SENSITIVE DEVICE OBSERVE HANDLING PRECAUTIONS

CMOS Control Voltages

State	Bias Condition
Low	0 to +1.3V
High	+3.5 to +5.0V

Truth Table

Serial Control Input						Attenuation	
C0.5	C1	C2	C4	C8	C16	Settings RF1 - RF2	
Н	Н	Н	Н	Н	Н	Reference I.L.	
L	н	Н	н	н	н	0.5 dB	
Н	L	Н	Н	Н	Н	1 dB	
Н	Н	L	Н	Н	Н	2 dB	
Н	Н	Н	L	Н	Н	4 dB	
Н	Н	Н	Н	L	Н	8 dB	
Н	Н	Н	Н	Н	L	16 dB	
L	L	L	L	L	L	31.5 dB	
1 1	Any combination of the above states will provide an attenuation approximately equal to the sum of the bits selected.						

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Timing

Parameter	Symbol	Min.	Max.	Units
Serial Input Setup Time	ts	20	-	ns
Hold time from Serial Input to Shift Clock	th	0	-	ns
Setup time from Shift Clock to Latch Enable	tlsup	40	-	ns
Propagation delay, Latch Enable to C0.5 through C8	tpd	-	30	ns
Setup time from Reset to Shift Clock	-	20	-	ns
Clock Frequency (1/tclk)	fclk	-	30	MHz

Timing Diagram

Serial data is shifted in on the rising edge of the Shift Clock, LSB first, and is latched on the rising edge of Latch Enable.







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Logic / Functional Diagram



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Programming Example to Select 0.5 dB Attenuation State







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ATTENUATORS

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Pin Description

Pin Number	Function	Description	Interface Schematic	
1	RF1	This pin is DC coupled and matched to 50 Ohms. Blocking capacitors are required if RF line potential is not equal to 0 Vdc.	RF10	
2	С	Shift Clock	5V Zener	
3	R	Reset	V1-V6 0	
4	S	Serial Input	4700 Ω	
5	L	Latch Enable	-4.4V(Internal)	
6	RF2	This pin is DC coupled and matched to 50 Ohms. Blocking capacitors are required if RF line potential is not equal to 0 Vdc.	RF2○	
7	Vdc	Supply voltage: -5 Vdc ±10%. (Internal diode for reverse bias protection)	Vdc 0	
8	GND	Power Supply Ground		



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Outline Drawing





VIEW SHOWN WITH CONNECTORS REMOVED

Package Information

Package Type	C-6	
Package Weight ^[1]	17.4 gms ^[2]	
Spacer Weight	3 gms ^[2]	

[1] Includes the connectors

[2] ±1 gms Tolerance

NOTES:

1. PACKAGE, LEADS, COVER MATERIAL: KOVAR™

- 2. PLATING: ELECTROLYTIC GOLD 50 MICROINCHES MIN., OVER ELECTROLYTIC NICKEL 75 MICROINCHES MIN
- 3. MOUNTING SPACER: NICKEL PLATED ALUMINUM

[5.08mm]

- 4. ALL DIMENSIONS ARE IN INCHES [MILLIMETERS]
- 5. TOLERANCES ±0.010 [0.25] UNLESS OTHERWISE SPECIFIED
- 6. FIELD REPLACEABLE SMA CONNECTORS TENSOLITE 5602 - 5CCSF OR EQUIVALENT
- 7. TO MOUNT MODULE TO SYSTEM PLATFORM REPLACE 0 -80 HARDWARE WITH DESIRED MOUNTING SCREWS

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