ART1K6FH; ART1K6FHS; ART1K6FHG

Power LDMOS transistor

AMPLEON

Rev. 3 — 8 July 2022

Product data sheet

1. Product profile

1.1 General description

Based on Advanced Rugged Technology (ART), this 1600 W LDMOS RF power transistor has been designed to cover a wide range of applications for ISM, broadcast and communications. The unmatched transistor has a frequency range of 1 MHz to 425 MHz.

Table 1. Application information

Test signal	f	V_{DS}	P_L	G_p	η_D
	(MHz)	(V)	(W)	(dB)	(%)
CW pulsed [1]	108	50	1400	28.7	77.3
CW pulsed [1]	108	55	1600	29.5	76.0
CW pulsed [2]	352	50	1200	20.0	68.0

[1] Production circuit: t_p = 100 μs; δ = 10 %.

[2] Application circuit: t_p = 100 μs; δ = 10 %.

1.2 Features and benefits

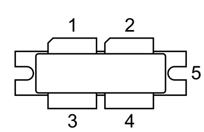
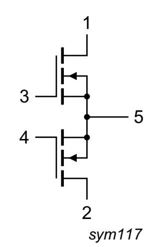
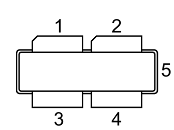
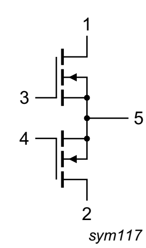
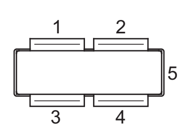
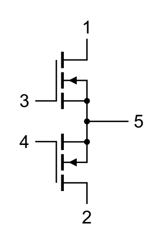
- High breakdown voltage enables class E operation at V_{DS} = 48 V
- Suitable for V_{DS} = 50 and 55 V
- Qualified up to a maximum of V_{DS} = 55 V
- Characterized from 30 V to 55 V for extended power range
- Easy power control
- Integrated dual sided ESD protection enables class C operation and complete switch off of the transistor
- Excellent ruggedness with no device degradation
- High efficiency
- Excellent thermal stability
- Designed for broadband operation
- For RoHS compliance see the product details on the Ampleon website

1.3 Applications

- Industrial, scientific and medical applications
  - Plasma generators
  - MRI systems
  - CO_2 lasers
  - Particle accelerators
- Broadcast
  - FM radio
  - VHF TV
- Communications
  - Non cellular communications
  - UHF radar

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
ART1K6FH (SOT539AN)			
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source [1]		
ART1K6FHS (SOT539BN)			
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source [1]		
ART1K6FHG (SOT1248C)			
1	drain1		
2	drain2		
3	gate1		
4	gate2		
5	source [1]		

[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Package name	Orderable part number	12NC	Packing description	Min. orderable quantity (pieces)
SOT539AN	ART1K6FHU	9349 603 27122	Tray; 20-fold; non-dry pack	60
SOT539BN	ART1K6FHSU	9349 605 33112	Tray; 20-fold; non-dry pack	60
SOT1248C	ART1K6FHGJ	9349 605 34118	TR13; 100-fold; 56 mm; non-dry pack	100

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	177	V
V_{GS}	gate-source voltage		–9	+13	V
T_{stg}	storage temperature		–65	+150	°C
T_j	junction temperature	[1]	-	225	°C

[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

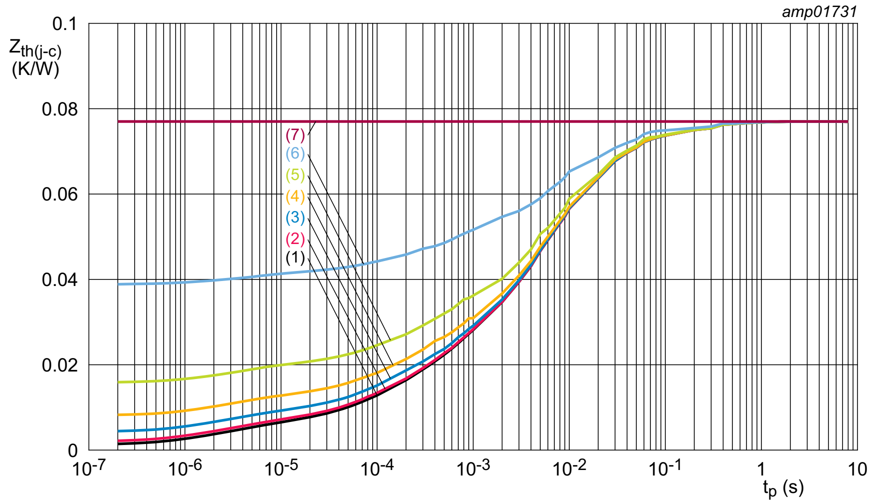
Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-c)}$	thermal resistance from junction to case	T_j = 95 °C [1][2]	0.077	K/W
$Z_{th(j-c)}$	transient thermal impedance from junction to case	T_j = 95 °C; t_p = 100 μs; δ = 10 % [3]	0.018	K/W

[1] T_j is the junction temperature.

[2] $R_{th(j-c)}$ is measured under RF conditions.

[3] See Figure 1.



(1) δ = 1 %

(2) δ = 2 %

(3) δ = 5 %

(4) δ = 10 %

(5) δ = 20 %

(6) δ = 50 %

(7) δ = 100 % (DC)

Fig 1. Transient thermal impedance from junction to case as a function of pulse duration

6. Characteristics

Table 6. DC characteristics

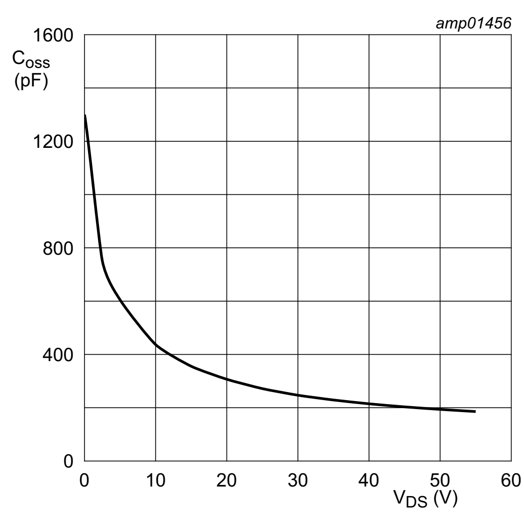
T_j = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0 V; I_D = 5.5 mA	177	191	-	V
$V_{GS(th)}$	gate-source threshold voltage	V_{DS} = 20 V; I_D = 550 mA	1.5	2.1	2.5	V
I_{DSS}	drain leakage current	V_{GS} = 0 V; V_{DS} = 50 V	-	-	2.8	μA
I_{DSX}	drain cut-off current	V_{GS} = $V_{GS(th)}$ + 3.75 V; V_{DS} = 20 V	-	81	-	A
I_{GSS}	gate leakage current	V_{GS} = 13 V; V_{DS} = 0 V	-	-	280	nA
$R_{DS(on)}$	drain-source on-state resistance	V_{GS} = $V_{GS(th)}$ + 3.75 V; I_D = 19.25 A	-	0.084	-	Ω

Table 7. AC characteristics

T_j = 25 °C; per section unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
C_{rs}	feedback capacitance	V_{GS} = 0 V; f = 1 MHz				
		V_{DS} = 50 V	-	1.71	-	pF
		V_{DS} = 55 V	-	1.65	-	pF
C_{iss}	input capacitance	V_{GS} = 0 V; f = 1 MHz				
		V_{DS} = 50 V	-	620	-	pF
		V_{DS} = 55 V	-	620	-	pF
C_{oss}	output capacitance	V_{GS} = 0 V; f = 1 MHz				
		V_{DS} = 50 V	-	193	-	pF
		V_{DS} = 55 V	-	185	-	pF



V_{GS} = 0 V; f = 1 MHz

Fig 2. Output capacitance as a function of drain-source voltage; typical values per section

Table 8. RF characteristics

Test signal: pulsed RF; t_p = 100 μs; δ = 5 %; f = 108 MHz; RF performance at V_{DS} = 55 V; I_{Dq} = 50 mA per section; T_{case} = 25 °C; unless otherwise specified; in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
G_p	power gain	P_L = 1600 W	27	28.0	-	dB
RL_{in}	input return loss	P_L = 1600 W	-	−16	-	dB
η_D	drain efficiency	P_L = 1600 W	71	74	-	%

7. Test information

7.1 Ruggedness in class-AB operation

The ART1K6FH, ART1K6FHS and ART1K6FHG are capable of withstanding a load mismatch corresponding to VSWR ≥ 65 : 1 through all phases under the following conditions: P_L = 1400 W pulsed at V_{DS} = 50 V and P_L = 1600 W pulsed at V_{DS} = 55 V; I_{Dq} = 100 mA per section; t_p = 100 μs; δ = 10 %; f = 108 MHz.

7.2 Impedance information

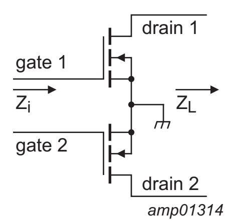


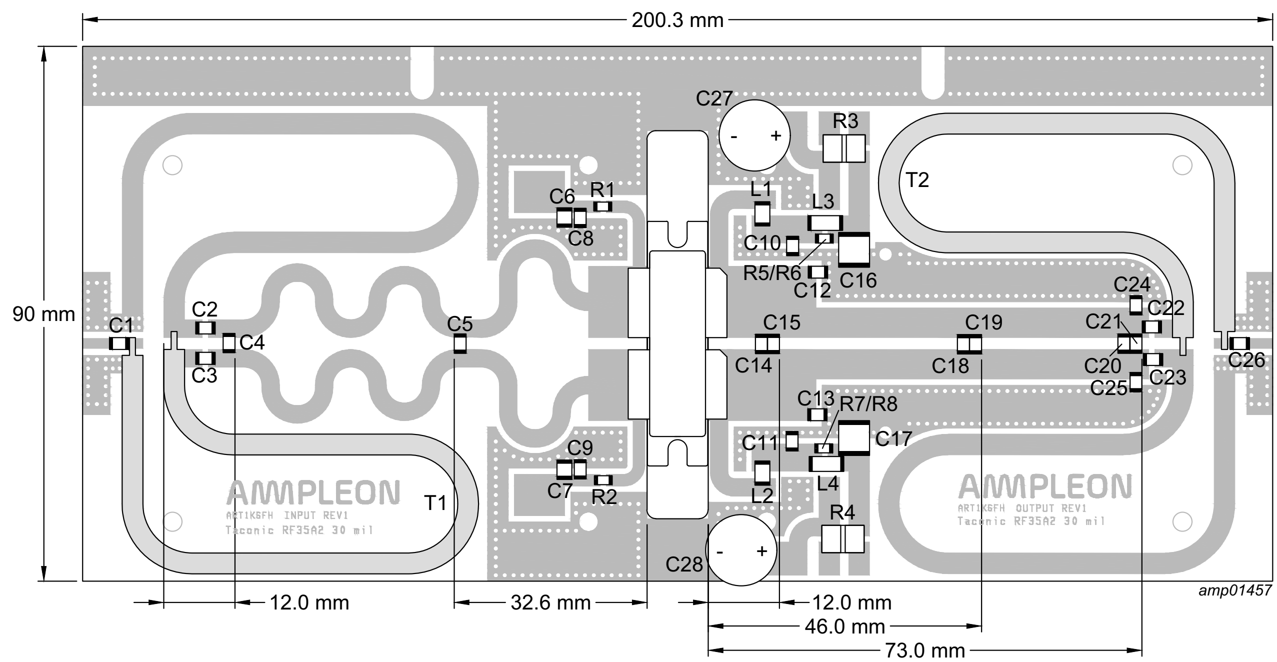
Fig 3. Definition of transistor impedance

Table 9. Typical push-pull impedance

Simulated Z_i and Z_L device impedance.

f	Z_i	Z_L	P_L
(MHz)	(Ω)	(Ω)	(W)
V_{DS} = 50 V			
108	2.4 – j8.7	3.3 + j0.7	1400
V_{DS} = 55 V			
108	2.4 – j8.7	3.5 + j0.8	1600

7.3 Test circuit



Printed-Circuit Board (PCB): RF-35; ε_r = 3.5 F/m; thickness = 0.762 mm.

See Table 10 for a list of components.

Fig 4. Component layout

Table 10. List of components

For test circuit see Figure 4.

Component	Description	Value	Remarks
C1, C26	multilayer ceramic chip capacitor	470 pF [1]	
C2, C3	multilayer ceramic chip capacitor	68 pF [1]	
C4	multilayer ceramic chip capacitor	43 pF [1]	
C5	multilayer ceramic chip capacitor	240 pF [1]	
C6, C7	multilayer ceramic chip capacitor	4.7 µF, 50 V	Murata: GRM32ER71H475KA88L
C8, C9, C10, C11	multilayer ceramic chip capacitor	820 pF [1]	
C12, C13	multilayer ceramic chip capacitor	180 pF [1]	
C14, C15	multilayer ceramic chip capacitor	39 pF [1]	
C16, C17	multilayer ceramic chip capacitor	4.7 µF, 100 V	TDK: C5750X7R2A475KT/A
C18, C19	multilayer ceramic chip capacitor	56 pF [1]	
C20, C21	multilayer ceramic chip capacitor	51 pF [1]	
C22, C23	multilayer ceramic chip capacitor	120 pF [1]	
C24, C25	multilayer ceramic chip capacitor	20 pF [1]	
C27, C28	electrolytic capacitor	2200 µF, 100 V	
L1, L2	air inductor	47 nH	Coilcraft: 1515SQ-47N
L3, L4	air inductor	82 nH	Coilcraft: 1515SQ-82N
R1, R2	resistor	4.7 kΩ	SMD 1206

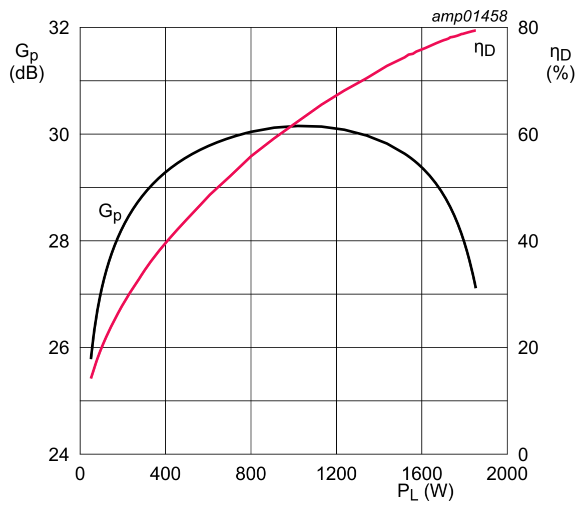
Table 10. List of components *...continued*

For test circuit see Figure 4.

Component	Description	Value	Remarks
R3, R4	resistor	0.01 Ω	Vishay: WSHP2818
R5, R6, R7, R8	resistor	9.1 Ω	SMD 1206
T1, T2	semi rigid coax	50 Ω, 160 mm	EZ141-AL-TP/M17

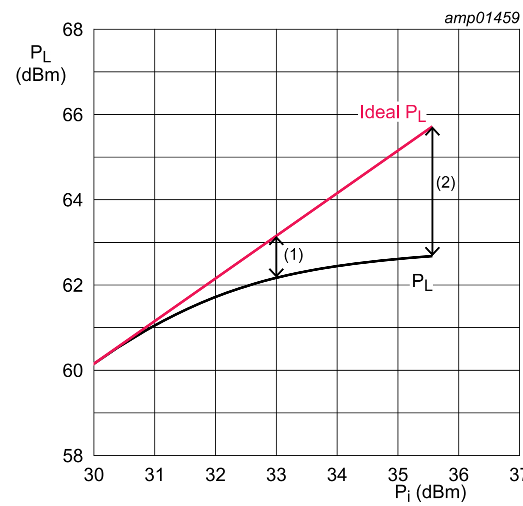
[1] American Technical Ceramics type 100B or capacitor of same quality.

7.4 Graphical data



V_{DS} = 55 V; I_{Dq} = 100 mA per section; f = 108 MHz; t_p = 100 μs; δ = 10 %.

Fig 5. Power gain and drain efficiency as function of output power; typical values

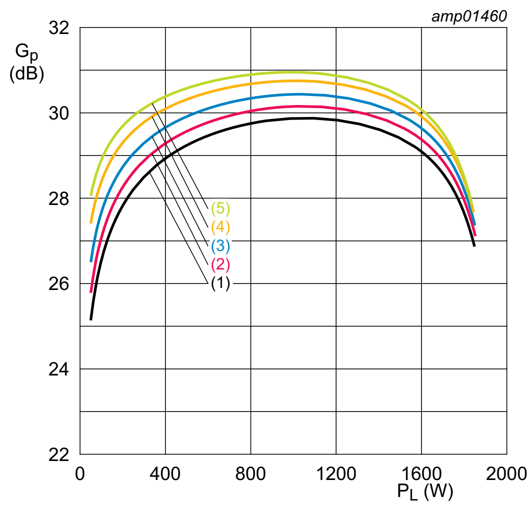


V_{DS} = 55 V; I_{Dq} = 100 mA per section; f = 108 MHz; t_p = 100 μs; δ = 10 %.

(1) $P_{L(1dB)}$ = 62.17 dBm (1650 W)

(2) $P_{L(3dB)}$ = 62.67 dBm (1850 W)

Fig 6. Output power as a function of input power; typical values



V_{DS} = 55 V; f = 108 MHz; t_p = 100 μs; δ = 10 %.

(1) I_{Dq} = 50 mA per section

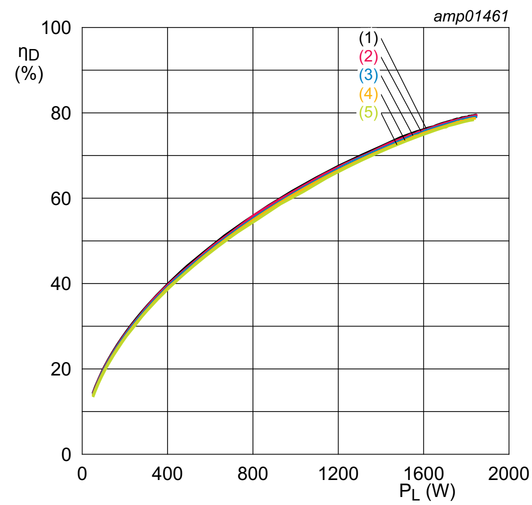
(2) I_{Dq} = 100 mA per section

(3) I_{Dq} = 200 mA per section

(4) I_{Dq} = 400 mA per section

(5) I_{Dq} = 600 mA per section

Fig 7. Power gain as a function of output power; typical values



V_{DS} = 55 V; f = 108 MHz; t_p = 100 μs; δ = 10 %.

(1) I_{Dq} = 50 mA per section

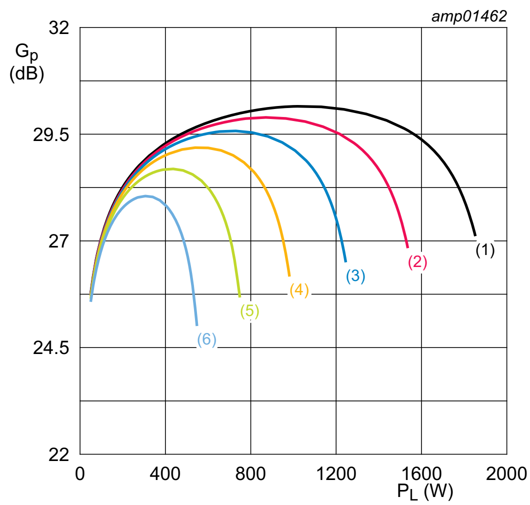
(2) I_{Dq} = 100 mA per section

(3) I_{Dq} = 200 mA per section

(4) I_{Dq} = 400 mA per section

(5) I_{Dq} = 600 mA per section

Fig 8. Drain efficiency as a function of output power; typical values



I_{Dq} = 100 mA per section; f = 108 MHz; t_p = 100 μs; δ = 10 %.

(1) V_{DS} = 55 V

(2) V_{DS} = 50 V

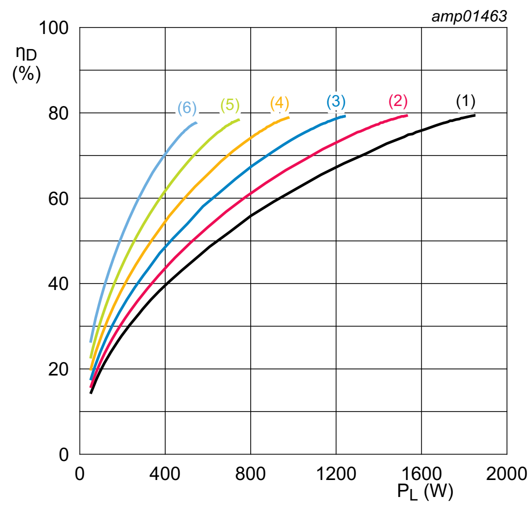
(3) V_{DS} = 45 V

(4) V_{DS} = 40 V

(5) V_{DS} = 35 V

(6) V_{DS} = 30 V

Fig 9. Power gain as a function of output power; typical values



I_{Dq} = 100 mA per section; f = 108 MHz; t_p = 100 μs; δ = 10 %.

(1) V_{DS} = 55 V

(2) V_{DS} = 50 V

(3) V_{DS} = 45 V

(4) V_{DS} = 40 V

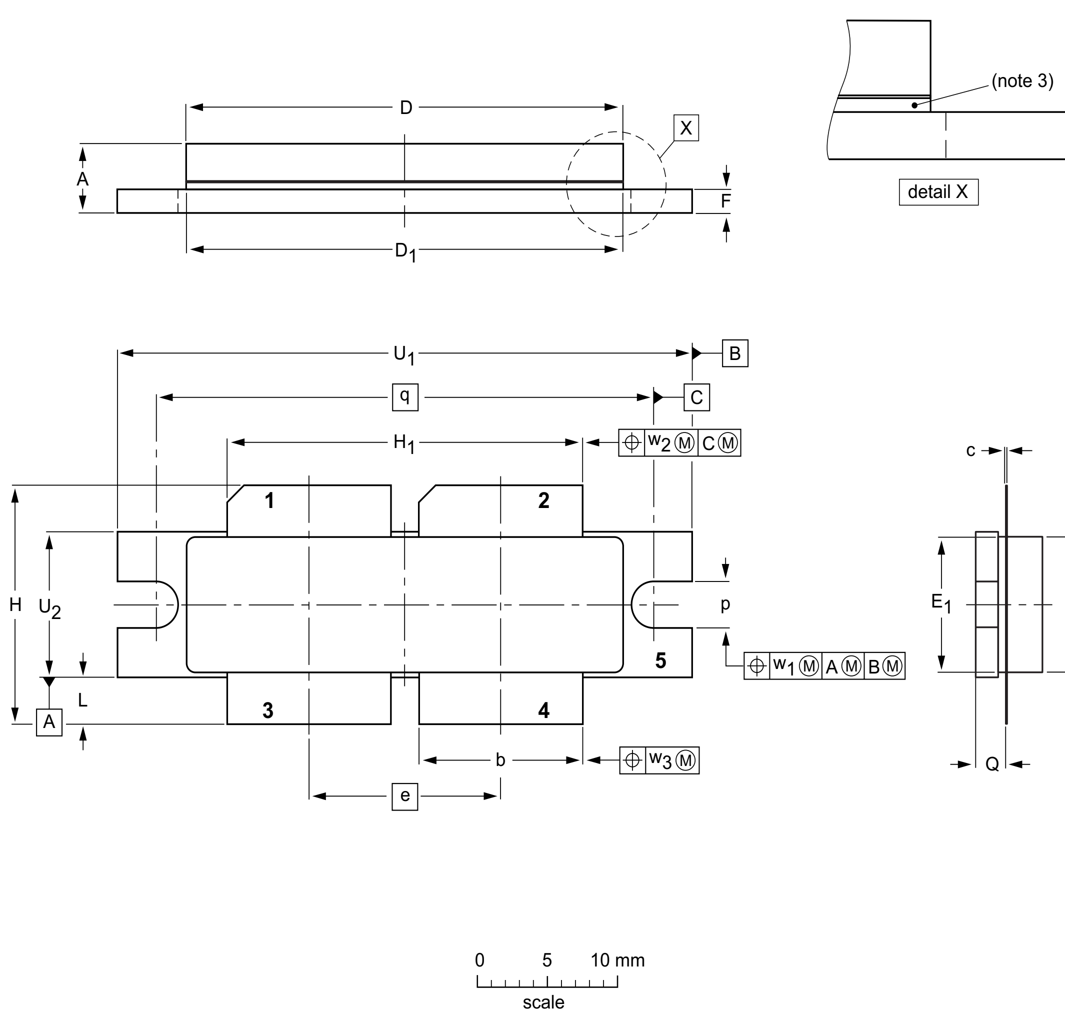
(5) V_{DS} = 35 V

(6) V_{DS} = 30 V

Fig 10. Drain efficiency as a function of output power; typical values

8. Package outline

Flanged balanced ceramic package; 2 mounting holes; 4 leads **SOT539AN**



Dimensions

Unit[(1)]		A	b	c	D	D1	E	E1	e	F	H	H1	L	p	Q	q[(2)]	U1	U2	w1	w2	w3
mm	max	4.7	11.81	0.18	31.55	31.52	9.5	9.53		1.75	17.12	25.53	3.48	3.30	2.26		41.28	10.29			
	nom								13.72							35.56			0.25	0.51	0.25
	min	4.2	11.56	0.10	30.94	30.96	9.3	9.27		1.50	16.10	25.27	2.97	3.05	2.01		41.02	10.03			
inches	max	0.185	0.465	0.007	1.242	1.241	0.374	0.375		0.069	0.674	1.005	0.137	0.130	0.089		1.625	0.405			
	nom								0.54							1.400			0.01	0.02	0.01
	min	0.165	0.455	0.004	1.218	1.219	0.366	0.365		0.059	0.634	0.995	0.117	0.120	0.079		1.615	0.395			

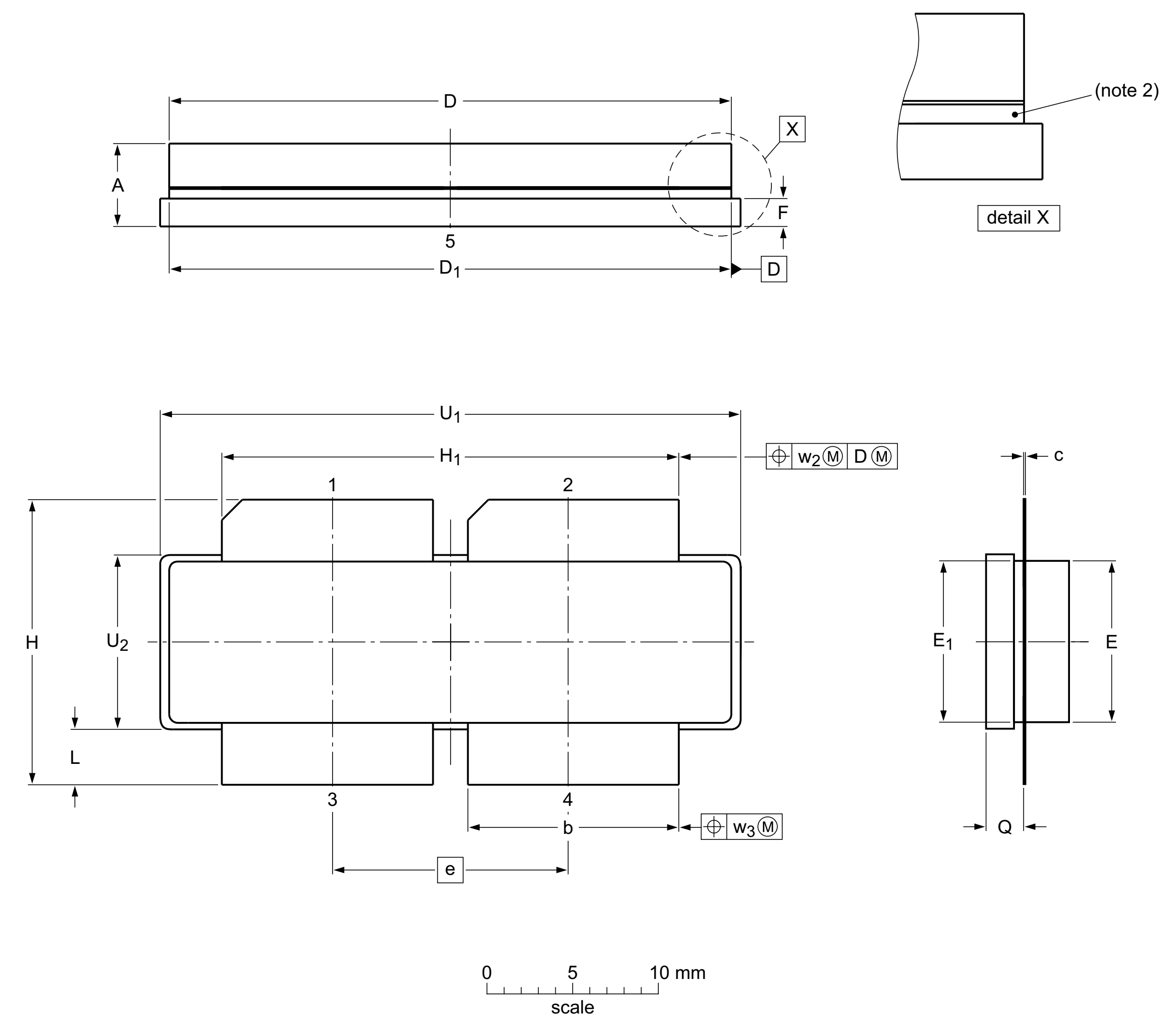
Note
1. millimeter dimensions are derived from the original inch dimensions.
2. recommended screw pitch dimension of 1.52 inch (38.6 mm) based on M3 screw.
3. ceramic window frame has a minimum thickness of 0.400 mm.

sot539an_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT539AN						20-04-20

Fig 11. Package outline SOT539AN

Earless flanged balanced ceramic package; 4 leads **SOT539BN**



Dimensions

Unit[1]		A	b	c	D	D_1	E	E_1	e	F	H	H_1	L	Q	U_1	U_2	w_2	w_3
mm	max	4.7	11.81	0.18	31.55	31.52	9.5	9.53		1.75	17.12	25.53	3.48	2.26	32.39	10.29		
	nom								13.72								0.25	0.25
	min	4.2	11.56	0.10	30.94	30.96	9.3	9.27		1.50	16.10	25.27	2.97	2.01	32.13	10.03		
inches	max	0.185	0.465	0.007	1.242	1.241	0.374	0.375		0.069	0.674	1.005	0.137	0.089	1.275	0.405		
	nom								0.54								0.01	0.01
	min	0.165	0.455	0.004	1.218	1.219	0.366	0.365		0.059	0.634	0.995	0.117	0.079	1.265	0.395		

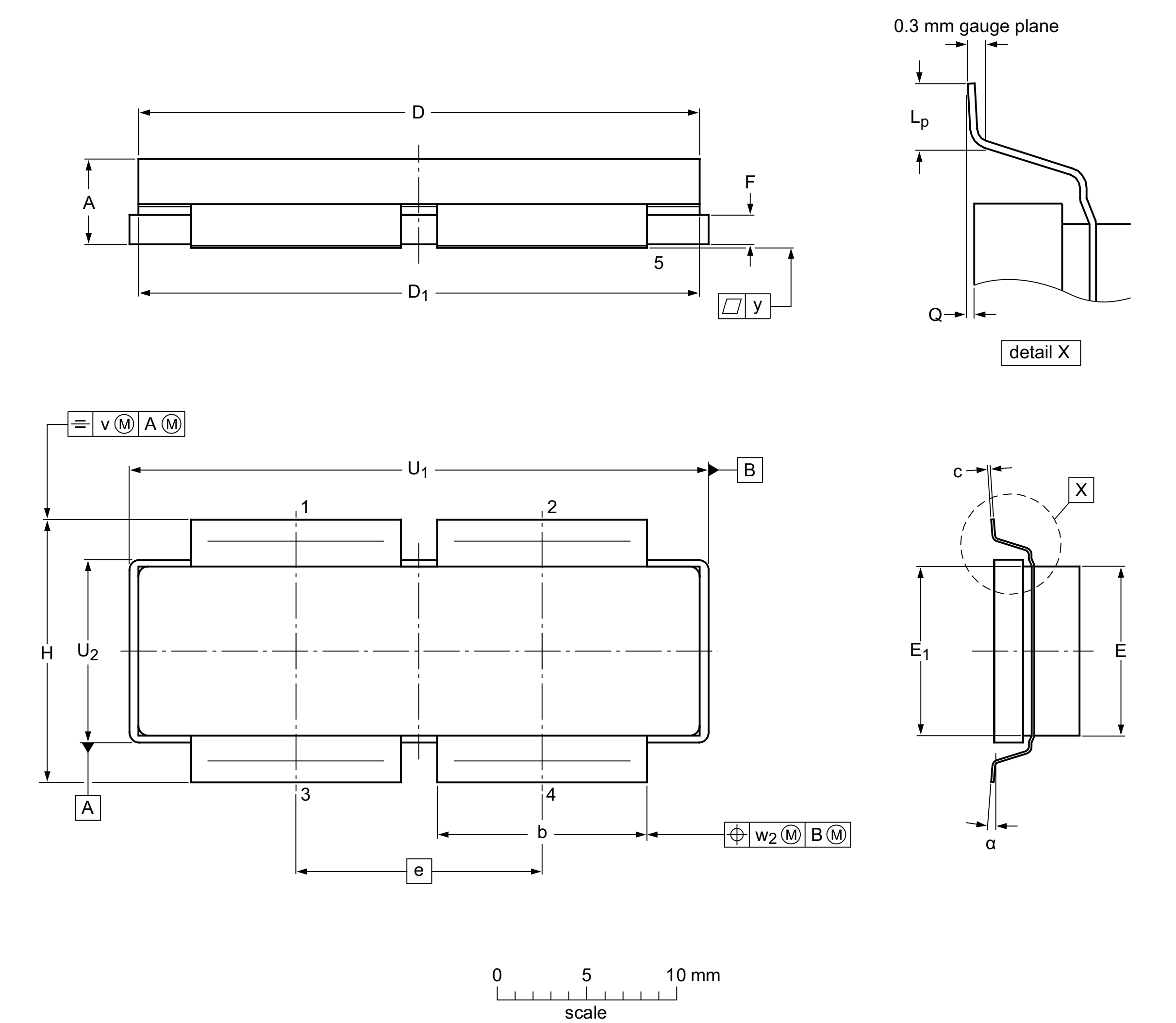
Note
1. millimeter dimensions are derived from the original inch dimensions.
2. ceramic window frame has a minimum thickness of 0.400 mm.

sot539bn_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT539BN						20-04-20

Fig 12. Package outline SOT539BN

Earless flanged LDMOST ceramic package; 4 leads **SOT1248C**



Dimensions

Unit(1)		A	b	c	D	D_1	e	E	E_1	F	H	L_p	Q	U_1	U_2	v	w_2	y	α
mm	max	5.5	11.81	0.18	31.55	31.52		9.50	9.53	1.75	14.70	1.38	0.195	32.39	10.29	0.25	0.25	0.15	7°
	nom						13.72												
	min	4.2	11.56	0.10	30.94	30.96		9.30	9.27	1.50	14.50	0.98	0.045	32.13	10.03				0°
inches	max	0.217	0.465	0.007	1.242	1.241		0.374	0.375	0.069	0.579	0.055	0.008	1.275	0.405	0.01	0.01	0.006	7°
	nom						0.540												
	min	0.165	0.455	0.004	1.218	1.219		0.366	0.365	0.059	0.571	0.039	0.002	1.265	0.395				0°

Note
1. Millimeter dimensions are derived from the original inch dimensions.

sot1248c_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1248C						~~13-04-16~~ 13-08-15

Fig 13. Package outline SOT1248C

9. Handling information

CAUTION	
	This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices. Such precautions are described in the *ANSI/ESD S20.20*, *IEC/ST 61340-5*, *JESD625-A* or equivalent standards.

Table 11. ESD sensitivity

ESD model	Class
Charged Device Model (CDM); According to ANSI/ESDA/JEDEC standard JS-002	C2A [1]
Human Body Model (HBM); According to ANSI/ESDA/JEDEC standard JS-001	2 [2]

[1] CDM classification C2A is granted to any part that passes after exposure to an ESD pulse of 500 V.

[2] HBM classification 2 is granted to any part that passes after exposure to an ESD pulse of 2000 V.

10. Abbreviations

Table 12. Abbreviations

Acronym	Description
CW	Continuous Wave
ESD	ElectroStatic Discharge
FM	Frequency Modulation
ISM	Industrial, Scientific and Medical
LDMOS	Laterally Diffused Metal-Oxide Semiconductor
MRI	Magnetic Resonance Imaging
MTF	Median Time to Failure
RoHS	Restriction of Hazardous Substances
SMD	Surface Mounted Device
UHF	Ultra High Frequency
VHF	Very High Frequency
VSWR	Voltage Standing Wave Ratio

11. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
ART1K6FH_1K6FHS_1K6FHG v.3	20220708	Product data sheet	-	ART1K6FH_1K6FHS_1K6FHG v.2
Modifications:	• Table 4 on page 3: changed values gate-source voltage • Table 6 on page 5: changed value gate-source voltage			
ART1K6FH_1K6FHS_1K6FHG v.2	20220322	Product data sheet	-	ART1K6FH v.1
ART1K6FH v.1	20200925	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.ampleon.com.

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14. Contents

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