

Keywords: protection, high-current output drivers, power supply, dV/dt

## APPLICATION NOTE 6093 TAKE THE EDGE OFF HIGH DV/DT SUPPLIES

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Abstract: There are times when high dV/dt rise times on the power supply can cause problems with downstream components. This is especially true in 24V powered industrial systems with high current output drivers. This application note describes how to control the rise time while limiting the power loss through the control FET.

## Overview

High dV/dt rise times on the power supply can cause problems with downstream components. This is especially true in 24V-powered industrial and automotive systems with high-current output drivers. This design idea describes how to control the rise time while limiting the power loss through the control FET.

## Limiting the Rise Time

For many systems, a simple pFET circuit with associated components is enough to limit the supply's rise time. However, when currents reach 8A and beyond, the  $R_{DSON}$  of the pFET can cause heat to rise in the system. An nFET with lower  $R_{DSON}$  is a nice alternative.

The MAX16127 is a 3mm x 3mm nFET controller designed for overvoltage protection. It can also be used to control the ramp of a supply voltage. The power-good active-low FLAG output on this protection circuit gives it the unique ability to enable downstream devices when the controlled voltage is at 90% of the input voltage, regardless of the input voltage. This feature is a nice improvement over setting a fixed turn-on voltage or delay time, especially in industrial and automotive systems where input voltages can vary over a wide range.

The circuit in **Figure 1** shows the basic configuration used to ramp  $V_{IN}$ . The GATE pin of the MAX16127 is a current-output circuit coming from an internal charge pump. It drives the gate of an nFET transistor to about 10V above the source of the nFET. The additional capacitor on GATE can be used to control the risetime of the nFET gate voltage, and the value of the capacitor can be adjusted for the desired slew rate. In this case C1, a 220nF capacitor is shown. Resistor R2 (1k $\Omega$ ) is in series with C1. R2 isolates C1, so that when the MAX16127 turns off during an overvoltage or fault condition, there is a quick turn-off time.

The nFET will be in its linear region while the gate ramps. Consequently, large amounts of power dissipation can be seen if all of the downstream circuits start working while it is ramping. The active-low FLAG pin of the MAX16127 is, in this case, used as an enable pin for downstream drivers and power supplies. Figure 2 and Figure 3 show how the active-low FLAG-enable signal moves out in time as  $V_{IN}$  changes, always enabling when  $V_{SUPPLY}$  is at 90% of  $V_{IN}$ . When using active-low FLAG as an enable, you only have to worry about sizing the nFET for that last 10% when everything is on.

The GATE pin of the MAX16127 has a nominal current of  $180\mu$ A, and you calculate your gate-drive rise time using the formula: I = C dV/dT. Using the 220nF capacitor shown gives us a dV/dT of approximately 0.82V/ms. Figure 2 shows V<sub>SUPPLY</sub> ramping to 30V in approximately 40ms, which is close to what we would expect, as the gate drive ramps linearly.

This circuit also provides the standard overvoltage protection using resistors R5 and R6, and the undervoltage lockout using resistors R3 and R7.



Figure 1. Schematic for rise time control circuit.



Figure 2. Waveforms and active-low FLAG behavior for a 30V  $V_{\rm IN^{\circ}}$ 



Figure 3. Waveforms and active-low FLAG behavior for an 18V  $V_{IN}$ .

## Sizing the FET

In this example, we use the 90% active-low FLAG to enable a downstream load of 10A. Assuming a maximum of 30V on V<sub>IN</sub>, we need to size the FET so that it can handle the average power as V<sub>SUPPLY</sub> ramps from 27V to 30V in about 4ms. The average power will be  $\frac{1}{2}$  (V<sub>IN</sub> - V<sub>OUT</sub>) × I or 1.5V × 10A = 15W, but for a short duration. Most power FET data sheets will have a safe-operating-area (SOA) graph that shows V<sub>DS</sub> versus current with an overlay of time. Check the SOA to size your FET.

A similar version of this article appeared the May 2015 issue of *How2Power* magazine.

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