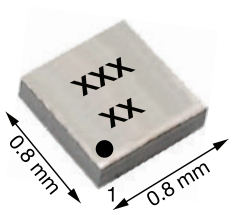
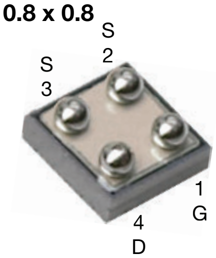
P-Channel 8 V (D-S) MOSFET

PRODUCT SUMMARY			
V_{DS} (V)	$R_{DS(on)}$ (Ω)	I_D (A) [a]	Q_g (TYP.)
-8	0.068 at V_{GS} = -4.5 V	-3.1	6.7 nC
	0.088 at V_{GS} = -2.5 V	-2.7	
	0.155 at V_{GS} = -1.5 V	-2.1	
	0.290 at V_{GS} = -1.2 V	-0.5	

MICRO FOOT® 0.8 x 0.8



Backside View



Bump Side View

Marking Code: xx = AC
xxx = Date/Lot traceability code

Ordering Information:
Si8805EDB-T2-E1 (lead (Pb)-free and halogen-free)

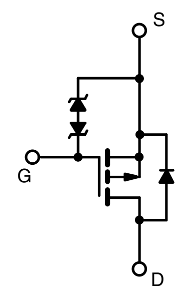
FEATURES

- TrenchFET® power MOSFET
- Ultra small 0.8 mm x 0.8 mm outline
- Ultra thin 0.357 mm height
- Typical ESD protection 1500 V HBM
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

Pb-free
RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

- Portable devices such as cell phones, smart phones, tablet PCs, and media players
  - Load switch for low voltage gate drive
  - Load switch for 1.2 V power line



P-Channel MOSFET

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V_{DS}	-8	V
Gate-Source Voltage		V_{GS}	± 5	
Continuous Drain Current (T_J = 150 °C)	T_A = 25 °C	I_D	-3.1 [a]	A
	T_A = 70 °C		-2.5 [a]	
	T_A = 25 °C		-2.2 [b]	
	T_A = 70 °C		-1.8 [b]	
Pulsed Drain Current		I_{DM}	-15	
Continuous Source-Drain Diode Current	T_A = 25 °C	I_S	-0.7 [a]	
	T_A = 25 °C		-0.4 [b]	
Maximum Power Dissipation	T_A = 25 °C	P_D	0.9 [a]	W
	T_A = 70 °C		0.6 [a]	
	T_A = 25 °C		0.5 [b]	
	T_A = 70 °C		0.3 [b]	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	-55 to +150	°C
Soldering Recommendations (Peak Temperature) [c]			260	

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum Junction-to-Ambient [a, d]	t ≤ 5 s	R_{thJA}	105	135	°C/W
Maximum Junction-to-Ambient [b, e]			200	260	

Notes

a. Surface mounted on 1" x 1" FR4 board with full copper, t = 5 s.
b. Surface mounted on 1" x 1" FR4 board with minimum copper, t = 5 s.
c. Refer to IPC/JEDEC® (J-STD-020), no manual or hand soldering.
d. Maximum under steady state conditions is 185 °C/W.
e. Maximum under steady state conditions is 330 °C/W.

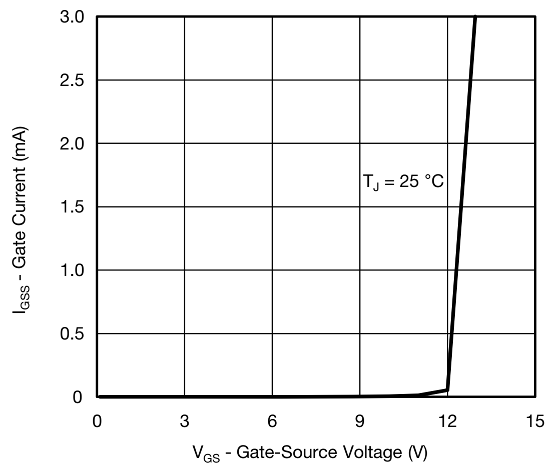
SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = -250 µA	-8	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	I_D = -250 µA	-	-4	-	mV/°C
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$		-	2.1	-	
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = -250 µA	-0.35	-	-0.7	V
Gate-Source Leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 5 V	-	-	± 1.5	µA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = -8 V, V_{GS} = 0 V	-	-	-1	
		V_{DS} = -8 V, V_{GS} = 0 V, T_J = 55 °C	-	-	-10	
On-State Drain Current [a]	$I_{D(on)}$	$V_{DS} \leq$ -4 V, V_{GS} = -4.5 V	-5	-	-	A
Drain-Source On-State Resistance [a]	$R_{DS(on)}$	V_{GS} = -4.5 V, I_D = -1.5 A	-	0.056	0.068	Ω
		V_{GS} = -2.5 V, I_D = -1.5 A	-	0.070	0.088	
		V_{GS} = -1.5 V, I_D = -0.5 A	-	0.115	0.155	
		V_{GS} = -1.2 V, I_D = -0.3 A	-	0.190	0.290	
Forward Transconductance [a]	g_{fs}	V_{DS} = -4 V, I_D = -1.5 A	-	8	-	S
Dynamic [b]						
Total Gate Charge	Q_g	V_{DS} = -4 V, V_{GS} = -4.5 V, I_D = -1.5 A	-	6.7	10	nC
Gate-Source Charge	Q_{gs}		-	0.7	-	
Gate-Drain Charge	Q_{gd}		-	1.8	-	
Gate Resistance	R_g	f = 1 MHz	-	10	-	Ω
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = -4 V, R_L = 2.7 Ω $I_D \cong$ -1.5 A, V_{GEN} = -4.5 V, R_g = 1 Ω	-	13	25	ns
Rise Time	t_r		-	13	25	
Turn-Off Delay Time	$t_{d(off)}$		-	25	50	
Fall Time	t_f		-	17	35	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	T_C = 25 °C	-	-	-0.7	A
Pulse Diode Forward Current	I_{SM}		-	-	-15	
Body Diode Voltage	V_{SD}	I_S = -1.5 A, V_{GS} = 0 V	-	-0.8	-1.2	V
Body Diode Reverse Recovery Time	t_{rr}	I_F = -1.5 A, dI/dt = 100 A/µs, T_J = 25 °C	-	35	70	ns
Body Diode Reverse Recovery Charge	Q_{rr}		-	15	30	nC
Reverse Recovery Fall Time	t_a		-	15	-	ns
Reverse Recovery Rise Time	t_b		-	20	-	

Notes

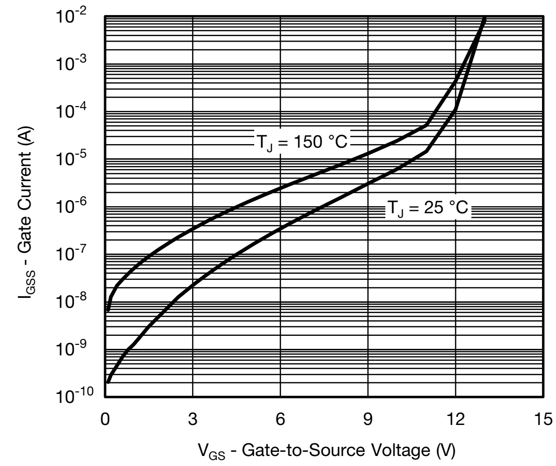
a. Pulse test; pulse width ≤ 300 µs, duty cycle ≤ 2 %.
b. Guaranteed by design, not subject to production testing.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

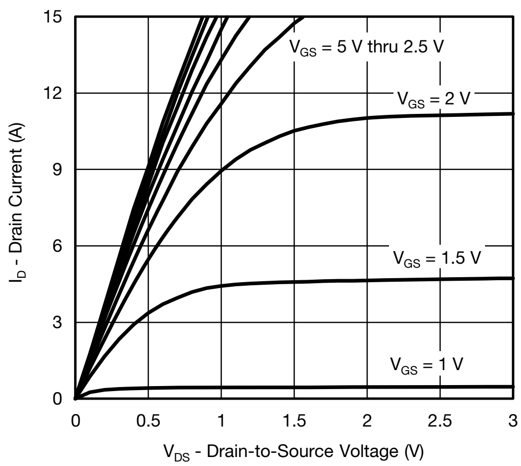
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



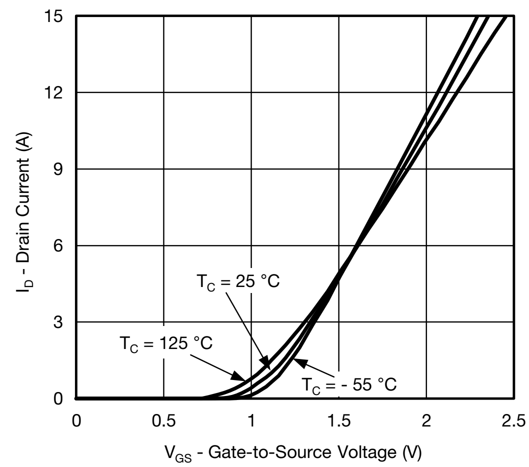
Gate Current vs. Gate-Source Voltage



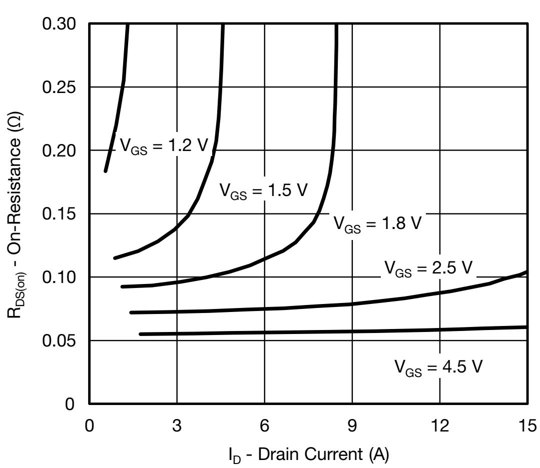
Gate Current vs. Gate-Source Voltage



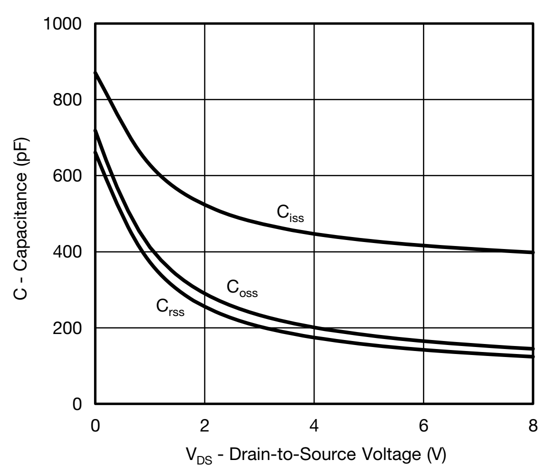
Output Characteristics



Transfer Characteristics

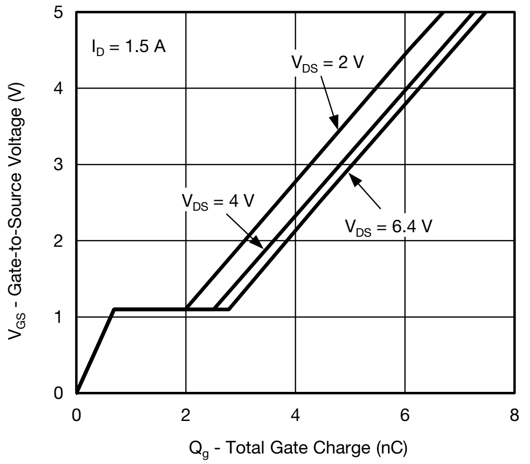


On-Resistance vs. Drain Current

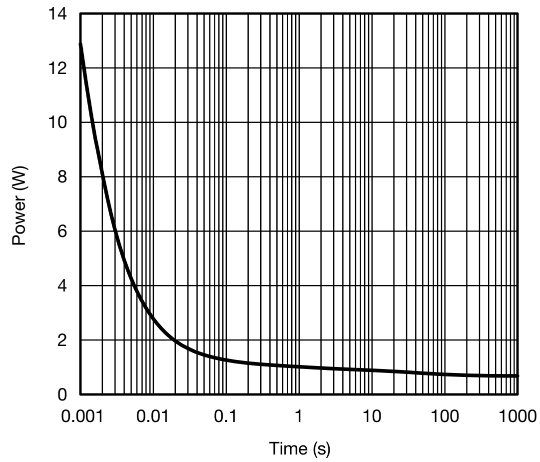


Capacitance

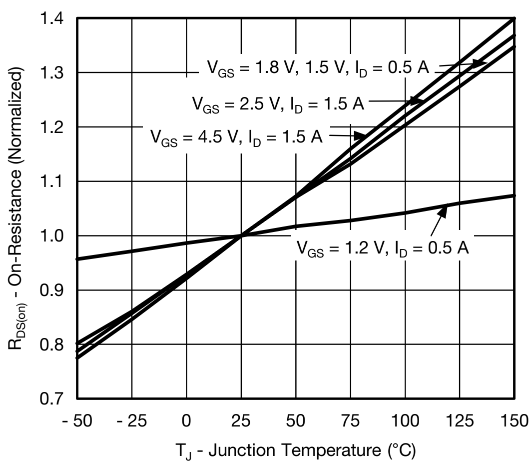
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



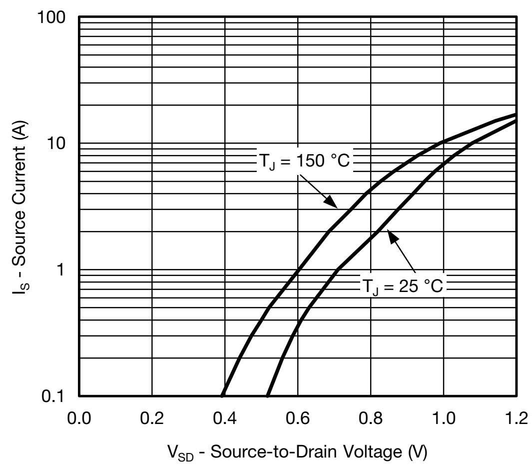
Gate Charge



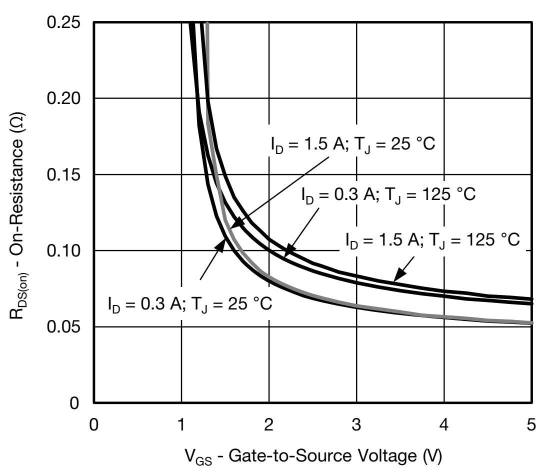
Single Pulse Power (Junction-to-Ambient)



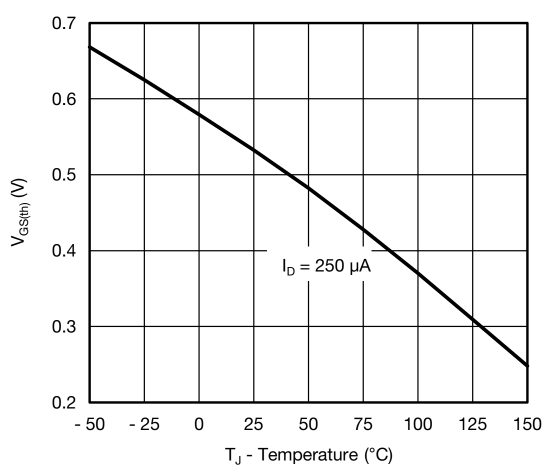
On-Resistance vs. Junction Temperature



Source-Drain Diode Forward Voltage

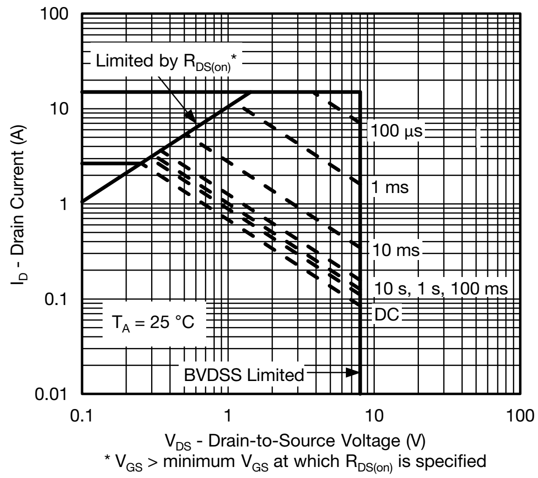


On-Resistance vs. Gate-to-Source Voltage

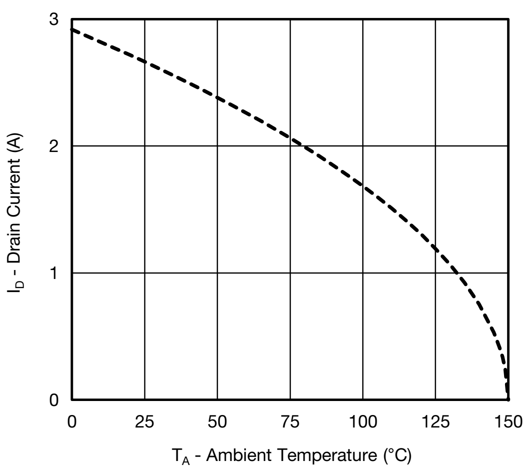


Threshold Voltage

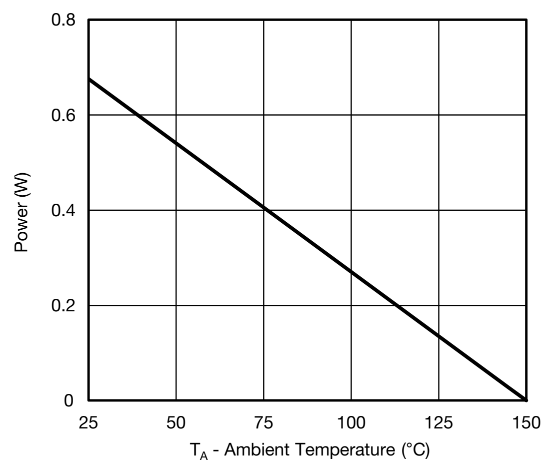
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Safe Operating Area, Junction-to-Ambient



Current Derating*



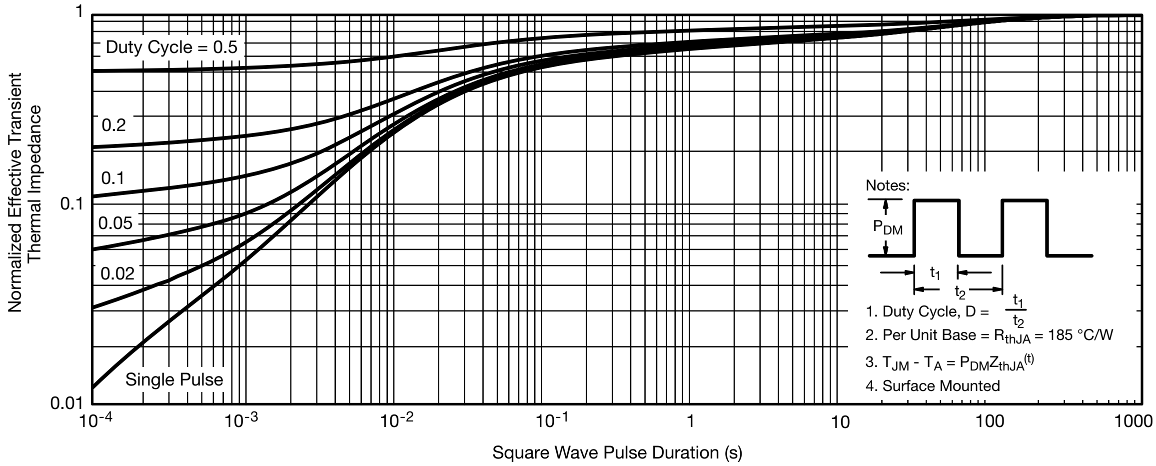
Power Derating

Note

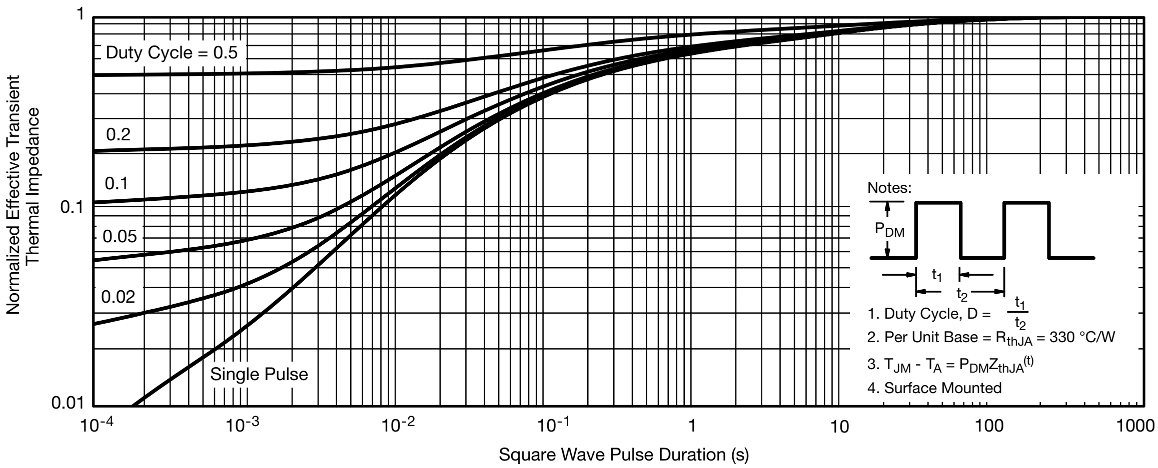
When mounted on 1" x 1" FR4 with full copper.

* The power dissipation P_D is based on $T_{J\ (max.)}$ = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



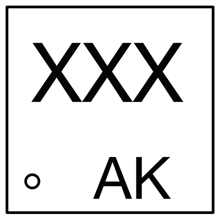
Normalized Thermal Transient Impedance, Junction-to-Ambient (On 1" x 1" FR4 Board with Maximum Copper)



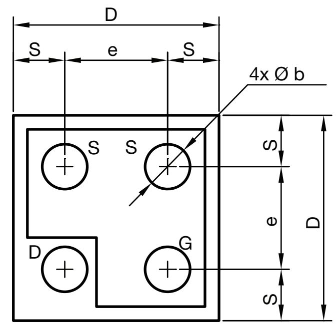
Normalized Thermal Transient Impedance, Junction-to-Ambient (On 1" x 1" FR4 Board with Minimum Copper)

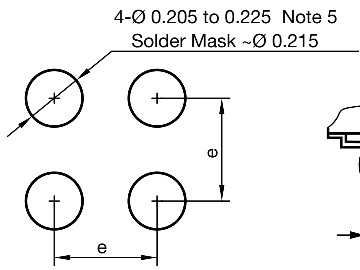
Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?67935.

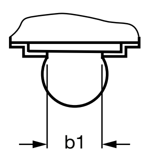
MICRO FOOT®: 4-Bump (0.8 mm x 0.8 mm, 0.4 mm Pitch)



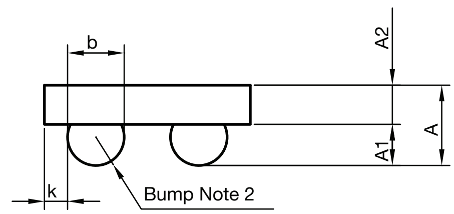
Mark on Backside of die







Note 4



Notes

(1) Laser mark on the backside surface of die
(2) Bumps are 95.5 % Sn,3.8 % Ag,0.7 % Cu
(3) "i" is the location of pin 1
(4) "b1" is the diameter of the solderable substrate surface, defined by an opening in the solder resist layer solder mask defined.
(5) Non-solder mask defined copper landing pad.

DIM.	MILLIMETERS [a]			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.328	0.365	0.402	0.0129	0.0144	0.0158
A1	0.136	0.160	0.184	0.0053	0.0062	0.0072
A2	0.192	0.205	0.218	0.0076	0.0081	0.0086
b	0.200	0.220	0.240	0.0078	0.0086	0.0094
b1		0.175			0.0068	
e		0.400			0.0157	
S	0.160	0.180	0.200	0.0062	0.0070	0.0078
D	0.720	0.760	0.800	0.0283	0.0299	0.0314
K	0.040	0.070	0.100	0.0015	0.0027	0.0039

Note

a. Use millimeters as the primary measurement.

ECN: T15-0053-Rev. A, 16-Feb-15
DWG: 6033

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