Cross-ship of Lead-free Bump and Substrates in Lead-free (FFG/FBG/SBG) Packages

XCN16022 (v1.0) October 31, 2016 Product Change Notice

Overview

The purpose of this notification is to announce that selected Xilinx lead-free flip chip products denoted by the package code “FFG”, “FBG”, or “SBG” will be shipped with *either* the current eutectic C4 bump and associated substrate *or* the new lead-free C4 bump and associated lead-free substrate. The external packaging and the current lead-free balls will not be changed. Form, fit, function and reliability will remain the same.

Description

Xilinx offers lead free components that comply with the European Union’s RoHS 2 directive (2011/95/EU). RoHS compliant devices are specified by adding the character “G” to the package designator portion of the part number. Under the current RoHS directive, Xilinx flip-chip packages are exempt from the full lead-free requirements under Exemption 15. Exemption 15 specifies that lead is allowed in solder bumps to complete a viable electrical connection between semiconductor die and substrate within integrated circuit flip chip packages.

In 2015, the RoHS committee planned to remove Exemption 15 in July 2016. Thus, Xilinx qualified and introduced versions of these parts with lead-free solder bump material between the semiconductor die and the substrate. In early 2016, however, removal of RoHS Exemption 15 was delayed. We do know that the RoHS directive will eventually eliminate Exemption 15 for newer device technologies and smaller die sizes, in 2018 at the earliest. In order to ease the transition for Xilinx and customers well ahead of the transition date, Xilinx will begin the gradual transition to lead-free material for the solder bumps between the semiconductor die and the substrate. Eligible devices are in the Virtex®-5, Virtex®-6, Artix®-7, Kintex®-7, Virtex®-7 FPGAs and Zynq®-7000 families. Defense-grade “XQ” and Automotive “XA” device-packages are not affected by this PCN.

The specific material that will change includes the C4 Bump on the wafer, the substrate, and the underfill used in assembly. The current RoHS parts in “G” packages use bumps, substrate, and underfill appropriate for eutectic solder (*eutectic material set*). The new bumps, substrate, and underfill (*lead-free material set*) enables the use of fully lead-free solder bumps.

There are no differences in package reliability, form, fit or function using the lead-free material set. There are no external package changes (BGA balls will be remain lead-free). There are no changes to the package outline drawing. All packages meet the 8 mil (0.2 mm) package coplanarity specifications and should provide seamless board mount results.

Until the cross ship date of July 1 2017, the products with “G” packages will only be shipped with the eutectic material set. After the cross ship date, the products with “G” packages will be shipped with *either* eutectic or lead-free material sets. When the RoHS Directive changes to remove Exemption 15, all product should be shifted to the lead-free material set already. Note that all affected product shipped will meet the RoHS Directive.

Products Affected

This change affects all speed, package, and temperature variations of “XC” commercial (C), industrial (I) and extended (E) device-package combinations listed in the tables below. Any associated Specification Control Documents (SCDs) are also affected.

Table 1: **Virtex-5 Products Affected**

Device	Package
XC5VFX30T	FFG665
XC5VFX70T	FFG1136
XC5VFX70T	FFG665
XC5VFX100T	FFG1136
XC5VFX100T	FFG1738
XC5VLX20T	FFG323
XC5VLX30	FFG324
XC5VLX30	FFG676
XC5VLX30T	FFG323
XC5VLX30T	FFG665
XC5VLX50	FFG1153
XC5VLX50	FFG324
XC5VLX50	FFG676
XC5VLX50T	FFG1136
XC5VLX50T	FFG665
XC5VLX85	FFG1153
XC5VLX85	FFG676
XC5VLX85T	FFG1136

Device	Package
XC5VSX35T	FFG665
XC5VSX50T	FFG1136
XC5VSX50T	FFG665
XC5VSX95T	FFG1136
XC5VLX110	FFG1153
XC5VLX110	FFG1760
XC5VLX110	FFG676
XC5VLX110T	FFG1136
XC5VLX110T	FFG1738
XC5VLX155	FFG1153
XC5VLX155	FFG1760
XC5VLX155T	FFG1136
XC5VLX155T	FFG1738
XCE05L11	FFG1153
XCE05L11T	FFG1136
XCE05L15	FFG1153
XCE05S05T	FFG1136

Table 2: **Virtex-6 Products Affected**

Device	Package
XC6VCX75T	FFG484
XC6VCX75T	FFG784
XC6VCX130T	FFG1156
XC6VCX130T	FFG484
XC6VCX130T	FFG784
XC6VCX195T	FFG1156
XC6VCX195T	FFG784
XC6VCX240T	FFG784
XC6VCX240T	FFG1156
XC6VCX240T	FFG1759
XC6VLX75T	FFG484
XC6VLX75T	FFG784

Device	Package
XC6VLX130T	FFG1156
XC6VLX130T	FFG484
XC6VLX130T	FFG784
XC6VLX195T	FFG1156
XC6VLX195T	FFG784
XC6VLX240T	FFG784
XC6VLX240T	FFG1156
XC6VLX240T	FFG1759
XC6VHX250T	FFG1154
XC6VHX255T	FFG1155
XC6VHX255T	FFG1923
XCE06L19T	FFG1156

Table 3: **7 Series and Zynq-7000 Products Affected**

Device	Package
XC7A200T	FBG676
XC7A200T	FFG1156
XC7A200T	FBG484
XC7A200T	FFG676
XC7A200T	SBG484
XC7K160T	FFG676
XC7K160T	FBG484
XC7K160T	FBG676
XC7K325T	FBG676
XC7K325T	FBG900
XC7K325T	FFG900
XC7K325T	FFG676
XC7K355T	FFG901
XC7K410T	FBG900
XC7K410T	FFG900
XC7K410T	FBG676
XC7K410T	FFG676
XC7K420T	FFG1156
XC7K420T	FFG901
XC7K480T	FFG1156
XC7K480T	FFG901
XC7K70T	FBG676

Device	Package
XC7K70T	FBG484
XC7K70T	FFG484
XC7V585T	FFG1157
XC7V585T	FFG1761
XC7VX330T	FFG1761
XC7VX330T	FFG1157
XC7VX415T	FFG1158
XC7VX415T	FFG1157
XC7VX415T	FFG1927
XC7Z030	FBG484
XC7Z030	FBG676
XC7Z030	FFG676
XC7Z030	SBG485
XC7Z035	FFG900
XC7Z035	FFG676
XC7Z035	FBG676
XC7Z045	FFG900
XC7Z045	FFG676
XC7Z045	FBG676
XC7Z100	FFG1156
XC7Z100	FFG900

Key Dates and Ordering Information

Xilinx will begin cross-shipping the new material set for bumps, substrate, and underfill on July 1, 2017.

Traceability

To enable traceability, any products with “G” packages shipped that use the new lead-free material set will be marked with a special Pb-Free character in the upper right corner of the part as shown in Figure 1 below. There will be no mark for the eutectic material set. Marking changes are reflected in the product documents UG475, UG865, UG365 and UG195, available on www.xilinx.com.

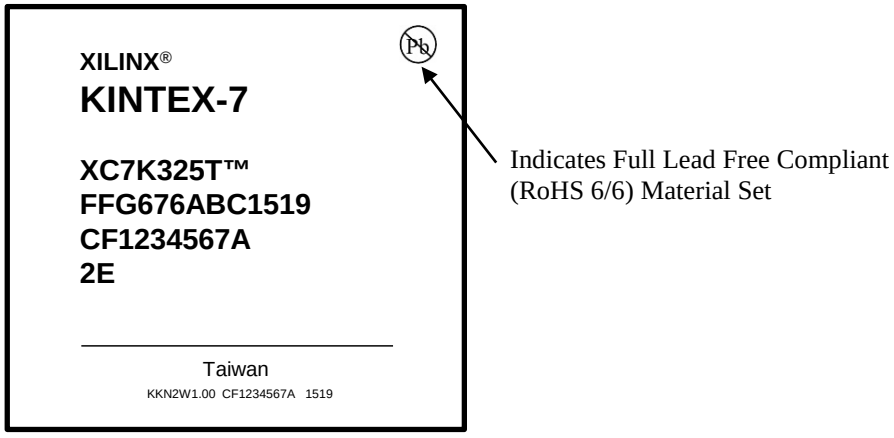

Figure 1: **Package Topmark**

Note: Refer to XCN16014 for 2D barcode additional marking.

Qualification Data

Qualification data will be available and provided upon request.

Response

No response is required. For additional information or questions, please contact Xilinx Technical Support.

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Revision History

The following table shows the revision history for this document.

Date	Version	Revision
10/31/16	1.0	Initial release.

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