

Data Sheet

1.2V Drive Pch MOSFET

RZE002P02

●Structure

Silicon P-channel MOSFET

● Features

- 1) High speed switching.
- 2) Small package (EMT3).
- 3) 1.2V drive.

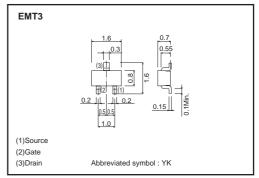
Applications

Switching

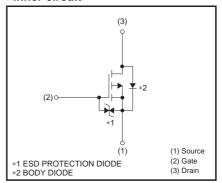
Package specifications

	Package	Taping
Type	Code	TL
	Basic ordering unit (pieces)	3000
RZE002P02		0

●Dimensions (Unit:mm)



●Inner circuit



●Absolute maximum ratings (Ta=25°C)

Parameter		Symbol	Limits	Unit
Drain-source voltage		V_{DSS}	-20	V
Gate-source voltage		V _{GSS}	±10	V
Drain current	Continuous	I_D	±200	mA
Drain current	Pulsed	I _{DP} *1	±800	mA
Souce current Continuous		Is	-100	mA
(Body diode)	Pulsed	I _{SP} *1	-800	mA
Total power dissipation		P _D *2	150	mW
Channel temperature		Tch	150	°C
Range of storage temperature		Tstg	-55 to +150	°C

Thermal resistance

Parameter	Symbol	Limits	Unit
Channel to ambient	Rth(ch-a)*	833	°C/W

^{*} Each terminal mounted on a recommended land

^{*1} Pw≤10μs, Duty cycle≤1% *2 Each terminal mounted on a recommended land

RZE002P02 Data Sheet

●Electrical characteristics (Ta=25°C)

Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
Gate-source leakage	Igss	_	-	±10	μΑ	V _{GS} = ±10V, V _{DS} =0V
Drain-source breakdown voltage	$V_{(BR)\;DSS}$	-20	_	_	V	I _D = -1mA, V _G S=0V
Zero gate voltage drain current	IDSS	-	-	-1	μΑ	V _{DS} = -20V, V _{GS} =0V
Gate threshold voltage	V _{GS (th)}	-0.3	-	-1.0	V	$V_{DS} = -10V, I_{D} = -100\mu A$
		_	8.0	1.2	Ω	I _D = -200mA, V _G S= -4.5V
Ctatia duain annua an atata		_	1.0	1.5	Ω	I _D = -100mA, V _G S= -2.5V
Static drain-source on-state resistance	R _{DS (on)} *	1	1.3	2.2	Ω	Ip= -100mA, Vgs= -1.8V
resistance		-	1.6	3.5	Ω	I _D = -40mA, V _G S= -1.5V
		-	2.4	9.6	Ω	I _D = -10mA, V _{GS} = -1.2V
Forward transfer admittance	Y _{fs} *	0.2	-	_	S	V _{DS} = -10V, I _D = -200mA
Input capacitance	Ciss	_	115	_	pF	V _{DS} = -10V
Output capacitance	Coss	_	10	_	pF	V _{GS} = 0V
Reverse transfer capacitance	Crss	-	6	_	pF	f=1MHz
Turn-on delay time	t _{d (on)} *	_	6	_	ns	V _{DD} ≒ −10V
Rise time	tr *	_	4	_	ns	I _D = −100mA V _G s= −4.5V
Turn-off delay time	t _{d (off)} *	_	17	_	ns	VGS= -4.5 V RL ≒ 100Ω
Fall time	t _f *	-	17	_	ns	R _G = 10Ω
Total gate charge	Qg *	_	1.4	-	nC	V _{DD} ≒ −10V R _L ≒ 50Ω
Gate-source charge	Qgs *	-	0.3	_	nC	$I_D = -200 \text{mA}$ $R_G = 10\Omega$
Gate-drain charge	Q _{gd} *	-	0.3	_	nC	Vgs= -4.5V

^{*}Pulsed

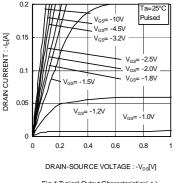
●Body diode characteristics (Source-drain)

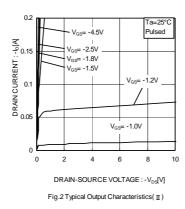
Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
Forward voltage	Vsp*	_	_	-1.2	V	I _S = -200mA, V _{GS} =0V

^{*}Pulsed

RZE002P02 **Data Sheet**

•Electrical characteristics curves





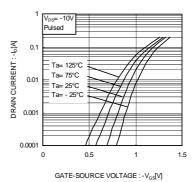


Fig.1 Typical Output Characteristics(I)

Fig.3 Typical Transfer Characteristics

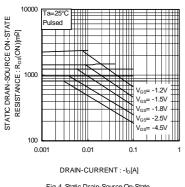


Fig.4 Static Drain-Source On-State Resistance vs. Drain Current(I)

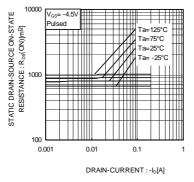


Fig.5 Static Drain-Source On-State Resistance vs. Drain Current(II)

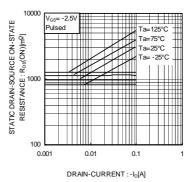


Fig.6 Static Drain-Source On-State Resistance vs. Drain Current(Ⅲ)

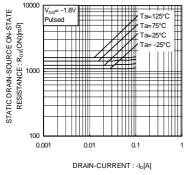


Fig.7 Static Drain-Source On-State Resistance vs. Drain Current(IV)

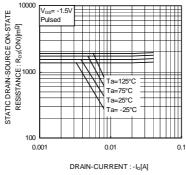


Fig.8 Static Drain-Source On-State Resistance vs. Drain Current(V)

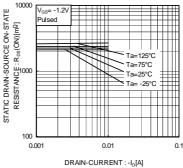
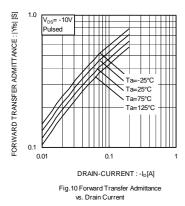
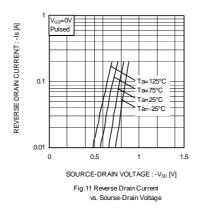


Fig.9 Static Drain-Source On-State Resistance vs. Drain Current(VI)





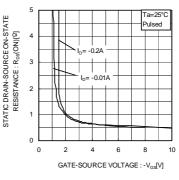
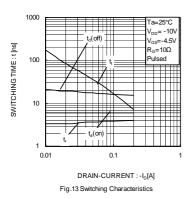
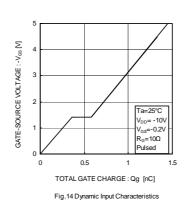
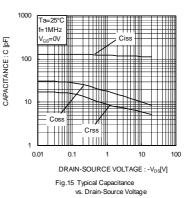


Fig.12 Static Drain-Source On-State Resistance vs. Gate Source Voltage







●Measurement circuit

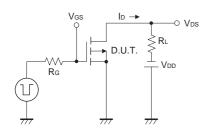


Fig.1-1 Switching Time Measurement Circuit

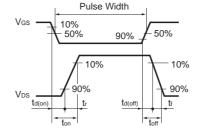


Fig.1-2 Switching Waveforms

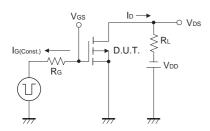


Fig.2-1 Gate Charge Measurement Circuit

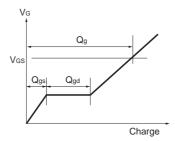


Fig.2-2 Gate Charge Waveform

●Notice

This product might cause chip aging and breakdown under the large electrified environment.

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