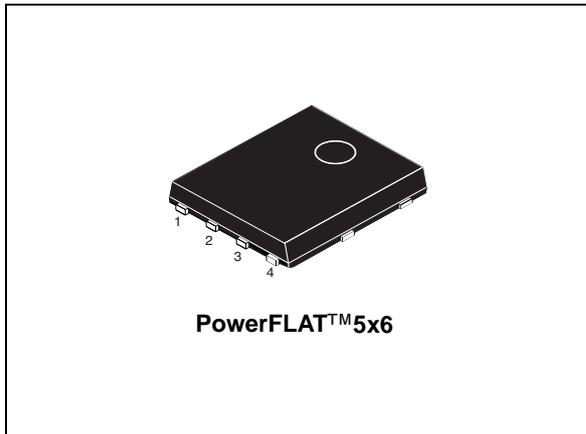


## Automotive-grade N-channel 100 V, 0.008 $\Omega$ typ., 16 A STripFET™ F7 Power MOSFET in a PowerFLAT™ 5x6 package

Datasheet - production data

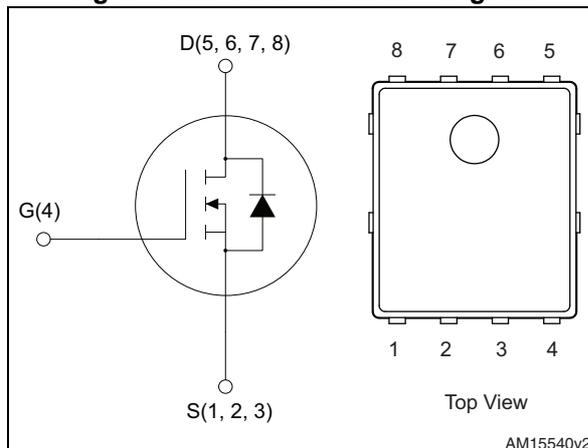


### Features

Order code	$V_{DS}$	$R_{DS(on)max}$	$I_D$	$P_{TOT}$
STL92N10F7AG	100 V	0.0095 $\Omega$	16 A	5 W

- Designed for automotive applications and AEC-Q101 qualified
- Among the lowest  $R_{DS(on)}$  on the market
- Excellent figure of merit (FoM)
- Low  $C_{rSS}/C_{iSS}$  ratio for EMI immunity
- High avalanche ruggedness
- Wettable flank package

**Figure 1. Internal schematic diagram**



### Applications

- Switching applications

### Description

This N-channel Power MOSFET utilizes STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

**Table 1. Device summary**

Order code	Marking	Package	Packaging
STL92N10F7AG	92N10F7	PowerFLAT™ 5x6	Tape and reel

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	100	V
$V_{GS}$	Gate-source voltage	$\pm 20$	V
$I_D^{(1)}$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	70	A
$I_D^{(1)}$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	50	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 25\text{ }^\circ\text{C}$	16	A
$I_D^{(2)}$	Drain current (continuous) at $T_{pcb} = 100\text{ }^\circ\text{C}$	11	A
$I_{DM}^{(2)(3)}$	Drain current (pulsed)	64	A
$P_{TOT}^{(1)}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	100	W
$P_{TOT}^{(2)}$	Total dissipation at $T_{pcb} = 25\text{ }^\circ\text{C}$	5	W
$T_{stg}$	Storage temperature	-55 to 175 °C	°C
$T_j$	Operating junction temperature		

1. This value is rated according to  $R_{thj-c}$
2. This value is rated according to  $R_{thj-pcb}$
3. Pulse width limited by safe operating area.

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb max	31	°C/W
$R_{thj-case}$	Thermal resistance junction-case max	1.5	°C/W

1. When mounted on FR-4 board of 1 inch<sup>2</sup>, 2 oz Cu.

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 4. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 250\ \mu\text{A}$ , $V_{GS} = 0$	100			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 100\ \text{V}$			1	$\mu\text{A}$
		$V_{DS} = 100\ \text{V}$ , $T_C = 125\text{ °C}$			100	$\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20\ \text{V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\ \mu\text{A}$	2.5	3.5	4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\ \text{V}$ , $I_D = 8\ \text{A}$		0.008	0.0095	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 50\ \text{V}$ , $f = 1\ \text{MHz}$ , $V_{GS} = 0$	-	3100	-	pF
$C_{oss}$	Output capacitance		-	700	-	pF
$C_{riss}$	Reverse transfer capacitance		-	45	-	pF
$Q_g$	Total gate charge	$V_{DD} = 50\ \text{V}$ , $I_D = 16\ \text{A}$ , $V_{GS} = 10\ \text{V}$ (see <a href="#">Figure 14</a> )	-	45	-	nC
$Q_{gs}$	Gate-source charge		-	18	-	nC
$Q_{gd}$	Gate-drain charge		-	13	-	nC

**Table 6. Switching times**

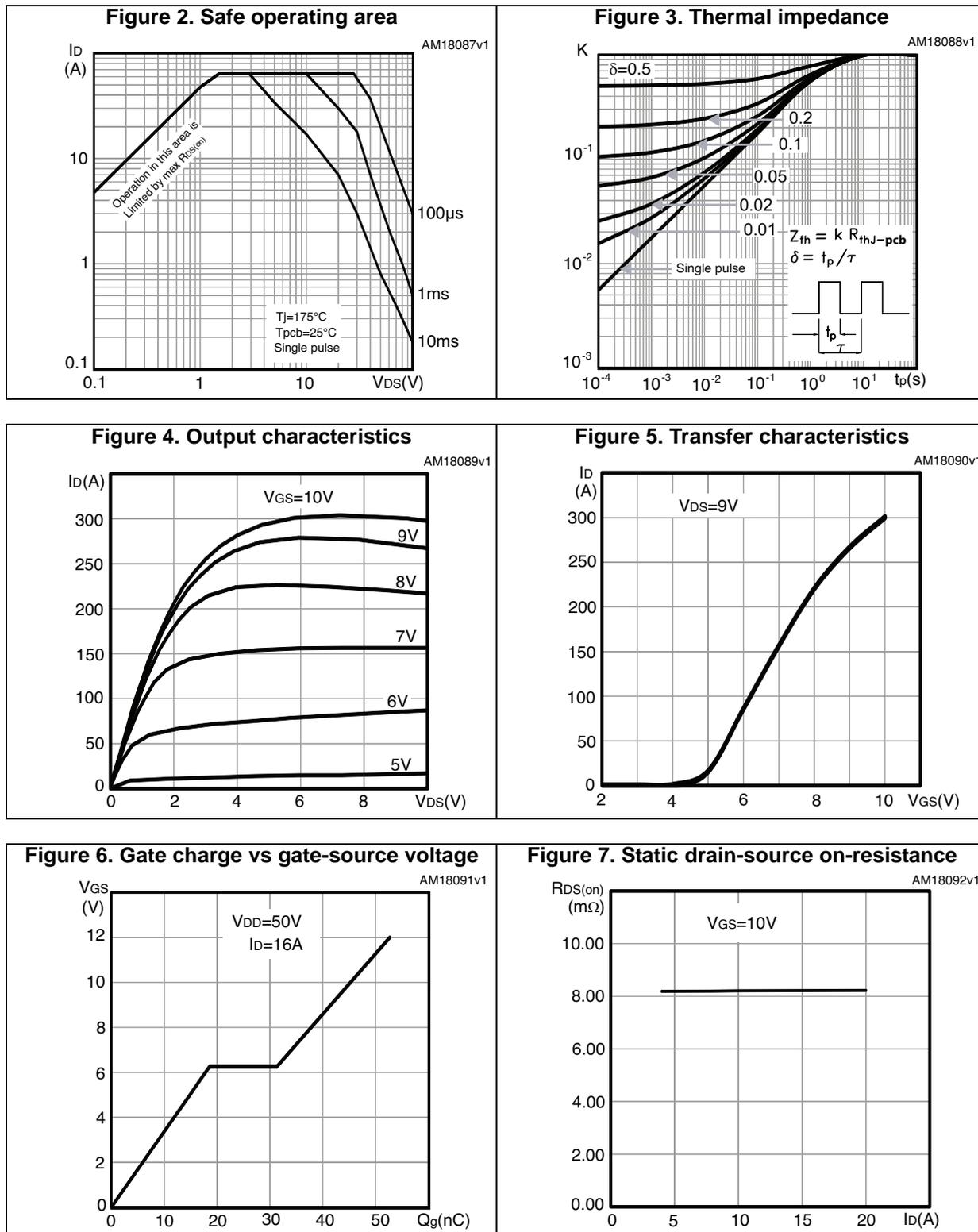
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 50\ \text{V}$ , $I_D = 8\ \text{A}$ , $R_G = 4.7\ \Omega$ , $V_{GS} = 10\ \text{V}$ (see <a href="#">Figure 15</a> and <a href="#">Figure 18</a> )	-	19	-	ns
$t_r$	Rise time		-	32	-	ns
$t_{d(off)}$	Turn-off delay time		-	36	-	ns
$t_f$	Fall time		-	13	-	ns

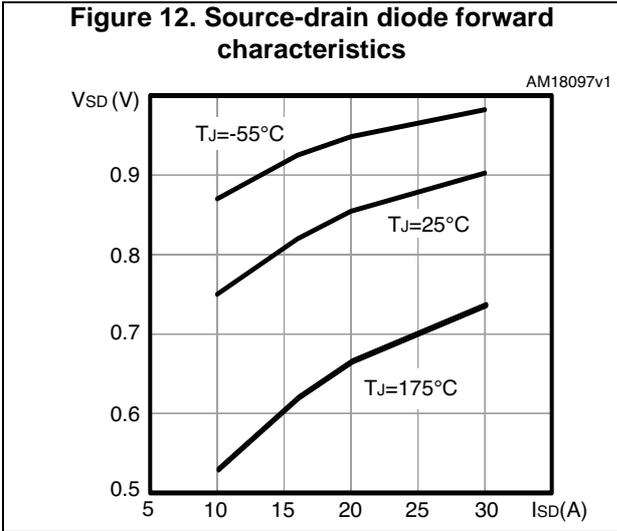
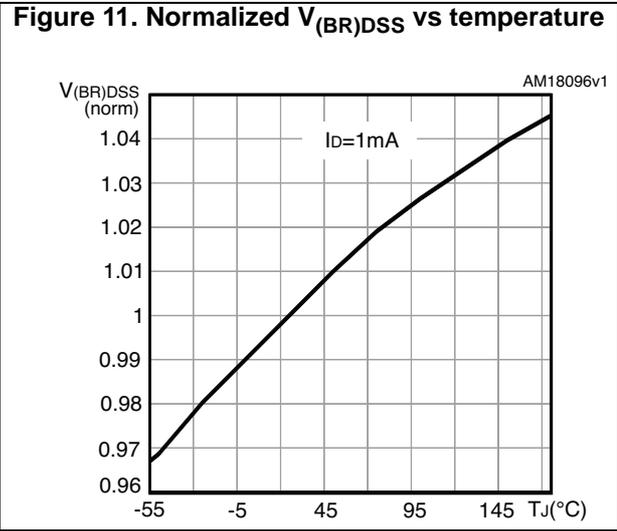
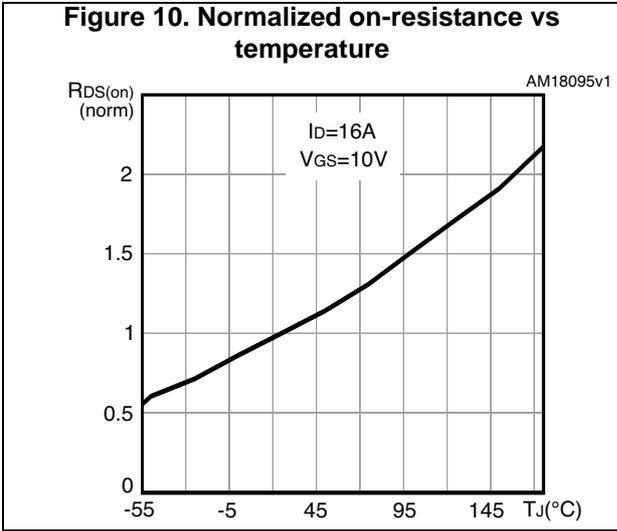
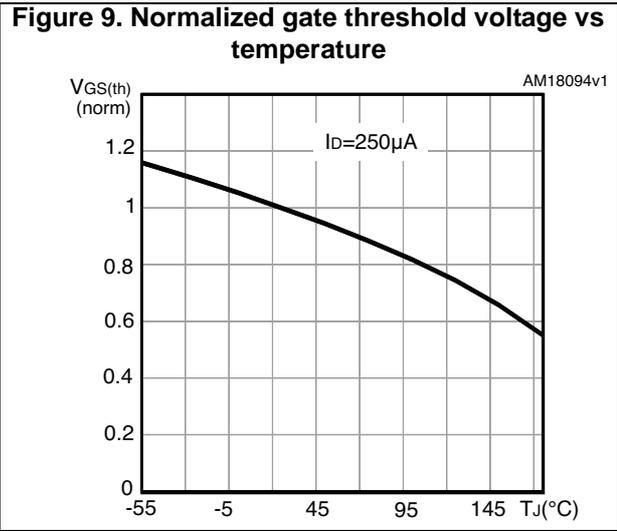
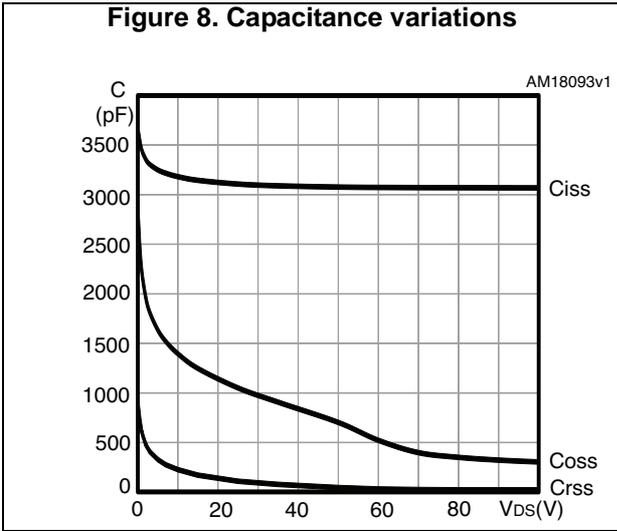
Table 7. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		16	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		64	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 16\text{ A}$ , $V_{GS} = 0$	-		1.1	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 16\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$	-	70		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 80\text{ V}$ , $T_j = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 18</a> )	-	125		nC
$I_{RRM}$	Reverse recovery current		-	3.6		A

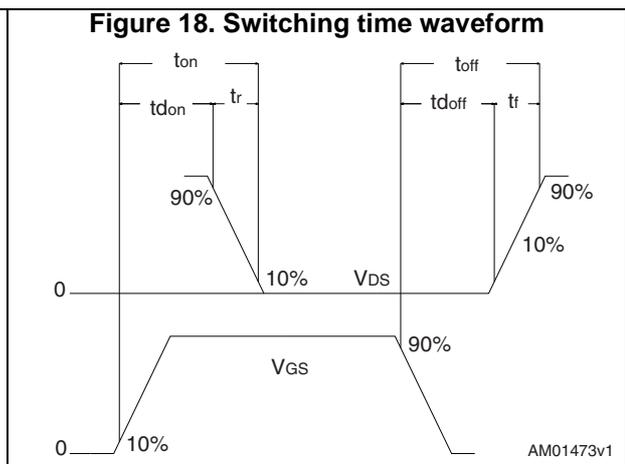
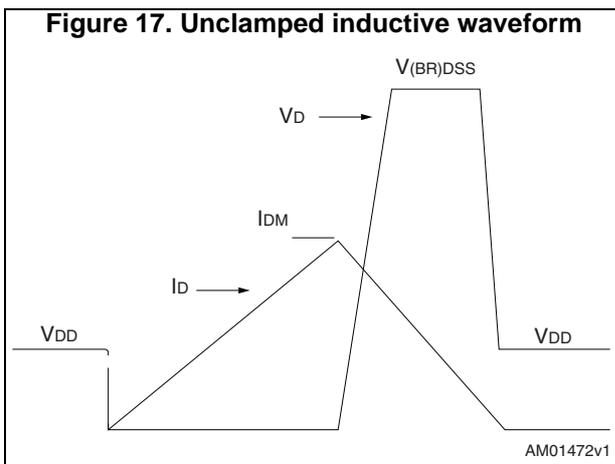
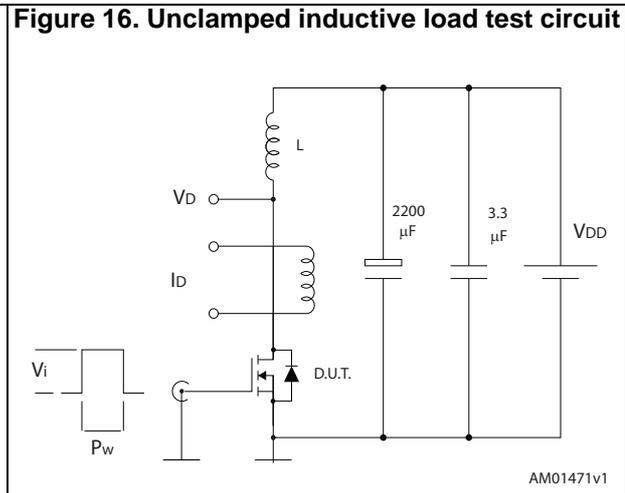
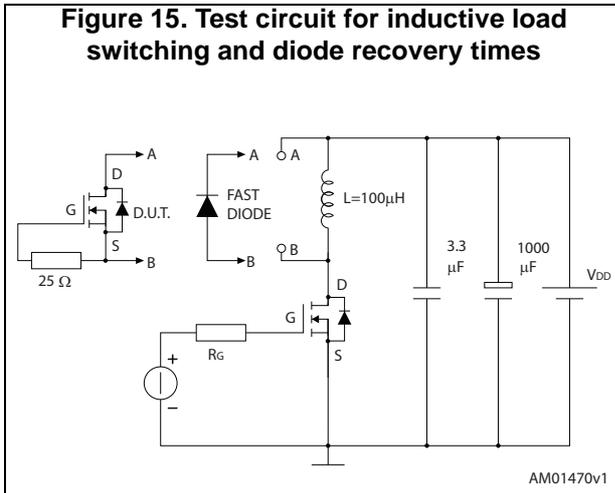
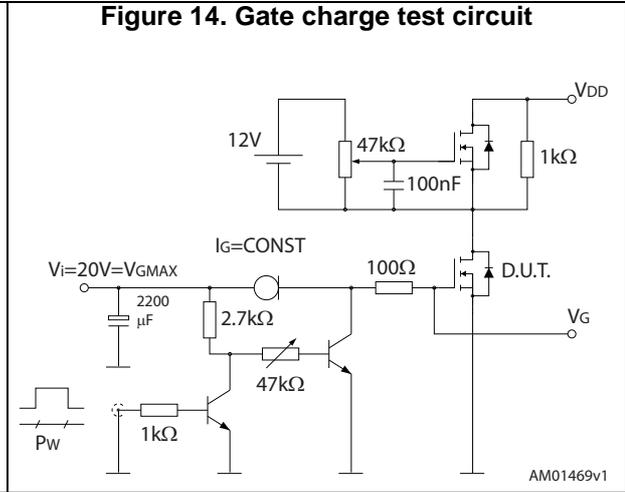
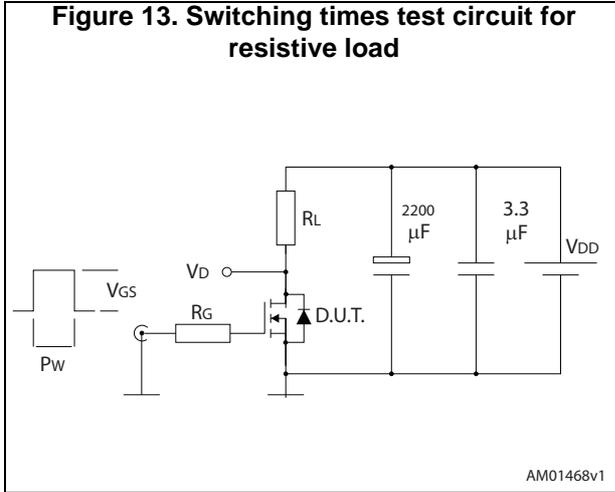
1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)





### 3 Test circuits



## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

### 4.1 PowerFLAT™ 5x6 WF type R package information

Figure 19. PowerFLAT™ 5x6 WF type R package outline

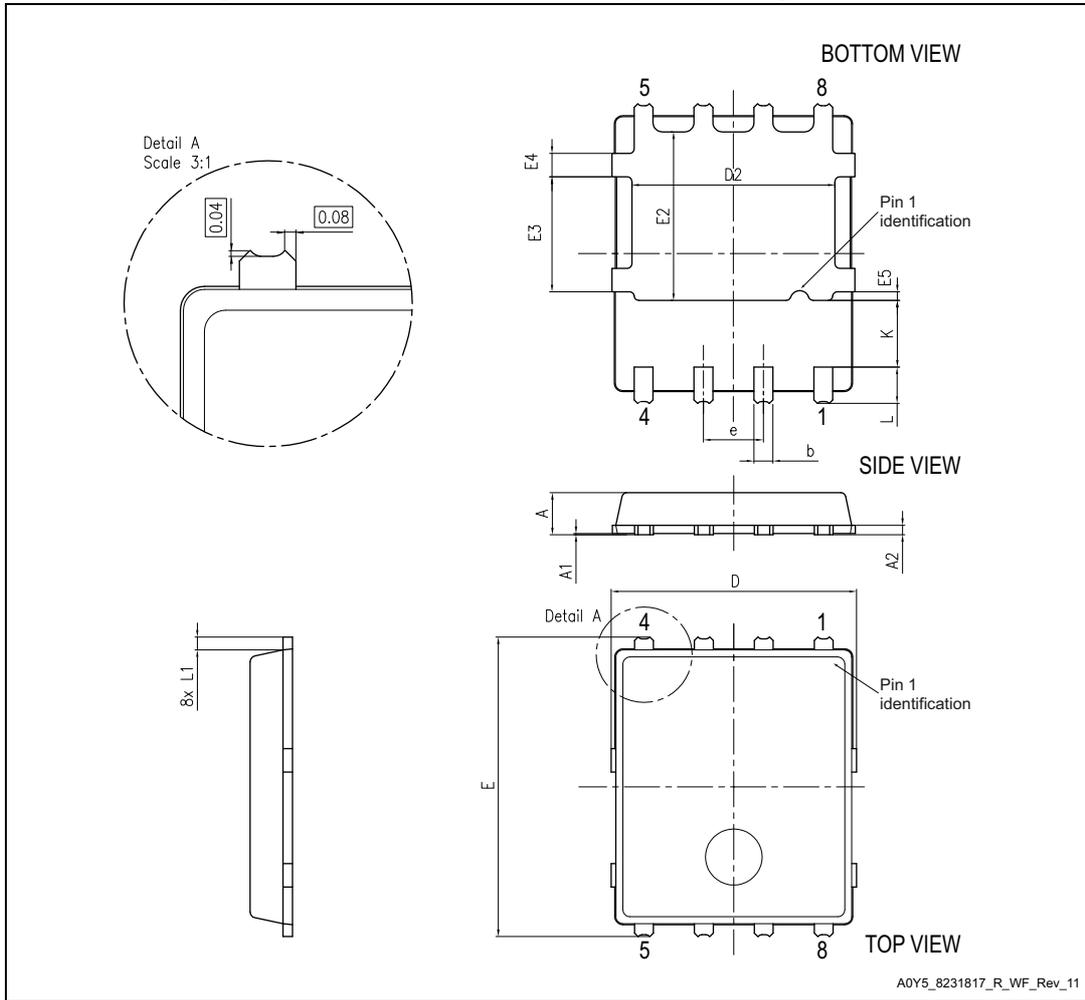
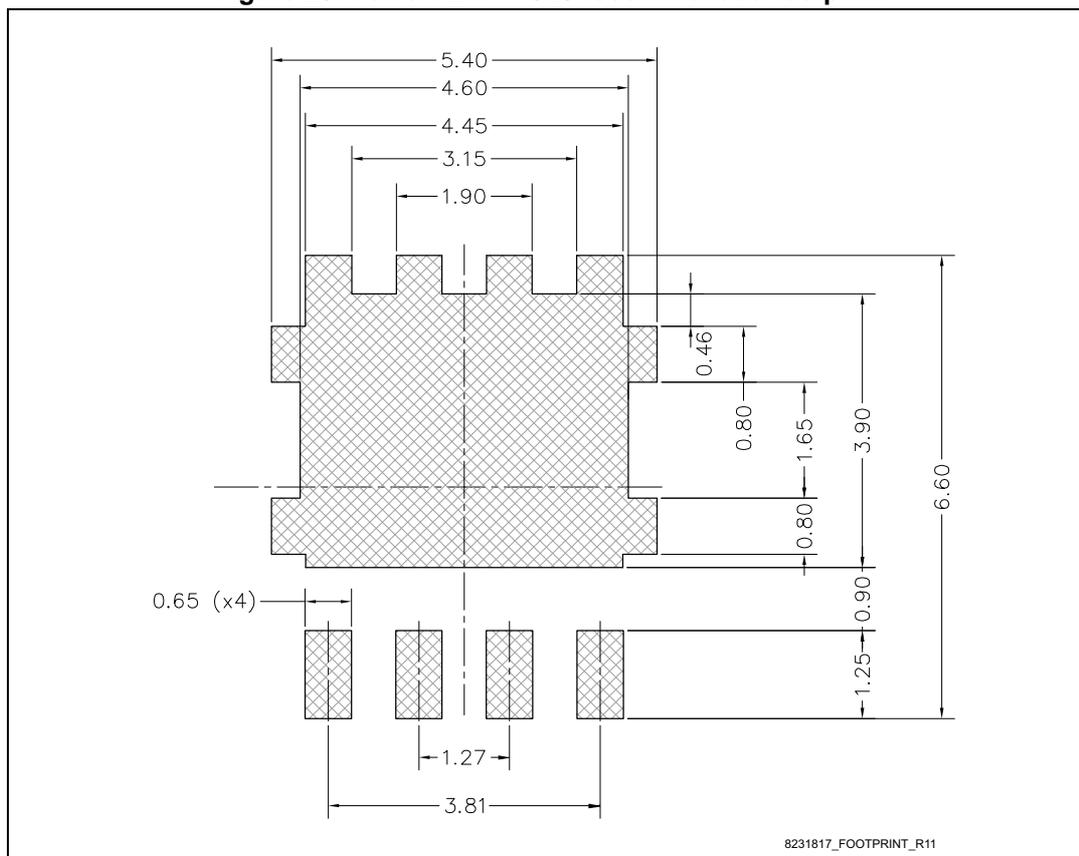


Table 8. PowerFLAT™ 5x6 WF type R mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.80		1.00
A1	0.02		0.05
A2		0.25	
b	0.30		0.50
D	5.00	5.20	5.40
E	6.20	6.40	6.60
D2	4.15		4.45
E2	3.50		3.70
e		1.27	
L	0.70		0.90
L1		0.275	
K	1.275		1.575
E3	2.35		2.55
E4	0.40		0.60
E5	0.08		0.28

Figure 20. PowerFLAT™ 5x6 recommended footprint



## 4.2 PowerFLAT™ 5x6 packing information

Figure 21. PowerFLAT™ 5x6 type WF tape<sup>(a)</sup>

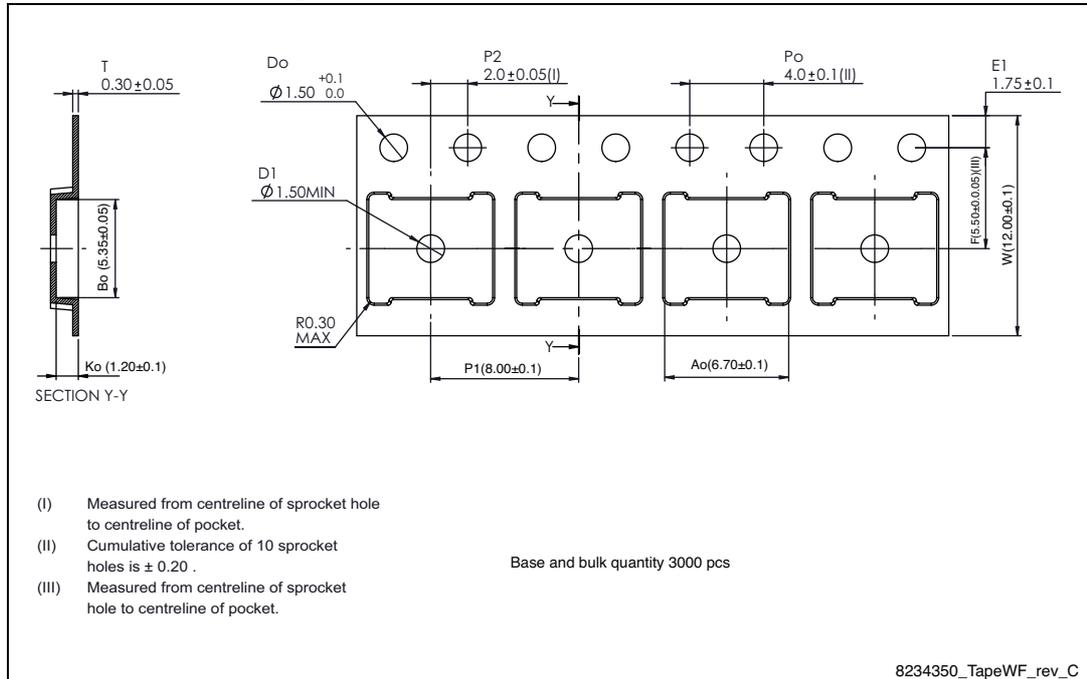
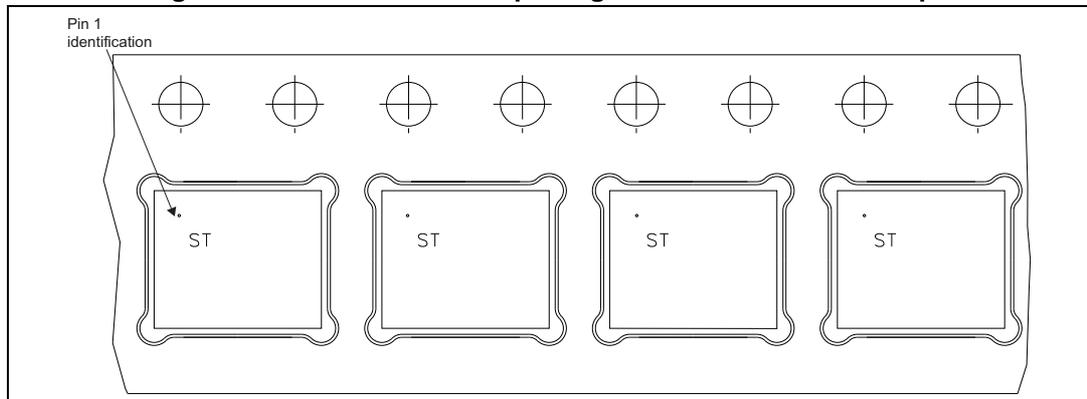
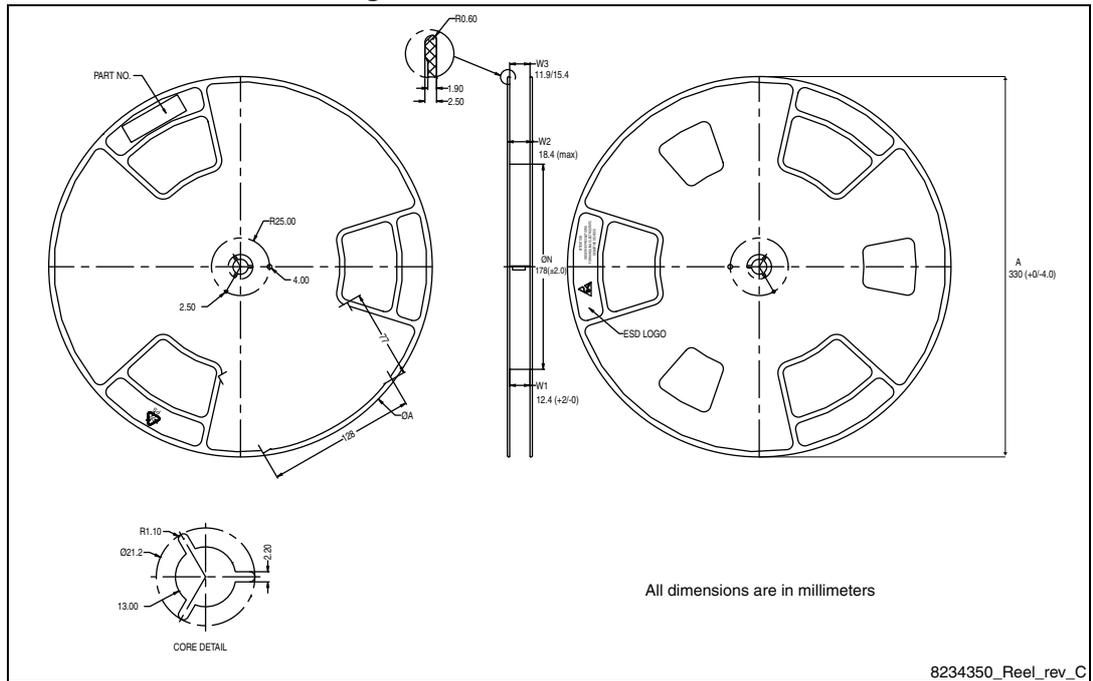


Figure 22. PowerFLAT™ 5x6 package orientation in carrier tape



a. All dimensions are in millimeters.

Figure 23. PowerFLAT™ 5x6 reel



## 5 Revision history

Table 9. Document revision history

Date	Revision	Changes
16-Oct-2014	1	First release.
12-Oct-2015	2	Updated: <a href="#">Section 4.1: PowerFLAT™ 5x6 WF type R package information</a> Datasheet promoted from preliminary data to production data Minor text changes

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