



N-Channel 30-V (D-S) MOSFET

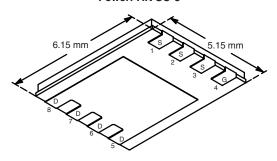
PRODUCT SUMMARY					
V _{DS} (V)	$R_{DS(on)}(\Omega)$	Ω) $I_D(A)^a$ $Q_g(T_S)$			
30	0.003 at V _{GS} = 10 V	40	54 nC		
	0.0035 at V _{GS} = 4.5 V	40	54 HC		

FEATURES

- · Halogen-free available
- TrenchFET[®] Power MOSFET
- PWM Optimized
- New Low Thermal Resistance PowerPAK[®]
 Package with Low 1.07 mm Profile
- 100 % R_q Tested

RoHS

PowerPAK SO-8



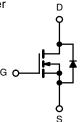
Bottom View

Ordering Information: Si7380ADP-T1-E3 (Lead (Pb)-free)

Si7380ADP-T1-GE3 (Lead (Pb)-free and Halogen-free)

APPLICATIONS

- DC/DC Converters
 - Low-Side MOSFET in Synchronous Buck in Desktops
- Secondary Synchronous Rectifier



N-Channel MOSFET

Parameter	Symbol	Limit	Unit		
Drain-Source Voltage		V _{DS}	30	V	
Gate-Source Voltage		V _{GS} ± 12		v	
	T _C = 25 °C		40		
Continuous Drain Current (T _{.I} = 150 °C)	T _C = 70 °C	1_	32		
Continuous Diain Current (1) = 130 C)	T _A = 25 °C	I _D	31 ^{b, c}		
	T _A = 70 °C		25 ^{b, c}	A	
Pulsed Drain Current		I _{DM}	70		
Continuous Source-Drain Diode Current	T _C = 25 °C	l _a	40		
Continuous Source-Drain Diode Current	T _A = 25 °C	I _S	4.9 ^{b, c}		
	T _C = 25 °C		83		
Maximum Power Dissipation	T _C = 70 °C	P _D	53	w	
waximum rowei Dissipation	T _A = 25 °C	' D	5.4 ^{b, c}	VV	
	T _A = 70 °C		3.4 ^{b, c}		
Operating Junction and Storage Temperature R	T _J , T _{stg}	- 55 to 150	°C		
Soldering Recommendations (Peak Temperatur		260			

THERMAL RESISTANCE RATINGS						
Parameter		Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^{b, f}	t ≤ 10 s	R_{thJA}	18	23	°C/W	
Maximum Junction-to-Case (Drain)	Steady State	R_{thJC}	1.0	1.5	- O/ VV	

Notes:

- a. Based on T_C = 25 °C.
- b. Surface Mounted on 1" x 1" FR4 board.
- c. t = 10 s.
- d. See Solder Profile (http://www.vishay.com/ppg?73257). The PowerPAK SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection.
- e. Rework Conditions: manual soldering with a soldering iron is not recommended for leadless components.
- f. Maximum under Steady State conditions is 65 °C/W.

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Parameter	Symbol	Test Conditions	Min.	Тур.	Max.	Unit	
Static	-				L		
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0 \text{ V}, I_D = 250 \mu\text{A}$	30			V	
V _{DS} Temperature Coefficient	$\Delta V_{DS}/T_{J}$	L = 250 uA		37		mV/°C	
V _{GS(th)} Temperature Coefficient	$\Delta V_{GS(th)}/T_J$	$I_{D} = 250 \mu A$		4.3			
Gate-Source Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}, I_D = 250 \mu A$	0.6		1.6	V	
Gate-Source Leakage	I _{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 12 \text{ V}$			± 100	nA	
Zana Oata Wallana Busin Oama i		$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}$	1		1		
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 30 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 ^{\circ}\text{C}$			10	- μΑ	
On-State Drain Current ^a	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 10 \text{ V}$	30			Α	
Drain-Source On-State Resistance ^a		$V_{GS} = 10 \text{ V}, I_D = 20 \text{ A}$		0.0024	0.003		
	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, I_D = 20 \text{ A}$		0.0027	0.0035	Ω	
Forward Transconductance ^a	9 _{fs}	V _{DS} = 15 V, I _D = 20 A		150		S	
Dynamic ^b					L		
Input Capacitance	C _{iss}			7785		pF	
Output Capacitance	C _{oss}	$V_{DS} = 15 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$		780			
Reverse Transfer Capacitance	C _{rss}			335			
Tatal Oats Obarra	Qg	V _{DS} = 15 V, V _{GS} = 10 V, I _D = 15 A		122	185	nC	
Total Gate Charge				54	85		
Gate-Source Charge	Q_{gs}	$V_{DS} = 15 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 15 \text{ A}$		14.5			
Gate-Drain Charge	Q_{gd}			8			
Gate Resistance	R_g	f = 1 MHz	0.5	1.0	1.5	Ω	
Turn-On Delay Time	t _{d(on)}			17	25		
Rise Time	t _r	V_{DD} = 15 V, R_L = 15 Ω		13	20	ns	
Turn-Off Delay Time	t _{d(off)}	$I_D\cong$ 1 A, V_{GEN} = 10 V, R_g = 6 Ω		155	235		
Fall Time	t _f			35	55		
Drain-Source Body Diode Characterist	ics						
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C			40	A	
Pulse Diode Forward Current ^a	I _{SM}				70	^	
Body Diode Voltage	V_{SD}	I _S = 5 A		0.68	1.1	V	
Body Diode Reverse Recovery Time	t _{rr}			45	70	ns	
Body Diode Reverse Recovery Charge	Q _{rr}	I _F = 3 A, di/dt = 100 A/μs, T _J = 25 °C		52	80	nC	
Reverse Recovery Fall Time	t _a	$I_F = 3 \text{ A}$, $I_{I} = 23 \text{ C}$		22		ns	
Reverse Recovery Rise Time	t _b			23			

Notes:

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

a. Pulse test; pulse width $\leq 300~\mu s,$ duty cycle $\leq 2~\%.$

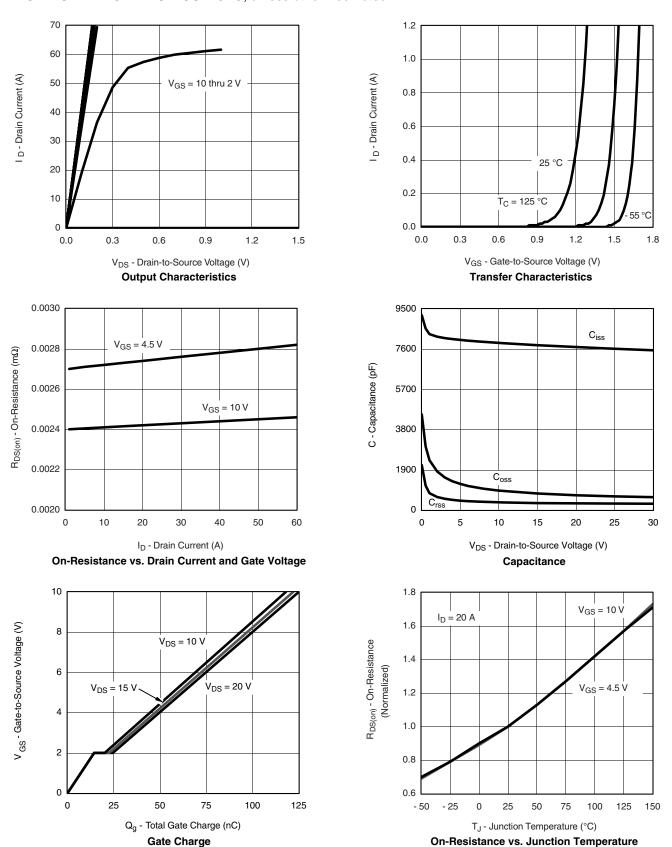
b. Guaranteed by design, not subject to production testing.





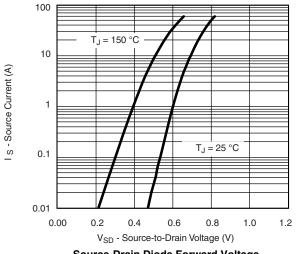


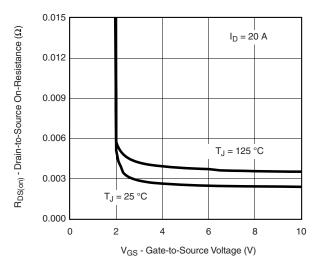
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



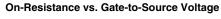
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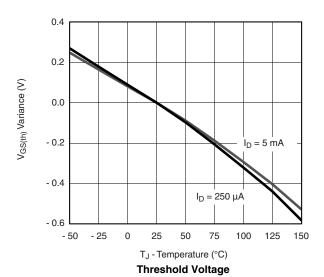
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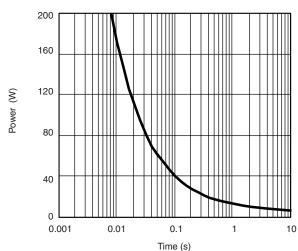




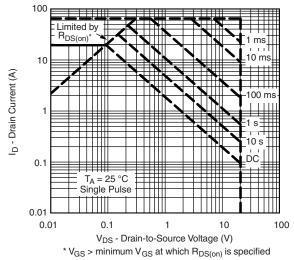
Source-Drain Diode Forward Voltage







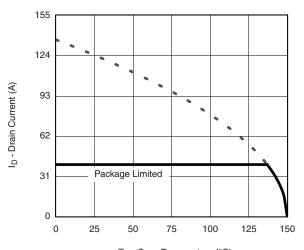
Single Pulse Power, Junction-to-Ambient



Safe Operating Area, Junction-to-Ambient

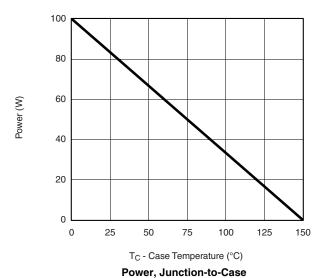


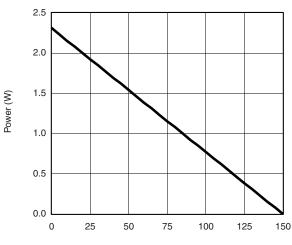
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T_C - Case Temperature (°C)

Current Derating*





T_C - Case Temperature (°C)

Power, Junction-to-Ambient

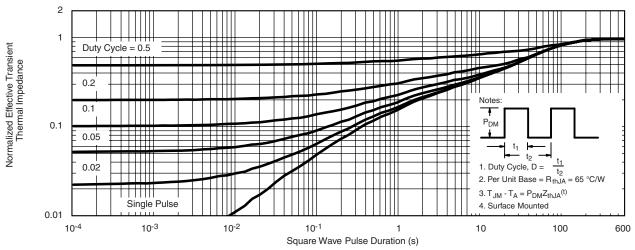
Document Number: 73408 S-80439-Rev. B, 03-Mar-08

^{*} The power dissipation P_D is based on $T_{J(max)} = 175$ °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

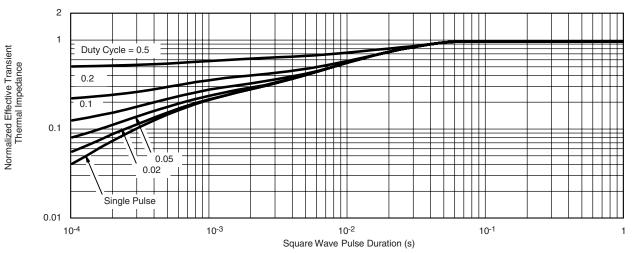
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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

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