

CDK2308

Dual, 20/40/65/80MSPS, 10-bit Analog-to-Digital Converters

CDK2308 Dual, 20/40/65/80MSPS, 10-bit Analog-to-Digital Converters Rev 2B

FEATURES

- 10-bit resolution
- 20/40/65/80MSPS maximum sampling rate
- Ultra-low power dissipation: 24/43/65/78mW
- 61.6dB SNR at 80MSPS and 8MHz F_{IN}
- Internal reference circuitry
- 1.8V core supply voltage
- 1.7V – 3.6V I/O supply voltage
- Parallel CMOS output
- 64-pin QFN package
- Dual channel
- Pin compatible with CDK2307

APPLICATIONS

- Medical Imaging
- Portable Test Equipment
- Digital Oscilloscopes
- IF Communication

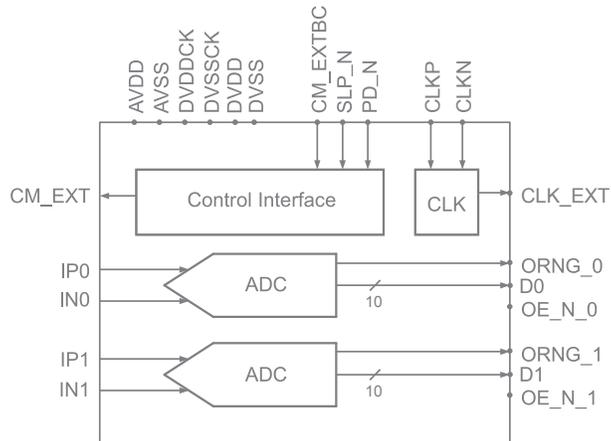
General Description

The CDK2308 is a high performance, low power dual Analog-to-Digital Converters (ADC). The ADC employs internal reference circuitry, a CMOS control interface and CMOS output data, and is based on a proprietary structure. Digital error correction is employed to ensure no missing codes in the complete full scale range.

Several idle modes with fast startup times exist. Each channel can independently be powered down and the entire chip can either be put in Standby Mode or Power Down mode. The different modes are optimized to allow the user to select the mode resulting in the smallest possible energy consumption during idle mode and startup.

The CDK2308 has a highly linear THA optimized for frequencies up to Nyquist. The differential clock interface is optimized for low jitter clock sources and supports LVDS, LVPECL, sine wave and CMOS clock inputs.

Functional Block Diagram



Ordering Information

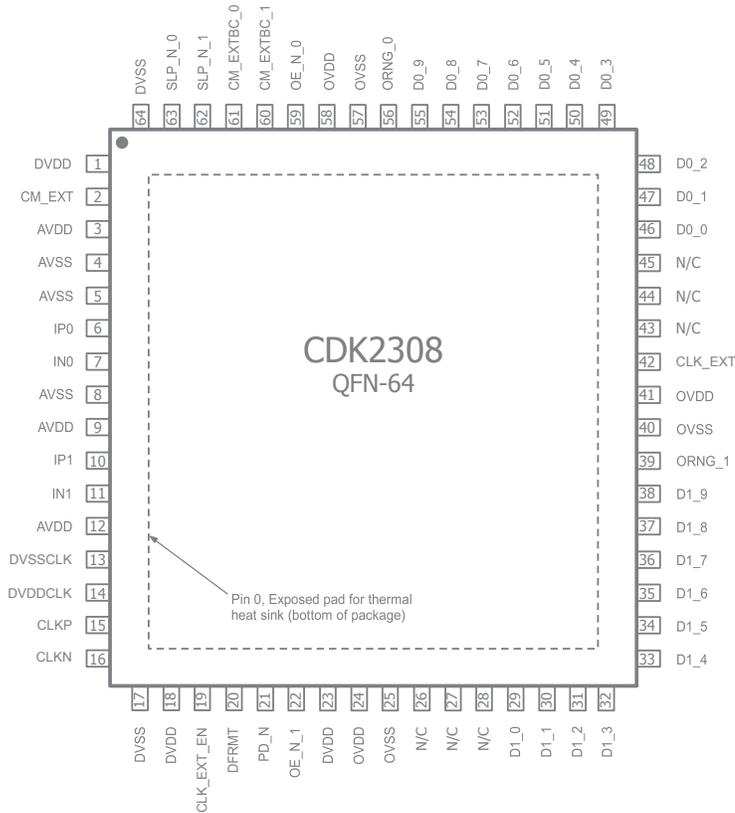
| Part Number | Speed | Package | Pb-Free | RoHS Compliant | Operating Temperature Range | Packaging Method |
|---------------|--------|---------|---------|----------------|-----------------------------|------------------|
| CDK2308AILP64 | 20MSPS | QFN-64 | Yes | Yes | -40°C to +85°C | Tray |
| CDK2308BILP64 | 40MSPS | QFN-64 | Yes | Yes | -40°C to +85°C | Tray |
| CDK2308CILP64 | 65MSPS | QFN-64 | Yes | Yes | -40°C to +85°C | Tray |
| CDK2308DILP64 | 80MSPS | QFN-64 | Yes | Yes | -40°C to +85°C | Tray |

Moisture sensitivity level for all parts is MSL-2A.



Pin Configuration

QFN-64, TQFP-64



Pin Assignments

| Pin No. | Pin Name | Description |
|------------|----------------------|--|
| 1, 18, 23 | DV _{DD} | Digital and I/O-ring pre driver supply voltage, 1.8V |
| 2 | CM_EXT | Common Mode voltage output |
| 3, 9, 12 | AV _{DD} | Analog supply voltage, 1.8V |
| 4, 5, 8 | AV _{SS} | Analog ground |
| 6, 7 | IPO, IN0 | Analog input Channel 0 (non-inverting, inverting) |
| 10, 11 | IP1, IN1 | Analog input Channel 1 (non-inverting, inverting) |
| 13 | DV _{SS} CLK | Clock circuitry ground |
| 14 | DV _{DD} CLK | Clock circuitry supply voltage, 1.8V |
| 15 | CLKP | Clock input, non-inverting (Format: LVDS, PECL, CMOS/TTL, Sine Wave) |
| 16 | CLKN | Clock input, inverting. For CMOS input on CLKP, connect CLKN to ground |
| 17, 64 | DV _{SS} | Digital circuitry ground |
| 19 | CLK_EXT_EN | CLK_EXT signal enabled when low (zero). Tristate when high. |
| 20 | DFRMT | Data format selection. 0: Offset Binary, 1: Two's Complement |
| 21 | PD_N | Full chip Power Down mode when Low. All digital outputs reset to zero. After chip power up, always apply Power Down mode before using Active mode to reset chip. |
| 22 | OE_N_1 | Output Enable Channel 0. Tristate when high |
| 24, 41, 58 | OV _{DD} | I/O ring post-driver supply voltage. Voltage range 1.7V to 3.6V. |
| 25, 40, 57 | OV _{SS} | Ground for I/O ring |



Pin Assignments (Continued)

| Pin No. | Pin Name | Description |
|---------|---------------------------|--|
| 26 | NC | No Connect |
| 27 | NC | No Connect |
| 28 | NC | No Connect |
| 29 | D1_0 | Output Data Channel 1 (LSB) |
| 30 | D1_1 | Output Data Channel 1 |
| 31 | D1_2 | Output Data Channel 1 |
| 32 | D1_3 | Output Data Channel 1 |
| 33 | D1_4 | Output Data Channel 1 |
| 34 | D1_5 | Output Data Channel 1 |
| 35 | D1_6 | Output Data Channel 1 |
| 36 | D1_7 | Output Data Channel 1 |
| 37 | D1_8 | Output Data Channel 1 |
| 38 | D1_9 | Output Data Channel 1 (MSB) |
| 39 | ORNG_1 | Out of Range flag Channel 1. High when input signal is out of range |
| 42 | CLK_EXT | Output clock signal for data synchronization. CMOS levels. |
| 43 | NC | No Connect |
| 44 | NC | No Connect |
| 45 | NC | No Connect |
| 46 | D0_0 | Output Data Channel 0 |
| 47 | D0_1 | Output Data Channel 0 |
| 48 | D0_2 | Output Data Channel 0 |
| 49 | D0_3 | Output Data Channel 0 |
| 50 | D0_4 | Output Data Channel 0 |
| 51 | D0_5 | Output Data Channel 0 |
| 52 | D0_6 | Output Data Channel 0 |
| 53 | D0_7 | Output Data Channel 0 |
| 54 | D0_8 | Output Data Channel 0 |
| 55 | D0_9 | Output Data Channel 0 (MSB) |
| 56 | ORNG_0 | Out of Range flag Channel 0. High when input signal is out of range. |
| 59 | OE_N_0 | Output Enable Channel 0. Tristate when low. |
| 60, 61 | CM_EXTBC_1, CM_EXTBC_0 | Bias control bits for the buffer driving pin CM_EXT 00: Off 01: 50uA 10: 500uA 11: 1mA |
| 62, 63 | SLP_N_1, SLP_N_0 | Sleep Mode 00: Sleep Mode 01: Channel 0 active 10: Channel 1 active 11: Both channels active |



Absolute Maximum Ratings

The safety of the device is not guaranteed when it is operated above the “Absolute Maximum Ratings”. The device should not be operated at these “absolute” limits. Adhere to the “Recommended Operating Conditions” for proper device function. The information contained in the Electrical Characteristics tables and Typical Performance plots reflect the operating conditions noted on the tables and plots.

| Parameter | Min | Max | Unit |
|---|------|------|------|
| AV _{DD} , AV _{SS} | -0.3 | +2.3 | V |
| DV _{DD} , DV _{SS} | -0.3 | +2.3 | V |
| AV _{SS} , DV _{SSCK} , DV _{SS} , OV _{SS} | -0.3 | +0.3 | V |
| OV _{DD} , OV _{SS} | -0.3 | +3.9 | V |
| CKP, CKN, DV _{SSCK} | -0.3 | +3.9 | V |
| Analog inputs and outputs (IP _x , IN _x , AV _{SS}) | -0.3 | +2.3 | V |
| Digital inputs | -0.3 | +3.9 | V |
| Digital outputs | -0.3 | +3.9 | V |

Reliability Information

| Parameter | Min | Typ | Max | Unit |
|-----------------------------------|-----------|-----|------|------|
| Storage Temperature Range | -60 | | +150 | °C |
| Lead Temperature (Soldering, 10s) | J-STD-020 | | | |

ESD Protection

| Product | QFN-64 | TQFP-64 |
|------------------------|--------|---------|
| Human Body Model (HBM) | 2kV | 2kV |

Recommended Operating Conditions

| Parameter | Min | Typ | Max | Unit |
|-----------------------------|-----|-----|-----|------|
| Operating Temperature Range | -40 | | +85 | °C |



Electrical Characteristics

(AVDD = 1.8V, DVDD = 1.8V, DVDDCLK = 1.8V, OVDD = 2.5V, 50MSPS clock, 50% clock duty cycle, -1dBFS 8MHz input signal, 13-bit output, unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|-------------------------------------|----------------------------|---|----------------------|----------------------|----------------------|-----------------|
| DC Accuracy | | | | | | |
| | No Missing Codes | | Guaranteed | | | |
| | Offset Error | Midscale offset | | 1 | | LSB |
| | Gain Error | Full scale range deviation from typical | -6 | | 6 | %FS |
| | Gain Matching | Gain matching between channels | | ±0.05 | | %FS |
| DNL | Differential Non-Linearity | 12-bit level | | ±0.15 | | LSB |
| ILE | Integral Non-Linearity | 12-bit level | | ±0.2 | | LSB |
| V _{CMO} | Common Mode Voltage Output | | | V _{AVDD} /2 | | V |
| Analog Input | | | | | | |
| V _{CMi} | Input Common Mode | Analog input common mode voltage | V _{CM} -0.1 | | V _{CM} +0.2 | V |
| V _{FSR} | Full Scale Range | Differential input voltage range | | 2 | | V _{pp} |
| | Input Capacitance | Differential input capacitance | | 2 | | pF |
| | Bandwidth | Input bandwidth, full power | 500 | | | MHz |
| Power Supply | | | | | | |
| AV _{DD} , DV _{DD} | Core Supply Voltage | Supply voltage to all 1.8V domain pins. See Pin Configuration and Description | 1.7 | 1.8 | 2.0 | V |
| OV _{DD} | I/O Supply Voltage | Output driver supply voltage (OVDD). Must be higher than or equal to Core Supply Voltage (VOVDD ≥ VD _{VDD}) | 1.7 | 2.5 | 3.6 | V |



Electrical Characteristics - CDK2308A

(AVDD = 1.8V, DVDD = 1.8V, DVDDCLK = 1.8V, OVDD = 2.5V, 20MSPS clock, 50% clock duty cycle, -1dBFS 8MHz input signal, 13-bit output, unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|--------------|--------------------------------------|--|-----|------|-----|---------------|
| Performance | | | | | | |
| SNR | Signal to Noise Ratio | $F_{IN} = 2\text{MHz}$ | | 61.7 | | dBFS |
| | | $F_{IN} = 8\text{MHz}$ | 60 | 61.6 | | dBFS |
| | | $F_{IN} \approx FS/2$ | | 61.6 | | dBFS |
| | | $F_{IN} = 20\text{MHz}$ | | 61.6 | | dBFS |
| SNDR | Signal to Noise and Distortion Ratio | $F_{IN} = 2\text{MHz}$ | | 61.7 | | dBFS |
| | | $F_{IN} = 8\text{MHz}$ | 60 | 61.6 | | dBFS |
| | | $F_{IN} \approx FS/2$ | | 60.5 | | dBFS |
| | | $F_{IN} = 20\text{MHz}$ | | 61.6 | | dBFS |
| SFDR | Spurious Free Dynamic Range | $F_{IN} = 2\text{MHz}$ | | 80 | | dBc |
| | | $F_{IN} = 8\text{MHz}$ | 70 | 81 | | dBc |
| | | $F_{IN} \approx FS/2$ | | 70 | | dBc |
| | | $F_{IN} = 20\text{MHz}$ | | 80 | | dBc |
| HD2 | Second order Harmonic Distortion | $F_{IN} = 2\text{MHz}$ | | -90 | | dBc |
| | | $F_{IN} = 8\text{MHz}$ | -80 | -90 | | dBc |
| | | $F_{IN} \approx FS/2$ | | -90 | | dBc |
| | | $F_{IN} = 20\text{MHz}$ | | -90 | | dBc |
| HD3 | Third order Harmonic Distortion | $F_{IN} = 2\text{MHz}$ | | -80 | | dBc |
| | | $F_{IN} = 8\text{MHz}$ | -70 | -81 | | dBc |
| | | $F_{IN} \approx FS/2$ | | -70 | | dBc |
| | | $F_{IN} = 20\text{MHz}$ | | -80 | | dBc |
| ENOB | Effective number of Bits | $F_{IN} = 2\text{MHz}$ | | 10 | | bits |
| | | $F_{IN} = 8\text{MHz}$ | 9.7 | 9.9 | | bits |
| | | $F_{IN} \approx FS/2$ | | 9.8 | | bits |
| | | $F_{IN} = 20\text{MHz}$ | | 9.9 | | bits |
| X_{TALK} | Crosstalk | Signal crosstalk between channels, $F_{IN1} = 8\text{MHz}$, $F_{IN0} = 9.9\text{MHz}$ | | -105 | | dBc |
| Power Supply | | | | | | |
| AI_{DD} | Analog Supply Current | | | 8.2 | | mA |
| DI_{DD} | Digital Supply Current | Digital core supply | | 1.7 | | mA |
| OI_{DD} | Output Driver Supply | 2.5V output driver supply, sine wave input, $F_{IN} = 1\text{MHz}$ | | 2.8 | | mA |
| | | 2.5V output driver supply, sine wave input, $F_{IN} = 1\text{MHz}$, CLK_EXT disabled | | 2.3 | | mA |
| | Analog Power Dissipation | | | 14.8 | | mW |
| | Digital Power Dissipation | $OV_{DD} = 2.5\text{V}$, 5pF load on output bits, $F_{IN} = 1\text{MHz}$, CLK_EXT disabled | | 8.8 | | mW |
| | Total Power Dissipation | $OV_{DD} = 2.5\text{V}$, 5pF load on output bits, $F_{IN} = 1\text{MHz}$, CLK_EXT disabled | | 23.6 | | mW |
| | Power Down Dissipation | | | 9.9 | | μW |
| | Sleep Mode 1 | Power Dissipation, Sleep mode one channel | | 15.2 | | mW |
| | Sleep Mode 2 | Power Dissipation, Sleep mode both channels | | 7.7 | | mW |
| Clock Inputs | | | | | | |
| | Max. Conversion Rate | | 20 | | | MSPS |
| | Min. Conversion Rate | | | | 15 | MSPS |



Electrical Characteristics - CDK2308B

(AVDD = 1.8V, DVDD = 1.8V, DVDDCLK = 1.8V, OVDD = 2.5V, 40MSPS clock, 50% clock duty cycle, -1dBFS 8MHz input signal, 13-bit output, unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|--------------|--------------------------------------|--|-----|------|-----|---------------|
| Performance | | | | | | |
| SNR | Signal to Noise Ratio | $F_{IN} = 2\text{MHz}$ | | 61.6 | | dBFS |
| | | $F_{IN} = 8\text{MHz}$ | 60 | 61.6 | | dBFS |
| | | $F_{IN} \approx FS/2$ | | 61.6 | | dBFS |
| | | $F_{IN} = 30\text{MHz}$ | | 61.5 | | dBFS |
| SNDR | Signal to Noise and Distortion Ratio | $F_{IN} = 2\text{MHz}$ | | 61.6 | | dBFS |
| | | $F_{IN} = 8\text{MHz}$ | 60 | 61.6 | | dBFS |
| | | $F_{IN} \approx FS/2$ | | 61.2 | | dBFS |
| | | $F_{IN} = 30\text{MHz}$ | | 61.4 | | dBFS |
| SFDR | Spurious Free Dynamic Range | $F_{IN} = 2\text{MHz}$ | | 80 | | dBc |
| | | $F_{IN} = 8\text{MHz}$ | 70 | 81 | | dBc |
| | | $F_{IN} \approx FS/2$ | | 72 | | dBc |
| | | $F_{IN} = 30\text{MHz}$ | | 80 | | dBc |
| HD2 | Second order Harmonic Distortion | $F_{IN} = 2\text{MHz}$ | | -90 | | dBc |
| | | $F_{IN} = 8\text{MHz}$ | -80 | -90 | | dBc |
| | | $F_{IN} \approx FS/2$ | | -85 | | dBc |
| | | $F_{IN} = 30\text{MHz}$ | | -85 | | dBc |
| HD3 | Third order Harmonic Distortion | $F_{IN} = 2\text{MHz}$ | | -80 | | dBc |
| | | $F_{IN} = 8\text{MHz}$ | -70 | -81 | | dBc |
| | | $F_{IN} \approx FS/2$ | | -72 | | dBc |
| | | $F_{IN} = 30\text{MHz}$ | | -80 | | dBc |
| ENOB | Effective number of Bits | $F_{IN} = 2\text{MHz}$ | | 9.9 | | bits |
| | | $F_{IN} = 8\text{MHz}$ | 9.7 | 9.9 | | bits |
| | | $F_{IN} \approx FS/2$ | | 9.9 | | bits |
| | | $F_{IN} = 30\text{MHz}$ | | 9.9 | | bits |
| X_{TALK} | Crosstalk | Signal crosstalk between channels, $F_{IN1} = 8\text{MHz}$, $F_{IN0} = 9.9\text{MHz}$ | | -100 | | dBc |
| Power Supply | | | | | | |
| AI_{DD} | Analog Supply Current | | | 14.4 | | mA |
| DI_{DD} | Digital Supply Current | Digital core supply | | 3.4 | | mA |
| OI_{DD} | Output Driver Supply | 2.5V output driver supply, sine wave input, $F_{IN} = 1\text{MHz}$ | | 5.1 | | mA |
| | | 2.5V output driver supply, sine wave input, $F_{IN} = 1\text{MHz}$, CLK_EXT disabled | | 4.2 | | mA |
| | Analog Power Dissipation | | | 25.9 | | mW |
| | Digital Power Dissipation | $OV_{DD} = 2.5\text{V}$, 5pF load on output bits, $F_{IN} = 1\text{MHz}$, CLK_EXT disabled | | 16.6 | | mW |
| | Total Power Dissipation | $OV_{DD} = 2.5\text{V}$, 5pF load on output bits, $F_{IN} = 1\text{MHz}$, CLK_EXT disabled | | 42.5 | | mW |
| | Power Down Dissipation | | | 9.7 | | μW |
| | Sleep Mode 1 | Power Dissipation, Sleep mode one channel | | 25.7 | | mW |
| | Sleep Mode 2 | Power Dissipation, Sleep mode both channels | | 11.3 | | mW |
| Clock Inputs | | | | | | |
| | Max. Conversion Rate | | 40 | | | MSPS |
| | Min. Conversion Rate | | | | 20 | MSPS |



Electrical Characteristics - CDK2308C

(AVDD = 1.8V, DVDD = 1.8V, DVDDCLK = 1.8V, OVDD=2.5V, 65MSPS clock, 50% clock duty cycle, -1dBFS 8MHz input signal, 13-bit output, unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|--------------|--------------------------------------|--|-----|------|-----|---------------|
| Performance | | | | | | |
| SNR | Signal to Noise Ratio | $F_{IN} = 8\text{MHz}$ | 60 | 61.6 | | dBFS |
| | | $F_{IN} = 20\text{MHz}$ | | 61.6 | | dBFS |
| | | $F_{IN} \approx FS/2$ | | 61.5 | | dBFS |
| | | $F_{IN} = 40\text{MHz}$ | | 61.3 | | dBFS |
| SNDR | Signal to Noise and Distortion Ratio | $F_{IN} = 8\text{MHz}$ | 60 | 61.6 | | dBFS |
| | | $F_{IN} = 20\text{MHz}$ | | 61.6 | | dBFS |
| | | $F_{IN} \approx FS/2$ | | 60.4 | | dBFS |
| | | $F_{IN} = 40\text{MHz}$ | | 61.1 | | dBFS |
| SFDR | Spurious Free Dynamic Range | $F_{IN} = 8\text{MHz}$ | 70 | 77 | | dBc |
| | | $F_{IN} = 20\text{MHz}$ | | 77 | | dBc |
| | | $F_{IN} \approx FS/2$ | | 70 | | dBc |
| | | $F_{IN} = 40\text{MHz}$ | | 75 | | dBc |
| HD2 | Second order Harmonic Distortion | $F_{IN} = 8\text{MHz}$ | -80 | -90 | | dBc |
| | | $F_{IN} = 20\text{MHz}$ | | -95 | | dBc |
| | | $F_{IN} \approx FS/2$ | | -85 | | dBc |
| | | $F_{IN} = 40\text{MHz}$ | | -90 | | dBc |
| HD3 | Third order Harmonic Distortion | $F_{IN} = 8\text{MHz}$ | -70 | -77 | | dBc |
| | | $F_{IN} = 20\text{MHz}$ | | -77 | | dBc |
| | | $F_{IN} \approx FS/2$ | | -70 | | dBc |
| | | $F_{IN} = 40\text{MHz}$ | | -75 | | dBc |
| ENOB | Effective number of Bits | $F_{IN} = 8\text{MHz}$ | 9.7 | 9.9 | | bits |
| | | $F_{IN} = 20\text{MHz}$ | | 9.9 | | bits |
| | | $F_{IN} \approx FS/2$ | | 9.7 | | bits |
| | | $F_{IN} = 40\text{MHz}$ | | 9.9 | | bits |
| X_{TALK} | Crosstalk | Signal crosstalk between channels, $F_{IN1} = 8\text{MHz}$, $F_{IN0} = 9.9\text{MHz}$ | | -97 | | dBc |
| Power Supply | | | | | | |
| AI_{DD} | Analog Supply Current | | | 22 | | mA |
| DI_{DD} | Digital Supply Current | Digital core supply | | 5.2 | | mA |
| OI_{DD} | Output Driver Supply | 2.5V output driver supply, sine wave input, $F_{IN} = 1\text{MHz}$ | | 7.9 | | mA |
| | | 2.5V output driver supply, sine wave input, $F_{IN} = 1\text{MHz}$, CLK_EXT disabled | | 6.4 | | mA |
| | Analog Power Dissipation | | | 39.6 | | mW |
| | Digital Power Dissipation | $OV_{DD} = 2.5\text{V}$, 5pF load on output bits, $F_{IN} = 1\text{MHz}$, CLK_EXT disabled | | 25.4 | | mW |
| | Total Power Dissipation | $OV_{DD} = 2.5\text{V}$, 5pF load on output bits, $F_{IN} = 1\text{MHz}$, CLK_EXT disabled | | 65 | | mW |
| | Power Down Dissipation | | | 9.3 | | μW |
| | Sleep Mode 1 | Power Dissipation, Sleep mode one channel | | 38.2 | | mW |
| | Sleep Mode 2 | Power Dissipation, Sleep mode both channels | | 15.7 | | mW |
| Clock Inputs | | | | | | |
| | Max. Conversion Rate | | 65 | | | MSPS |
| | Min. Conversion Rate | | | | 40 | MSPS |



Electrical Characteristics - CDK2308D

(AVDD = 1.8V, DVDD = 1.8V, DVDDCLK = 1.8V, OVDD = 2.5V, 80MSPS clock, 50% clock duty cycle, -1dBFS 8MHz input signal, 13-bit output, unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|--------------|--------------------------------------|--|-----|------|-----|---------------|
| Performance | | | | | | |
| SNR | Signal to Noise Ratio | $F_{IN} = 8\text{MHz}$ | 60 | 61.6 | | dBFS |
| | | $F_{IN} = 20\text{MHz}$ | | 61.2 | | dBFS |
| | | $F_{IN} = 30\text{MHz}$ | | 61.3 | | dBFS |
| | | $F_{IN} \approx FS/2$ | | 61.3 | | dBFS |
| SNDR | Signal to Noise and Distortion Ratio | $F_{IN} = 8\text{MHz}$ | 60 | 61.3 | | dBFS |
| | | $F_{IN} = 20\text{MHz}$ | | 60.7 | | dBFS |
| | | $F_{IN} = 30\text{MHz}$ | | 61 | | dBFS |
| | | $F_{IN} \approx FS/2$ | | 59 | | dBFS |
| SFDR | Spurious Free Dynamic Range | $F_{IN} = 8\text{MHz}$ | 70 | 75 | | dBc |
| | | $F_{IN} = 20\text{MHz}$ | | 75 | | dBc |
| | | $F_{IN} = 30\text{MHz}$ | | 75 | | dBc |
| | | $F_{IN} \approx FS/2$ | | 65 | | dBc |
| HD2 | Second order Harmonic Distortion | $F_{IN} = 8\text{MHz}$ | -80 | -90 | | dBc |
| | | $F_{IN} = 20\text{MHz}$ | | -95 | | dBc |
| | | $F_{IN} = 30\text{MHz}$ | | -90 | | dBc |
| | | $F_{IN} \approx FS/2$ | | -80 | | dBc |
| HD3 | Third order Harmonic Distortion | $F_{IN} = 8\text{MHz}$ | -70 | -75 | | dBc |
| | | $F_{IN} = 20\text{MHz}$ | | -75 | | dBc |
| | | $F_{IN} = 30\text{MHz}$ | | -75 | | dBc |
| | | $F_{IN} \approx FS/2$ | | -65 | | dBc |
| ENOB | Effective number of Bits | $F_{IN} = 8\text{MHz}$ | 9.7 | 9.9 | | bits |
| | | $F_{IN} = 20\text{MHz}$ | | 9.8 | | bits |
| | | $F_{IN} = 30\text{MHz}$ | | 9.8 | | bits |
| | | $F_{IN} \approx FS/2$ | | 9.5 | | bits |
| X_{TALK} | Crosstalk | Signal crosstalk between channels, $F_{IN1} = 8\text{MHz}$, $F_{IN0} = 9.9\text{MHz}$ | | -95 | | dBc |
| Power Supply | | | | | | |
| AI_{DD} | Analog Supply Current | | | 26.5 | | mA |
| DI_{DD} | Digital Supply Current | Digital core supply | | 6.1 | | mA |
| OI_{DD} | Output Driver Supply | 2.5V output driver supply, sine wave input, $F_{IN} = 1\text{MHz}$ | | 9.5 | | mA |
| | | 2.5V output driver supply, sine wave input, $F_{IN} = 1\text{MHz}$, CLK_EXT disabled | | 7.6 | | mA |
| | Analog Power Dissipation | | | 47.7 | | mW |
| | Digital Power Dissipation | $OV_{DD} = 2.5\text{V}$, 5pF load on output bits, $F_{IN} = 1\text{MHz}$, CLK_EXT disabled | | 30 | | mW |
| | Total Power Dissipation | $OV_{DD} = 2.5\text{V}$, 5pF load on output bits, $F_{IN} = 1\text{MHz}$, CLK_EXT disabled | | 77.7 | | mW |
| | Power Down Dissipation | | | 9.1 | | μW |
| | Sleep Mode 1 | Power Dissipation, Sleep mode one channel | | 46.1 | | mW |
| | Sleep Mode 2 | Power Dissipation, Sleep mode both channels | | 18.3 | | mW |
| Clock Inputs | | | | | | |
| | Max. Conversion Rate | | 80 | | | MSPS |
| | Min. Conversion Rate | | | | 65 | MSPS |



Digital and Timing Electrical Characteristics

(AVDD = 1.8V, DVDD = 1.8V, DVDDCLK = 1.8V, OVDD = 2.5V, 50 MSPS clock, 50% clock duty cycle, -1 dBFS input signal, 5pF capacitive load, unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ | Max | Units |
|------------------|-----------------------------------|--|-------------------------------|------|-------------------------|------------|
| Clock Inputs | | | | | | |
| | Duty Cycle | | 20 | | 80 | % high |
| | Compliance | | CMOS, LVDS, LVPECL, Sine Wave | | | |
| | Input Range | Differential input swing | 400 | | | mVpp |
| | | Differential input swing, sine wave clock input | 1.6 | | | Vpp |
| | Input Common Mode Voltage | Keep voltages within ground and voltage of OV _{DD} | 0.3 | | V _{OVDD} - 0.3 | V |
| | Input Capacitance | Differential | | 2 | | pF |
| Timing | | | | | | |
| T _{PD} | Start Up Time Active Mode | From Power Down Mode to Active Mode | | | 900 | clk cycles |
| T _{SLP} | Start Up Time Mode | From Sleep Mode to Active Mode | | 20 | | clk cycles |
| T _{OVR} | Out Of Range Recovery Time | | | 1 | | clk cycles |
| T _{AP} | Aperture Delay | | | 0.8 | | ns |
| ε _{RMS} | Aperture Jitter | | | <0.5 | | ps |
| T _{LAT} | Pipeline Delay | | | 12 | | clk cycles |
| T _D | Output Delay (see timing diagram) | 5pF load on output bits | | 4 | | ns |
| T _{DC} | Output Delay (see timing diagram) | Relative to CLK_EXT | | 2 | | ns |
| Logic Inputs | | | | | | |
| V _{IH} | High Level Input Voltage | V _{OVDD} ≥ 3.0V | 2 | | | V |
| | | V _{OVDD} = 1.7V – 3.0V | 0.8 • V _{OVDD} | | | V |
| V _{IL} | Low Level Input Voltage | V _{OVDD} ≥ 3.0V | 0 | | 0.8 | V |
| | | V _{OVDD} = 1.7V – 3.0V | 0 | | 0.2 • V _{OVDD} | V |
| I _{IH} | High Level Input Leakage Current | | -10 | | 10 | μA |
| I _{IL} | Low Level Input Leakage Current | | -10 | | 10 | μA |
| C _I | Input Capacitance | | | 3 | | pF |
| Logic Outputs | | | | | | |
| V _{OH} | High Level Output Voltage | | V _{OVDD} - 0.1 | | | V |
| V _{OL} | Low Level Output Voltage | | | | 0.1 | V |
| C _L | Max Capacitive Load | Post-driver supply voltage equal to pre-driver supply voltage V _{OVDD} = V _{OCVDD} | | | 5 | pF |
| | | Post-driver supply voltage above 2.25V ⁽¹⁾ | | 10 | | pF |

Note:

(1) The outputs will be functional with higher loads. However, it is recommended to keep the load on output data bits as low as possible to keep dynamic currents and resulting switching noise at a minimum.

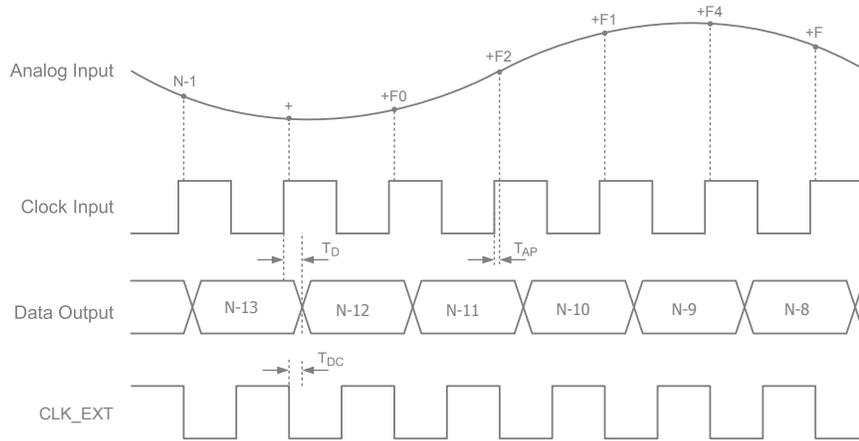


Figure 1. Timing Diagram

Recommended Usage

Analog Input

The analog inputs to the CDK2308 is a switched capacitor track-and-hold amplifier optimized for differential operation. Operation at common mode voltages at mid supply is recommended even if performance will be good for the ranges specified. The CM_EXT pin provides a voltage suitable as common mode voltage reference. The internal buffer for the CM_EXT voltage can be switched off, and driving capabilities can be changed by using the CM_EXT-BC control input.

Figure 2 shows a simplified drawing of the input network. The signal source must have sufficiently low output impedance to charge the sampling capacitors within one clock cycle. A small external resistor (e.g. 22Ω) in series with each input is recommended as it helps reducing transient currents and dampens ringing behavior. A small differential shunt capacitor at the chip side of the resistors may be used to provide dynamic charging currents and may improve performance. The resistors form a low pass filter with the capacitor, and values must therefore be determined by requirements for the application.

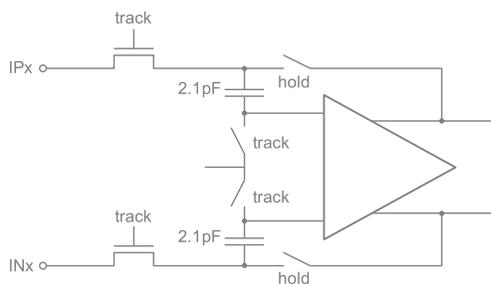


Figure 2. Input Configuration

DC-Coupling

Figure 3 shows a recommended configuration for DC-coupling. Note that the common mode input voltage must be controlled according to specified values. Preferably, the CM_EXT output should be used as a reference to set the common mode voltage.

The input amplifier could be inside a companion chip or it could be a dedicated amplifier. Several suitable single ended to differential driver amplifiers exist in the market. The system designer should make sure the specifications of the selected amplifier is adequate for the total system, and that driving capabilities comply with the CDK2308 input specifications.

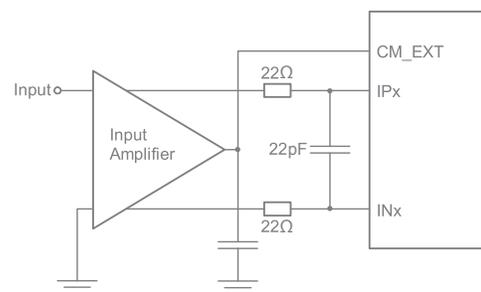


Figure 3. DC-Coupled Input

Detailed configuration and usage instructions must be found in the documentation of the selected driver.

AC-Coupling

A signal transformer or series capacitors can be used to make an AC-coupled input network. Figure 4 shows a recommended configuration using a transformer. Make sure that a transformer with sufficient linearity is selected,



and that the bandwidth of the transformer is appropriate. The bandwidth should exceed the sampling rate of the ADC with at least a factor of 10. It is also important to keep phase mismatch between the differential ADC inputs small for good HD2 performance. This type of transformer coupled input is the preferred configuration for high frequency signals as most differential amplifiers do not have adequate performance at high frequencies. Magnetic coupling between the transformers and PCB traces may impact channel crosstalk, and must hence be taken into account during PCB layout.

If the input signal is traveling a long physical distance from the signal source to the transformer (for example a long cable), kick-backs from the ADC will also travel along this distance. If these kick-backs are not terminated properly at the source side, they are reflected and will add to the input signal at the ADC input. This could reduce the ADC performance. To avoid this effect, the source must effectively terminate the ADC kick-backs, or the traveling distance should be very short. If this problem could not be avoided, the circuit in Figure 6 can be used.

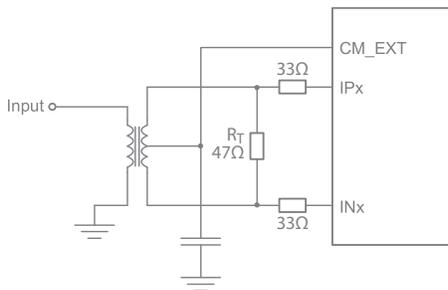


Figure 4. Transformer-Coupled Input

Figure 5 shows AC-coupling using capacitors. Resistors from the CM_EXT output, RCM, should be used to bias the differential input signals to the correct voltage. The series capacitor, CI, form the high-pass pole with these resistors, and the values must therefore be determined based on the requirement to the high-pass cut-off frequency.

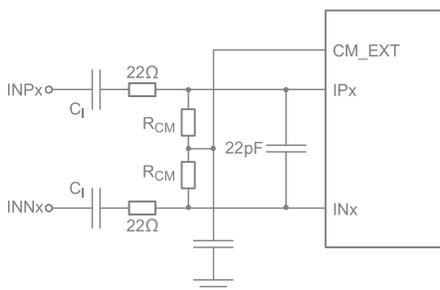


Figure 5. AC-Coupled Input

Note that startup time from Sleep Mode and Power Down Mode will be affected by this filter as the time required to charge the series capacitors is dependent on the filter cut-off frequency.

If the input signal has a long traveling distance, and the kick-backs from the ADC not are effectively terminated at the signal source, the input network of figure 8 can be used. The configuration in figure 8 is designed to attenuate the kickback from the ADC and to provide an input impedance that looks as resistive as possible for frequencies below Nyquist. Values of the series inductor will however depend on board design and conversion rate. In some instances a shunt capacitor in parallel with the termination resistor (e.g. 33pF) may improve ADC performance further. This capacitor attenuate the ADC kick-back even more, and minimize the kicks traveling towards the source. However, the impedance match seen into the transformer becomes worse.

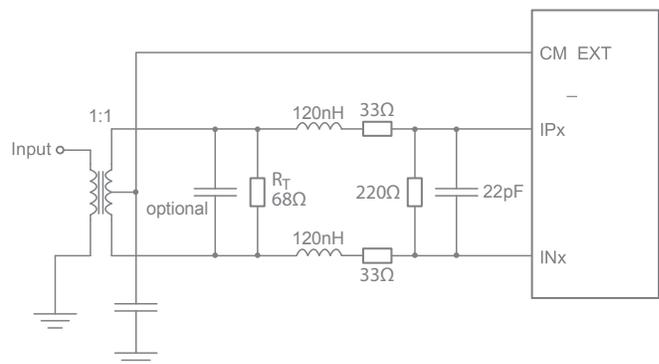


Figure 6. Alternative Input Network

Clock Input And Jitter Considerations

Typically high-speed ADCs use both clock edges to generate internal timing signals. In the CDK2308 only the rising edge of the clock is used. Hence, input clock duty cycles between 20% and 80% is acceptable.

The input clock can be supplied in a variety of formats. The clock pins are AC-coupled internally, and hence a wide common mode voltage range is accepted. Differential clock sources as LVDS, LVPECL or differential sine wave can be connected directly to the input pins. For CMOS inputs, the CLKN pin should be connected to ground, and the CMOS clock signal should be connected to CLKP. For differential sine wave clock input the amplitude must be at least $\pm 80\text{mV}_{pp}$.



The quality of the input clock is extremely important for high-speed, high-resolution ADCs. The contribution to SNR from clock jitter with a full scale signal at a given frequency is shown in equation 1.

$$\text{SNR}_{\text{jitter}} = 20 \cdot \log (2 \cdot \pi \cdot F_{\text{IN}} \cdot \epsilon_t)$$

where F_{IN} is the signal frequency, and ϵ_t is the total rms jitter measured in seconds. The rms jitter is the total of all jitter sources including the clock generation circuitry, clock distribution and internal ADC circuitry.

For applications where jitter may limit the obtainable performance, it is of utmost importance to limit the clock jitter. This can be obtained by using precise and stable clock references (e.g. crystal oscillators with good jitter specifications) and make sure the clock distribution is well controlled. It might be advantageous to use analog power and ground planes to ensure low noise on the supplies to all circuitry in the clock distribution. It is of utmost importance to avoid crosstalk between the ADC output bits and the clock and between the analog input signal and the clock since such crosstalk often results in harmonic distortion.

The jitter performance is improved with reduced rise and fall times of the input clock. Hence, optimum jitter performance is obtained with LVDS or LVPECL clock with fast edges. CMOS and sine wave clock inputs will result in slightly degraded jitter performance.

If the clock is generated by other circuitry, it should be retimed with a low jitter master clock as the last operation before it is applied to the ADC clock input.

Digital Outputs

Digital output data are presented on parallel CMOS form. The voltage on the OV_{DD} pin set the levels of the CMOS outputs. The output drivers are dimensioned to drive a wide range of loads for OV_{DD} above 2.25V, but it is recommended to minimize the load to ensure as low transient switching currents and resulting noise as possible. In applications with a large fanout or large capacitive loads, it is recommended to add external buffers located close to the ADC chip.

The timing is described in the Timing Diagram section. Note that the load or equivalent delay on CLK_{EXT} always should be lower than the load on data outputs to ensure sufficient timing margins.

The digital outputs can be set in tristate mode by setting the OE_{N} signal high.

The CDK2308 employs digital offset correction. This means that the output code will be 4096 with the positive and negative inputs shorted together (zero differential). However, small mismatches in parasitics at the input can cause this to alter slightly. The offset correction also results in possible loss of codes at the edges of the full scale range. With "NO" offset correction, the ADC would clip in one end before the other, in practice resulting in code loss at the opposite end. With the output being centered digitally, the output will clip, and the out of range flags will be set, before max code is reached. When out of range flags are set, the code is forced to all ones for over-range and all zeros for under-range.

Data Format Selection

The output data are presented on offset binary form when DFRMT is low (connect to OV_{SS}). Setting DFRMT high (connect to OV_{DD}) results in 2's complement output format. Details are shown in Table 1 on page 14.

Reference Voltages

The reference voltages are internally generated and buffered based on a bandgap voltage reference. No external decoupling is necessary, and the reference voltages are not available externally. This simplifies usage of the ADC since two extremely sensitive pins, otherwise needed, are removed from the interface.

Operational Modes

The operational modes are controlled with the PD_{N} and SLP_{N} pins. If PD_{N} is set low, all other control pins are overridden and the chip is set in Power Down mode. In this mode all circuitry is completely turned off and the internal clock is disabled. Hence, only leakage current contributes to the Power Down Dissipation. The startup time from this mode is longer than for other idle modes as all references need to settle to their final values before normal operation can resume.

The SLP_{N} bus can be used to power down each channel independently, or to set the full chip in Sleep Mode. In this mode internal clocking is disabled, but some low bandwidth circuitry is kept on to allow for a short startup time. However, Sleep Mode represents a significant reduction in supply current, and it can be used to save power even for short idle periods.

The input clock should be kept running in all idle modes. However, even lower power dissipation is possible in Power Down mode if the input clock is stopped. In this case it is important to start the input clock prior to enabling active mode.

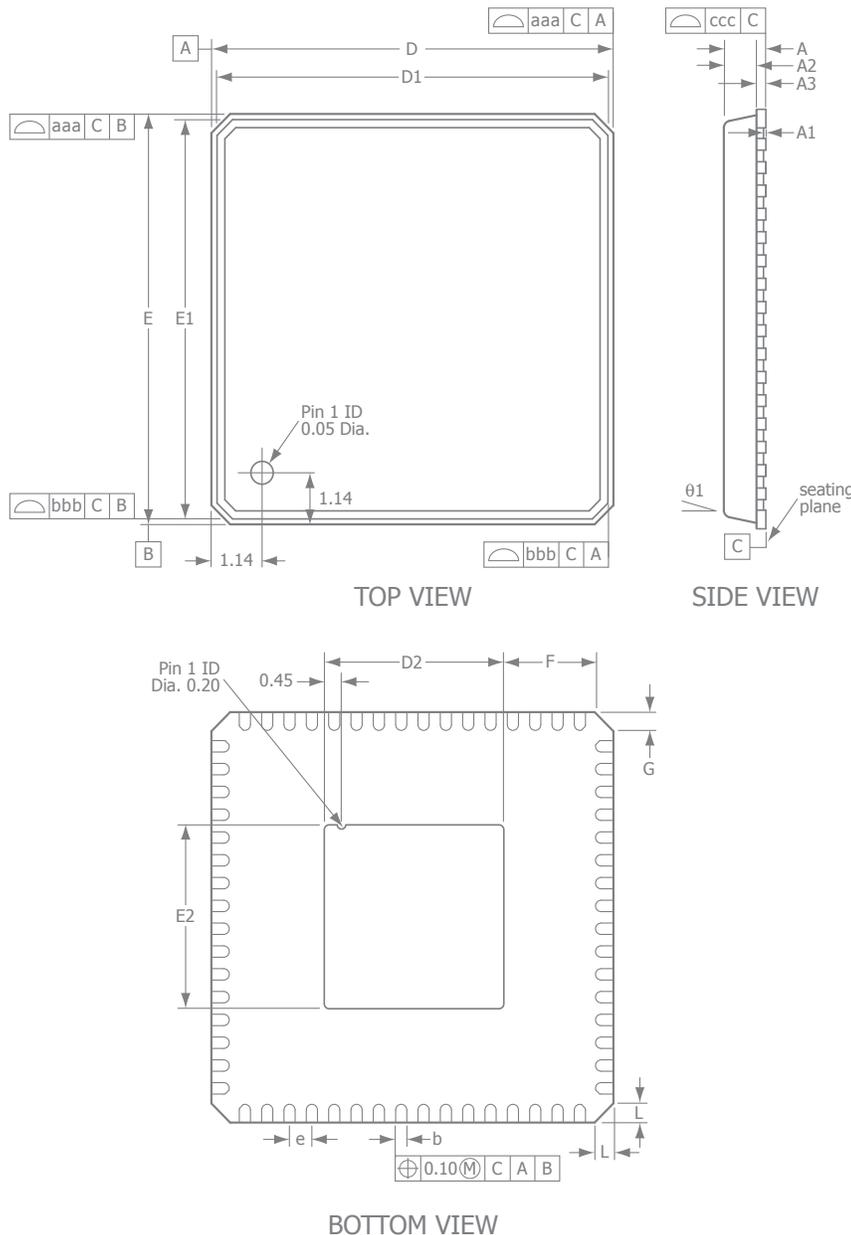


Table 1: Data Format Description for 2V_{pp} Full Scale Range

| Differential Input Voltage (IP _x - IN _x) | Output data: Dx_9 : Dx_0 (DFRMT = 0, offset binary) | Output Data: Dx_9 : Dx_0 (DFRMT = 1, 2's complement) |
|---|--|---|
| 1.0 V | 11 1111 1111 | 01 1111 1111 |
| +0.24mV | 10 0000 0000 | 00 0000 0000 |
| -0.24mV | 01 1111 1111 | 11 1111 1111 |
| -1.0V | 00 0000 0000 | 10 0000 0000 |

Mechanical Dimensions

QFN-64 Package



| Symbol | Inches | | | Millimeters | | |
|--------------------------------|--------|-----------|-------|-------------|----------|------|
| | Min | Typ | Max | Min | Typ | Max |
| A | – | – | 0.035 | – | – | 0.9 |
| A ₁ | 0.00 | 0.0004 | 0.002 | 0.00 | 0.01 | 0.05 |
| A ₂ | – | 0.026 | 0.028 | – | 0.65 | 0.7 |
| A ₃ | – | 0.008 REF | – | – | 0.2 REF | – |
| b | 0.008 | 0.010 | 0.012 | 0.2 | 0.25 | 0.30 |
| D | – | 0.354 BSC | – | – | 9.00 BSC | – |
| D ₁ | – | 0.354 BSC | – | – | 8.75 BSC | – |
| D ₂ | 0.197 | 0.205 | 0.213 | 5.0 | 5.2 | 5.4 |
| E | – | 0.354 BSC | – | – | 9.00 BSC | – |
| E ₁ | – | 0.344 BSC | – | – | 8.75 BSC | – |
| E ₂ | 0.197 | 0.205 | 0.213 | 5.0 | 5.2 | 5.4 |
| F | 0.05 | – | – | 1.3 | – | – |
| G | 0.0096 | 0.0168 | 0.024 | 0.24 | 0.42 | 0.6 |
| L | 0.012 | 0.016 | 0.020 | 0.3 | 0.4 | 0.5 |
| e | – | 0.020 BSC | – | – | 0.50 BSC | – |
| θ ₁ | 0° | – | 12° | 0° | – | 12° |
| Tolerance of Form and Position | | | | | | |
| aaa | – | 0.10 | – | – | 0.004 | – |
| bbb | – | 0.10 | – | – | 0.004 | – |
| ccc | – | 0.05 | – | – | 0.002 | – |

- NOTES:**
- All dimensions are in millimeters.
 - Die thickness allowable is 0.305mm maximum (.012 inches maximum)
 - Dimensioning & tolerances conform to ASME y14.5m, -1994.
 - Dimension applies to plated terminal and is measured between 0.20 and 0.25mm from terminal tip.
 - The pin #1 identifier must be placed on the top surface of the package by using indentation mark or other feature of package body.
 - Exact shape and size of this feature is optional.
 - Package warpage max 0.08mm.
 - Applied for exposed pad and terminals. Exclude embedding part of exposed pad from measuring.
 - Applied only to terminals.
 - Package corners unless otherwise specified are R0.175±0.025mm.



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