# QUAD DIFFERENTIAL AND/NAND

SY10E404 SY100E404

#### **FEATURES**

- Differential D and Q
- Extended 100E VEE range of -4.2V to -5.5V
- 700ps max. propagation delay
- **■** High frequency outputs
- Internal 75K $\Omega$  input pull-down resistors
- Fully compatible with Motorola 10E/100E404
- Available in 28-pin PLCC package

#### **DESCRIPTION**

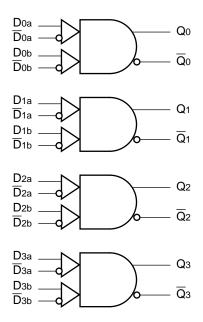
The SY10/100E404 are 4-bit differential AND/NAND devices. The differential operation of these devices make them ideal for pulse shaping applications where duty cycle skew is critical. Special design techniques were incorporated to minimize the skew between the upper and lower level gate inputs.

Because a negative 2-input NAND function is equivalent to a 2-input OR function, the differential inputs and outputs of the devices also allow for their use as fully differential 2-input OR/NOR functions.

The output RISE/FALL times of these devices are significantly faster than most other standard ECLinPS devices, resulting in an increased bandwidth.

The differential inputs have clamp structures which will force the Q output of a gate in an open input condition to go to a LOW state. Thus, inputs of unused gates can be left open and will not affect the operation of the rest of the device.

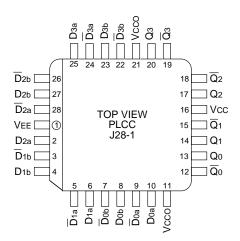
#### **BLOCK DIAGRAM**



#### **PIN NAMES**

Pin	Function
D[0:4], $\overline{D}$ [0:4]	Differential Data Inputs
Q[0:4], Q[0:4]	Differential Data Outputs
Vcco	Vcc to Output

## **PACKAGE/ORDERING INFORMATION**



28-Pin PLCC (J28-1)

## Ordering Information<sup>(1)</sup>

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY10E404JC	J28-1	Commercial	SY10E404JC	Sn-Pb
SY10E404JCTR <sup>(2)</sup>	J28-1	Commercial	SY10E404JC	Sn-Pb
SY100E404JC	J28-1	Commercial	SY100E404JC	Sn-Pb
SY100E404JCTR <sup>(2)</sup>	J28-1	Commercial	SY100E404JC	Sn-Pb
SY10E404JZ <sup>(3)</sup>	J28-1	Commercial	SY10E404JZ with Pb-Free bar-line indicator	Matte-Sn
SY10E404JZTR <sup>(2, 3)</sup>	J28-1	Commercial	SY10E404JZ with Pb-Free bar-line indicator	Matte-Sn
SY100E404JZ <sup>(3)</sup>	J28-1	Commercial	SY100E404JZ with Pb-Free bar-line indicator	Matte-Sn
SY100E404JZTR <sup>(2, 3)</sup>	J28-1	Commercial	SY100E404JZ with Pb-Free bar-line indicator	Matte-Sn

#### Notes

- 1. Contact factory for die availability. Dice are guaranteed at  $T_A$  = 25°C, DC Electricals only.
- 2. Tape and Reel.
- 3. Pb-Free package is recommended for new designs.

### **TRUTH TABLE**

Da	Db	Q	Da	Db	Q
L	L	L	L	L	L
L	Н	L	L	Н	Н
Н	L	L	Н	L	Н
Н	Н	Н	Н	Н	Н

## DC ELECTRICAL CHARACTERISTICS

VEE = VEE (Min.) to VEE (Max.); VCC = VCCO = GND

		TA = 0°C		TA = +25°C			TA = +85°C					
Symbol	Parameter	Min.	Тур.	Max.	Min.	Тур.	Max.	Min.	Тур.	Max.	Unit	Condition
IIН	Input HIGH Current	_	_	150	_	_	150	_	_	150	μΑ	_
lee	Power Supply Current 10E 100E	_	106 106	127 127	_	106 106	127 127	_	106 122	127 146	mA	
VPP (DC)	Input Sensitivity	50	_	_	50	_	_	50	_	_	mV	1
VCMR	Common Mode Range	-1.5	_	0	-1.5	_	0	-1.5	_	0	V	2

#### Notes:

- 1. Differential input voltage required to obtain a full ECL swing on the outputs.
- 2. VCMR is referenced to the most positive side of the differential input signal. Normal operation is obtained when the input signals are within the VCMR range and the input swing is greater than VPP (min.) and <1V.

### **AC ELECTRICAL CHARACTERISTICS**

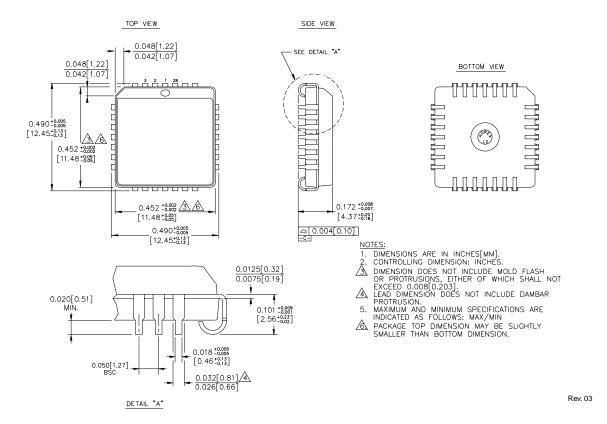
VEE = VEE (Min.) to VEE (Max.); VCC = VCCO = GND

		TA = 0°C		TA = +25°C			TA = +85°C					
Symbol	Parameter	Min.	Тур.	Max.	Min.	Тур.	Max.	Min.	Тур.	Max.	Unit	Condition
tPD	Propagation Delay to Output Da (Diff) Da (SE) Db (Diff) Db (SE)	350 300 375 325	475 475 500 500	650 700 675 725	350 300 375 325	475 475 500 500	650 700 675 725	350 300 375 325	475 475 500 500	650 700 675 725	ps	
tskew	Within-Device Skew	_	50	_	_	50	_	_	50	_	ps	1
VPP(AC)	Minimum Input Swing	150	_	_	150	_	_	150	_	_	mV	2
tr tf	Rise/Fall Time 20–80%	150	_	400	150	_	400	150	_	400	ps	_

#### Notes:

- 1. Within-device skew is defined as identical transitions on similar paths through a device.
- 2. Minimum input swing for which AC parameters are guaranteed.

#### 28-PIN PLCC (J28-1)



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