

M95M04-DR

Errata sheet

M95M04-DR device limitations

Silicon identification

This errata sheet applies to the device M95M04-DR, the 4-Mbit serial SPI bus EEPROM. The Table 1 give the list of the orderable part numbers impacted by this change.

Table 1. Device summary

Reference	Part number
M95M04-DR	M95M04-DRMN6TP
	M95M04-DRDW6TP
	M95M04-DRCS6TPVF

1 Limitation

1.1 Lock ID instruction

Description

The section of the M95M04-DR datasheet (DS12179 rev 1, available on www.st.com) detailing the Lock ID instruction indicates that the data byte to be sent must be equal to the binary value xxxx xx1x, where x = Don't care

The value xxxx xx10 does not lock the identification page.

Workaround

The correct data byte to be sent for locking the identification page is:

- Bits b7 to b1 equal to "Don't care"
- Bit b0 must be equal to 1
- That is in binary: xxxx xxx1

1.2 Datasheet change

In revision 1 of the M95M04-DR datasheet the text in the section describing the Lock ID instruction

"The Lock ID instruction is issued by driving Chip select (S) low, sending the instruction code, the address and a data byte on Serial data input (D), and driving Chip select (S) high. In the address sent, A10 must be equal to 1, all other address bits are Don't Care. The data byte sent must be equal to the binary value xxxx xx1x, where x = Don't Care"

must be replaced by

"The Lock ID instruction is issued by driving Chip select (S) low, sending the instruction code, the address and a data byte on Serial data input (D), and driving Chip select (S) high. In the address sent, A10 must be equal to 1, all other address bits are Don't Care. The data byte sent must have the b0 bit equal to 1 (b0=1) and the others value of the bits b7 to b1 are Don't Care"

Revision history

Table 2. Document revision history

Date	Version	Changes
24-Mar-2020	1	Initial release.

Contents

1	Limit	ation	.2
	1.1	Lock ID instruction.	. 2
	1.2	Datasheet change	. 2
Revi	ision h	listory	.3

List of tables

Table 1.	Device summary	1
Table 2.	Document revision history	3

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