Product Specification

PE43705

UltraCMOS® RF Digital Step Attenuator, 7-bit, 31.75 dB 50 MHz – 8 GHz

Features

- Attenuation options: covers a 31.75 dB range in 0.25 dB, 0.5 dB, or 1.0 dB steps
  - 0.25 dB monotonicity for ≤ 6 GHz
  - 0.50 dB monotonicity for ≤ 7 GHz
  - 1.00 dB monotonicity for ≤ 8 GHz
- Safe attenuation state transitions
- High power handling
  - 31 dBm, Pulsed @ 8 GHz
  - 28 dBm, CW @ 8 GHz
- High linearity: +58 dBm IIP3
- 1.8V control logic compatible
- 105°C operating temperature
- Programming modes
  - Direct Parallel
  - Latched Parallel
  - Serial
  - Serial Addressable
- High-attenuation state @ power-up (PUP)
- ESD performance
  - 1.5 kV HBM on all pins

Product Description

The PE43705 is a 50Ω, HaRP™ technology-enhanced, 7-bit RF digital step attenuator (DSA) designed for use in 3G/4G wireless infrastructure and other high performance RF applications.

This DSA is a pin-compatible upgraded version of PE43703 with higher power handling and a wider frequency, control voltage and operating temperature range. An integrated digital control interface supports both serial and parallel programming of the attenuation, including the capability to program an initial attenuation state at power-up.

Covering a 31.75 dB attenuation range in 0.25 dB, 0.50 dB, or 1 dB steps, it maintains a monotonic step response from 50 MHz through 8 GHz. PE43705 also features safe attenuation state transitions and is offered in a 32-lead 5x5 mm QFN package. In addition, no external blocking capacitors are required if 0V DC is present on the RF ports.

The PE43705 is manufactured on pSemi's UltraCMOS® process, a patented variation of silicon-on-insulator (SOI) technology on a sapphire substrate.

pSemi's HaRP™ technology enhancements deliver high linearity and excellent harmonics performance. It is an innovative feature of the UltraCMOS process, offering the performance of GaAs with the economy and integration of conventional CMOS.

Figure 1. Functional Diagram

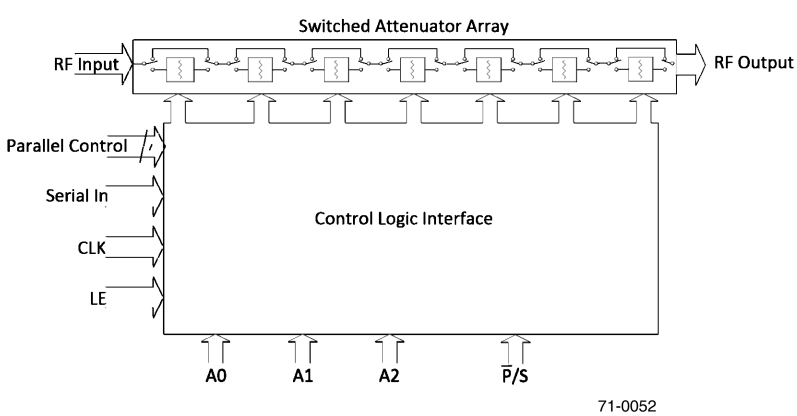


Figure 2. Package Type
32-lead 5x5 mm QFN

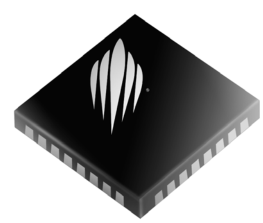


Table 1. Electrical Specifications: 0.25 dB steps @ +25°C, V_{DD} = 2.3V to 5.5V, (Z_S = Z_L = 50Ω), unless otherwise noted

Parameter	Condition	Frequency	Min	Typ	Max	Unit
Operating frequency			50		6000	MHz
Attenuation range	0.25 dB step			0 – 31.75		dB
Insertion loss		50 MHz – 2.2 GHz 2.2 GHz – 4 GHz 4 GHz – 6 GHz		1.3 1.7 2.4	1.6 2.0 2.8	dB dB dB
Attenuation error	0 dB – 15.75 dB Attenuation settings	50 MHz – 2.2 GHz			+ (0.15 + 1.5% of attenuation setting) – (0.1 + 1% of attenuation setting)	dB dB
		>2.2 GHz – 4 GHz			+ (0.15 + 3% of attenuation setting) – (0.1 + 1% of attenuation setting)	dB dB
		>4 GHz – 6 GHz			+ (0.2 + 6% of attenuation setting) – (0.15 + 1% of attenuation setting)	dB dB
	16 dB – 31.75 dB Attenuation settings	50 MHz – 2.2 GHz			+ (0.15 + 1.5% attenuation Setting) – (0.1 + 1.5% of attenuation setting)	dB dB
		>2.2 GHz – 4 GHz			+ (0.15 + 4% attenuation Setting) – (0.1 + 0.75% of attenuation setting)	dB dB
		>4 GHz – 6 GHz			+ (0.25 + 7.5% of attenuation setting) – (0.2 + 0% of attenuation setting)	dB dB
Return loss	Input port	50 MHz – 4 GHz 4 GHz – 6 GHz		20 15		dB dB
Return loss	Output port	50 MHz – 4 GHz 4 GHz – 6 GHz		17 13		dB dB
Relative phase	0 dB – 31.75 dB Attenuation settings	50 MHz – 6 GHz		55		deg
Input 0.1dB compression point[1]		50 MHz – 6 GHz		34		dBm
Input IP3	Two tones at +20 dBm, 500 kHz spacing	50 MHz – 6 GHz		58		dBm
RF Trise/Tfall	10% / 90% RF			568		ns
Switching time	50% CTRL to 90% or 10% RF			1		µs

Note 1: The input 0.1dB compression point is a linearity figure of merit. Refer to *Table 5* for the operating RF input power (50Ω).

Table 2. Electrical Specifications: 0.5 dB steps @ +25°C, V_{DD} = 2.3V to 5.5V, (Z_S = Z_L = 50Ω), unless otherwise noted

Parameter	Condition	Frequency	Min	Typ	Max	Unit
Operating frequency			50		7000	MHz
Attenuation range	0.5 dB step			0 – 31.5		dB
Insertion loss		50 MHz – 2.2 GHz 2.2 GHz – 4 GHz 4 GHz – 6 GHz 6 GHz – 7 GHz		1.3 1.7 2.4 2.5	1.6 2.0 2.8 2.9	dB dB dB dB
Attenuation error	0 dB – 15.5 dB Attenuation settings	50 MHz – 2.2 GHz			(0.15 + 1.5% of attenuation setting) – (0.1 + 2% of attenuation setting)	dB dB
		>2.2 GHz – 4 GHz			(0.15 + 3.5% of attenuation setting) – (0.1 + 1% of attenuation setting)	dB dB
		>4 GHz – 7 GHz			+ (0.25 + 6% of attenuation setting) – (0.25 + 0% of attenuation setting)	dB dB
	16 dB – 31.5 dB Attenuation settings	50 MHz – 2.2 GHz			+ (0.2 + 1.5% of attenuation setting) – (0.1 + 2% of attenuation setting)	dB dB
		>2.2 GHz – 4 GHz			(0.2 + 4% of attenuation setting) – (0.1 + 1% of attenuation setting)	dB dB
		>4 GHz – 7 GHz			+ (0.3 + 7% of attenuation setting) – (0.25 + 2.5% of attenuation setting)	dB dB
Return loss	Input port	50 MHz – 4 GHz 4 GHz – 7 GHz		20 17		dB dB
Return loss	Output port	50 MHz – 4 GHz 4 GHz – 7 GHz		17 15		dB dB
Relative phase	0 dB – 31.5 dB Attenuation settings	50 MHz – 7 GHz		66		deg
Input 0.1dB compression point[1]		50 MHz – 7 GHz		34		dBm
Input IP3	Two tones at +20 dBm, 500 kHz spacing	50 MHz –7 GHz		58		dBm
RF Trise/Tfall	10% / 90% RF			568		ns
Switching time	50% CTRL to 90% or 10% RF			1		μs

Note 1: The input 0.1dB compression point is a linearity figure of merit. Refer to *Table 5* for the operating RF input power (50Ω).

Table 3. Electrical Specifications: 1 dB steps @ +25°C, V_{DD} = 2.3V to 5.5V, (Z_S = Z_L = 50Ω), unless otherwise noted

Parameter	Condition	Frequency	Min	Typ	Max	Unit
Operating frequency			50		8000	MHz
Attenuation range	1 dB step			0 – 31		dB
Insertion loss		50 MHz – 2.2 GHz 2.2 GHz – 4 GHz 4 GHz – 6 GHz 6 GHz – 8 GHz		1.3 1.7 2.4 2.8	1.6 2.0 2.8 3.2	dB dB dB dB
Attenuation error	0 dB – 15 dB Attenuation settings	50 MHz – 2.2 GHz			+ (0.15 + 1.5% of attenuation setting) – (0.1 + 1% of attenuation setting)	dB dB
		>2.2 GHz – 4 GHz			+ (0.15 + 3.5% of attenuation setting) – (0.1 + 1% of attenuation setting)	dB dB
		>4 GHz – 8 GHz			+ (0.3 + 6.5% of attenuation setting) – (0.25 + 2% of attenuation setting)	dB dB
	16dB – 31 dB Attenuation settings	50 MHz – 2.2 GHz			+ (0.2 + 1.5% of attenuation setting) – (0.1 + 1.5% of attenuation setting)	dB dB
		>2.2 GHz – 4 GHz			+ (0.2 + 4% of attenuation setting) – (0.1 + 1% of attenuation setting)	dB dB
		>4 GHz – 8 GHz			+ (0.3 + 7% of attenuation setting) – (0.3 + 4.5% of attenuation setting)	dB dB
Return loss	Input port	50 MHz – 4 GHz 4 GHz – 8 GHz		20 15		dB dB
Return loss	Output port	50 MHz – 4 GHz 4 GHz – 8 GHz		17 13		dB dB
Relative phase	0 dB – 31 dB Attenuation settings	50 MHz – 8 GHz		77		deg
Input 0.1dB compression point[1]		50 MHz – 8 GHz		34		dBm
Input IP3	Two tones at +20 dBm, 500 kHz spacing	50 MHz – 8 GHz		58		dBm
RF Trise/Tfall	10% / 90% RF			568		ns
Switching time	50% CTRL to 90% or 10% RF			1		μs

Note 1: The input 0.1dB compression point is a linearity figure of merit. Refer to *Table 5* for the operating RF input power (50Ω).

Figure 3. Pin Configuration (Top View)

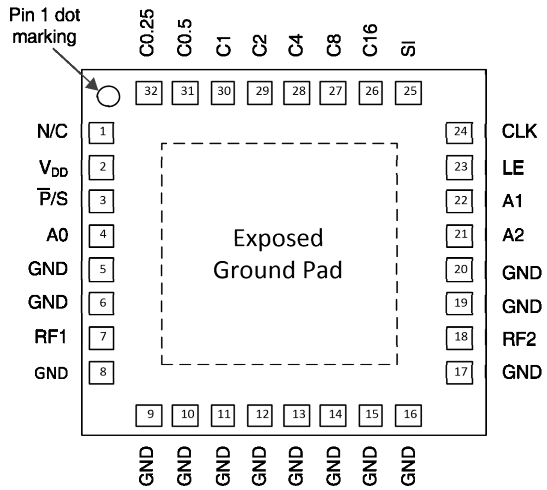


Table 4. Pin Descriptions

Pin #	Pin Name	Description
1	N/C	No connect
2	V_{DD}	Supply voltage
3	$\overline{P}$/S	Serial/Parallel mode select
4	A0	Address bit A0 connection
5, 6, 8-17, 19, 20	GND	Ground
7	RF1[1]	RF1 port (RF input)
18	RF2[1]	RF2 port (RF output)
21	A2	Address bit A2 connection
22	A1	Address bit A1 connection
23	LE	Serial interface latch enable input
24	CLK	Serial interface clock input
25	SI	Serial interface data input
26	C16 (D6)[2]	Parallel control bit, 16 dB
27	C8 (D5)[2]	Parallel control bit, 8 dB
28	C4 (D4)[2]	Parallel control bit, 4 dB
29	C2 (D3)[2]	Parallel control bit, 2 dB
30	C1 (D2)[2]	Parallel control bit, 1 dB
31	C0.5 (D1)[2]	Parallel control bit, 0.5 dB
32	C0.25 (D0)[2]	Parallel control bit, 0.25 dB
Pad	GND	Exposed pad: ground for proper operation

Notes: 1. RF pins 7 and 18 must be at 0V DC. The RF pins do not require DC blocking capacitors for proper operation if the 0V DC requirement is met
2. Ground C0.25, C0.5, C1 C2, C4, C8, C16 if not in use

Table 5. Operating Ranges

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{DD}	2.3		5.5	V
Supply current	I_{DD}		130	200	µA
Digital input high	V_{IH}	1.17		3.6	V
Digital input low	V_{IL}	–0.3		0.6	V
Digital input current	I_{CTRL}			15	µA
RF input power, CW	$P_{MAX,CW}$			+28	dBm
RF input power, pulsed[1]	$P_{MAX,PULSED}$			+31	dBm
Operating temperature range	T_{OP}	-40		+105	°C

Note 1: Pulsed, 2.5% duty cycle of 4620 µs period, 50Ω

Table 6. Absolute Maximum Ratings

Parameter/Condition	Symbol	Min	Max	Unit
Supply voltage	V_{DD}	-0.3	5.5	V
Digital input voltage	V_{CTRL}	-0.3	3.6	V
Maximum input power	$P_{MAX,ABS}$		+34	dBm
Storage temperature range	T_{ST}	-65	150	°C
ESD voltage HBM[1], all pins	$V_{ESD,HBM}$		1500	V
ESD voltage MM[2], all pins	$V_{ESD,MM}$		200	V
ESD voltage CDM[3], all pins	$V_{ESD,CDM}$		250	V

Notes: 1. Human Body Model (MIL-STD 883 Method 3015)
2. Machine Model (JEDEC JESD22-A115)

Exceeding absolute maximum ratings may cause permanent damage. Operation should be restricted to the limits in the Operating Ranges table. Operation between operating range maximum and absolute maximum for extended periods may reduce reliability.

Safe Attenuation State Transitions

The PE43705 features a novel architecture to provide safe transition behavior when changing attenuation states. When RF input power is applied, positive output power spikes are prevented during attenuation state changes by optimized internal timing control.

Electrostatic Discharge (ESD) Precautions

When handling this UltraCMOS® device, observe the same precautions that you would use with other ESD-sensitive devices. Although this device contains circuitry to protect it from damage due to ESD, precautions should be taken to avoid exceeding the specified rating.

Latch-Up Avoidance

Unlike conventional CMOS devices, UltraCMOS® devices are immune to latch-up.

Moisture Sensitivity Level

The moisture sensitivity level rating for the PE43705 in the 32-lead 5x5 mm QFN package is MSL1.

Switching Frequency

The PE43705 has a maximum 25 kHz switching rate.

Switching frequency is defined to be the speed at which the DSA can be toggled across attenuation states. Switching time is the time duration between the point the control signal reaches 50% of the final value and the point the output signal reaches within 10% or 90% of its target value.

Spurious Performance

The typical low-frequency spurious performance of the PE43705 is -140 dBm.

Table 7. Parallel Truth Table

Parallel Control Setting							Attenuation Setting RF1-RF2
D6	D5	D4	D3	D2	D1	D0	
L	L	L	L	L	L	L	Reference I.L.
L	L	L	L	L	L	H	0.25 dB
L	L	L	L	L	H	L	0.5 dB
L	L	L	L	H	L	L	1 dB
L	L	L	H	L	L	L	2 dB
L	L	H	L	L	L	L	4 dB
L	H	L	L	L	L	L	8 dB
H	L	L	L	L	L	L	16 dB
H	H	H	H	H	H	H	31.75 dB

Table 8. Serial Attenuation Word Truth Table

Attenuation Word								Attenuation Setting RF1-RF2
D7	D6	D5	D4	D3	D2	D1	D0 (LSB)	
L	L	L	L	L	L	L	L	Reference I.L.
L	L	L	L	L	L	L	H	0.25 dB
L	L	L	L	L	L	H	L	0.5 dB
L	L	L	L	L	H	L	L	1 dB
L	L	L	L	H	L	L	L	2 dB
L	L	L	H	L	L	L	L	4 dB
L	L	H	L	L	L	L	L	8 dB
L	H	L	L	L	L	L	L	16 dB
L	H	H	H	H	H	H	H	31.75 dB

Table 9. Serial Address Word Truth Table

Address Word								Address Setting
A7 (MSB)	A6	A5	A4	A3	A2	A1	A0	
X	X	X	X	X	L	L	L	000
X	X	X	X	X	L	L	H	001
X	X	X	X	X	L	H	L	010
X	X	X	X	X	L	H	H	011
X	X	X	X	X	H	L	L	100
X	X	X	X	X	H	L	H	101
X	X	X	X	X	H	H	L	110
X	X	X	X	X	H	H	H	111

Table 10. Serial Addressable Register Map

(checkered) Bits can either be set to logic high or logic low

(grey) D7 must be set to logic low

MSB (last in) ... LSB (first in)

Q15	Q14	Q13	Q12	Q11	Q10	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
A7	A6	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0
Address Word								Attenuation Word							

Attenuation Word is derived directly from the attenuation value. For example, to program the 18.25 dB state at address 3:

Address word: XXXXX011
Attenuation Word: Multiply by 4 and convert to binary → 4 * 18.25 dB → 73 → 01001001
Serial Input: XXXXX01101001001

Programming Options

Parallel/Serial Selection

Either a parallel or serial addressable interface can be used to control the PE43705. The P/S bit provides this selection, with P/S = LOW selecting the Parallel interface and P/S = HIGH selecting the Serial Addressable interface.

Parallel Mode Interface

The parallel interface consists of seven CMOS-compatible control lines that select the desired attenuation state, as shown in *Table 7*.

The parallel interface timing requirements are defined by *Figure 5* (Parallel Interface Timing Diagram), *Table 13* (Parallel and Direct Interface AC Characteristics) and switching time (*Tables 1-3*).

For latched parallel programming, the latch enable (LE) should be held LOW while changing attenuation state control values, then pulse LE HIGH to LOW (*per Figure 5*) to latch new attenuation state into device.

For direct parallel programming, the LE line should be pulled HIGH. Changing attenuation state control values will change device state to new attenuation. Direct mode is ideal for manual control of the device (using hardwire, switches, or jumpers).

Serial Interface

The serial addressable interface is a 16-bit serial-in, parallel-out shift register buffered by a transparent latch. The 16-bits make up two words comprised of 8-bits each. The first word is the attenuation word, which controls the state of the DSA. The second word is the address word, which is compared to the static (or programmed) logical states of the A0, A1 and A2 digital inputs. If there is an address match, the DSA changes state; otherwise its current state will remain unchanged. *Figure 4* illustrates an example timing diagram for programming a state. It is required that all parallel control inputs be grounded when the DSA is used in serial addressable mode.

The serial interface is controlled using three CMOS-compatible signals: serial-in (SI), clock (CLK), and latch enable (LE). The SI and CLK inputs allow data to be serially entered into the shift register. Serial data is clocked in LSB first, beginning with the attenuation word.

The shift register must be loaded while LE is held LOW to prevent the attenuator value from changing as data is entered. The LE input should then be toggled HIGH and brought LOW again, latching the new data into the DSA. Attenuation word and address word truth tables are listed in *Table 8* and *Table 9*. A programming example of the serial register is illustrated in *Table 10.* The serial timing diagram is illustrated in *Figure 4.*

Power-up Control Settings

The PE43705 will always initialize to the maximum attenuation setting (31.75 dB) on power-up for both the serial addressable and latched parallel modes of operation and will remain in this setting until the user latches in the next programming word. In direct parallel mode, the DSA can be preset to any state within the 31.75 dB range by pre-setting the parallel control pins prior to power-up. In this mode, there is a 400 μs delay between the time the DSA is powered-up to the time the desired state is set. During this power-up delay, the device attenuates to the maximum attenuation setting (31.75 dB) before defaulting to the user defined state. If the control pins are left floating in this mode during power-up, the device will default to the minimum attenuation setting (insertion loss state).

Dynamic operation between serial and parallel programming modes is possible.

If the DSA powers up in Serial mode (P/S = HIGH), all the parallel control inputs DI[6:0] must be set to logic LOW. Prior to toggling to parallel mode, the DSA *must* be programmed serially to ensure D[7] is set to logic low.

If the DSA powers up in either latched or direct parallel mode, all parallel pins DI[6:0] must be set to logic LOW prior to toggling to serial addressable mode (P/S = HIGH), and *held* low until the DSA has been programmed serially to ensure bit D[7] is set to logic low.

The sequencing is only required once on power-up. Once completed, the DSA may be toggled between serial and parallel programming modes at will.

Figure 4. Serial Timing Diagram

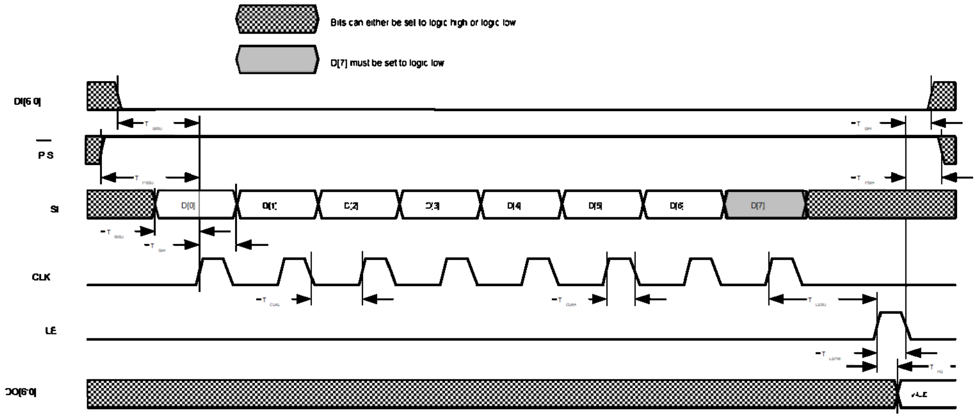


Figure 5. Latched Parallel/Direct Parallel Timing Diagram

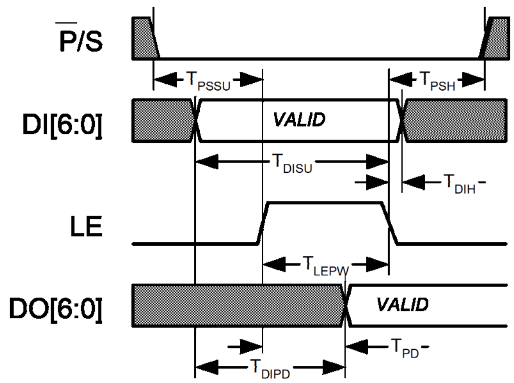


Table 11. Latch and Clock Specifications

Latch Enable	Shift Clock	Function
0	↑	Shift register clocked
↑	X	Contents of shift register transferred to attenuator core

Table 12. Serial Interface AC Characteristics

V_{DD} = 3.4V or 5.0V, –40°C < T_A < 105°C, unless otherwise specified

Parameter	Symbol	Min	Max	Unit
Serial clock frequency	F_{CLK}		10	MHz
Serial clock HIGH time	T_{CLKH}	30		ns
Serial clock LOW time	T_{CLKL}	30		ns
Last serial clock rising edge setup time to Latch Enable rising edge	T_{LESU}	10		ns
Latch enable min. pulse width	T_{LEPW}	30		ns
Serial data setup time	T_{SISU}	10		ns
Serial data hold time	T_{SIH}	10		ns
Parallel data setup time	T_{DISU}	100		ns
Parallel data hold time	T_{DIH}	100		ns
Address setup time	T_{ASU}	100		ns
Address hold time	T_{AH}	100		ns
Parallel/serial setup time	T_{PSSU}	100		ns
Parallel/serial hold time	T_{PSH}	100		ns
Digital register delay (internal)	T_{PD}		10	ns

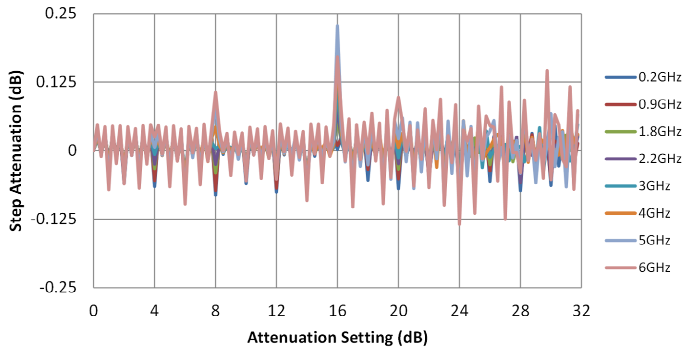
Table 13. Parallel and Direct Interface AC Characteristics

V_{DD} = 3.4V or 5.0V, –40°C < T_A < 105°C, unless otherwise specified

Parameter	Symbol	Min	Max	Unit
Latch enable minimum pulse width	T_{LEPW}	30		ns
Parallel data setup time	T_{DISU}	100		ns
Parallel data hold time	T_{DIH}	100		ns
Parallel/serial setup time	T_{PSSU}	100		ns
Parallel/serial hold time	T_{PSIH}	100		ns
Digital register delay (internal)	T_{PD}		10	ns
Digital register delay (internal, direct mode only)	T_{DIPD}		5	ns

Typical Performance Data, 0.25 dB Step @ 25°C and V_{DD} = 3.3V unless otherwise specified

Figure 6. 0.25 dB Step Attenuation vs. Frequency*



* Monotonicity is held so long as step-attenuation does not cross below –0.25 dB

Figure 7. 0.25 dB Step, Actual vs. Frequency

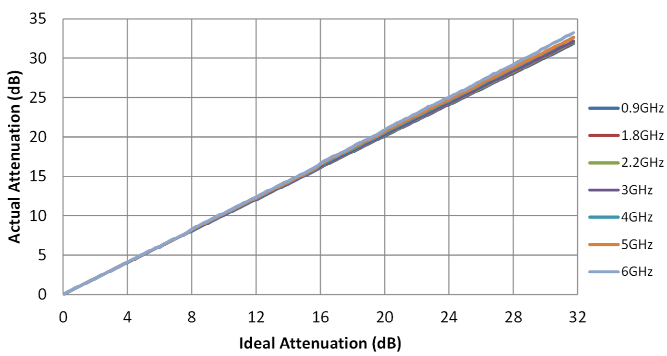


Figure 8. 0.25 dB Major State Bit Error vs. Attenuation Setting

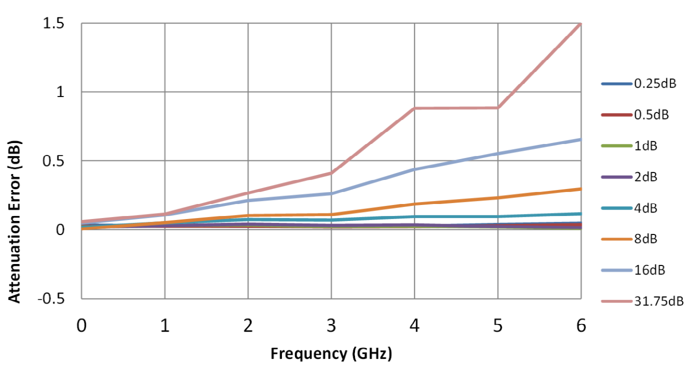
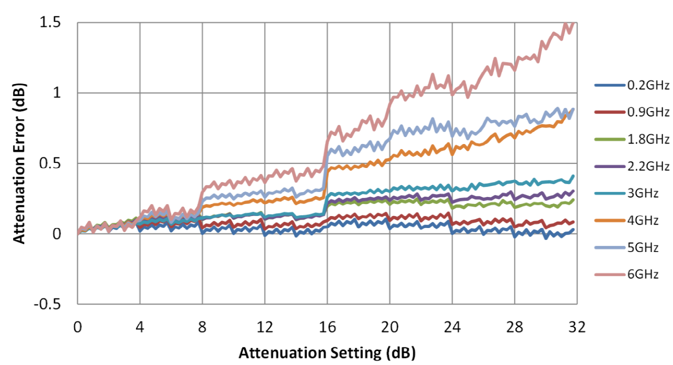
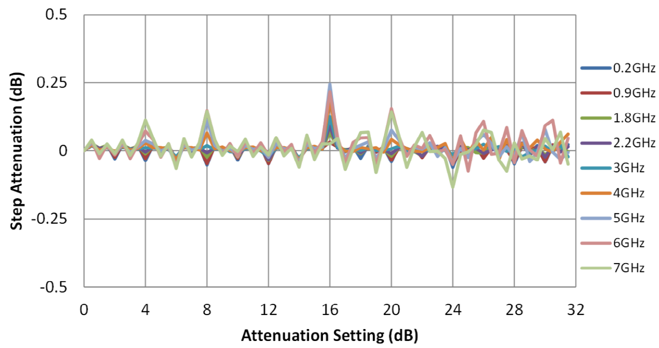


Figure 9. 0.25 dB Attenuation Error vs. Frequency



Typical Performance Data, 0.5 dB Step @ 25°C and V_{DD} = 3.3V unless otherwise specified

Figure 10. 0.5 dB Step Attenuation vs. Frequency*



* Monotonicity is held so long as step-attenuation does not cross below –0.5 dB

Figure 11. 0.5 dB Step, Actual vs. Frequency

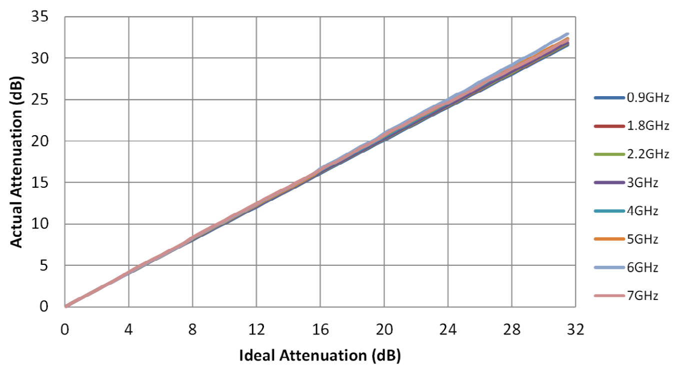


Figure 12. 0.5 dB Major State Bit Error vs. Attenuation Setting

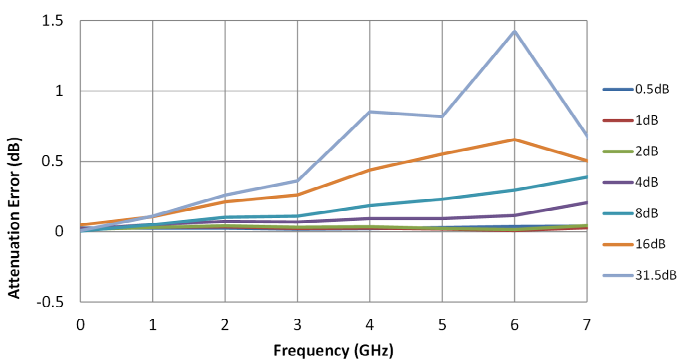
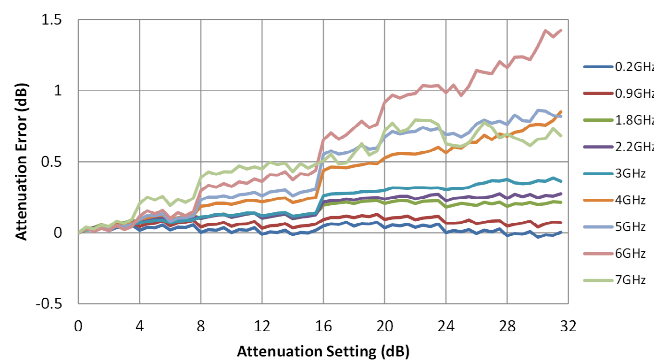
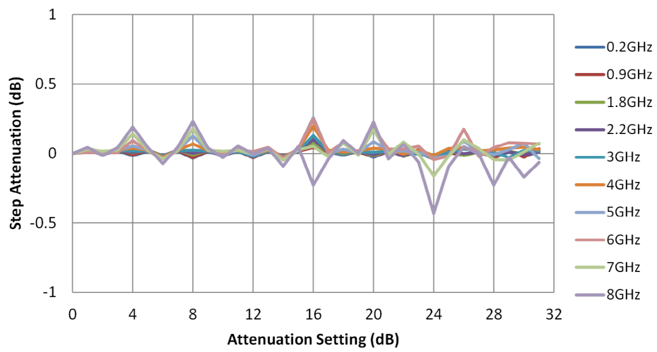


Figure 13. 0.5 dB Attenuation Error vs. Frequency



Typical Performance Data, 1 dB Step @ 25°C and V_{DD} = 3.3V unless otherwise specified

Figure 14. 1 dB Step Attenuation vs. Frequency*



* Monotonicity is held so long as step-attenuation does not cross below –1.0 dB

Figure 15. 1 dB Step, Actual vs. Frequency

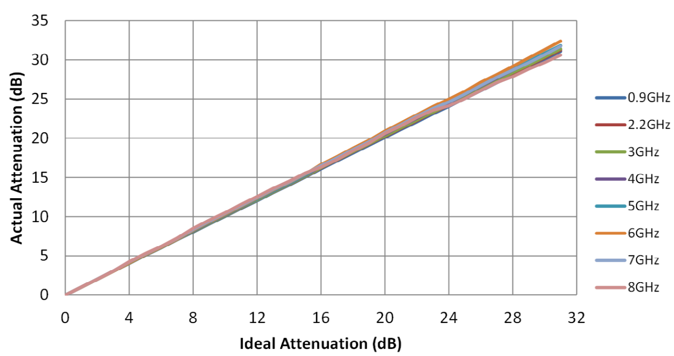


Figure 16. 1 dB Major State Bit Error vs. Attenuation Setting

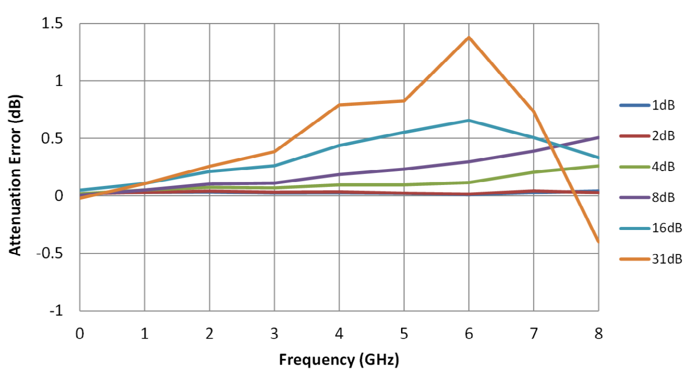
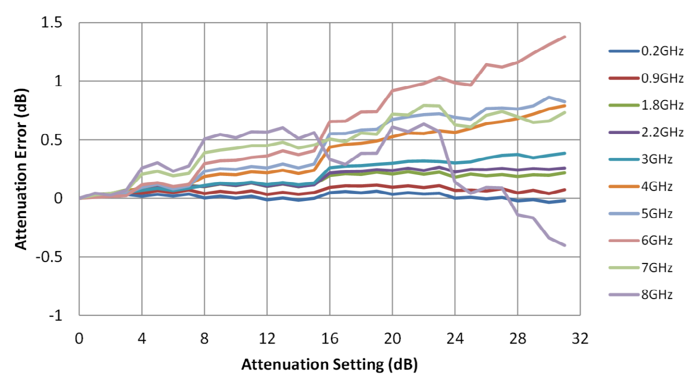


Figure 17. 1 dB Attenuation Error vs. Frequency



Typical Performance Data, 1 dB Step @ 25°C and V_{DD} = 3.3V unless otherwise specified

Figure 18. Insertion Loss vs. Temperature

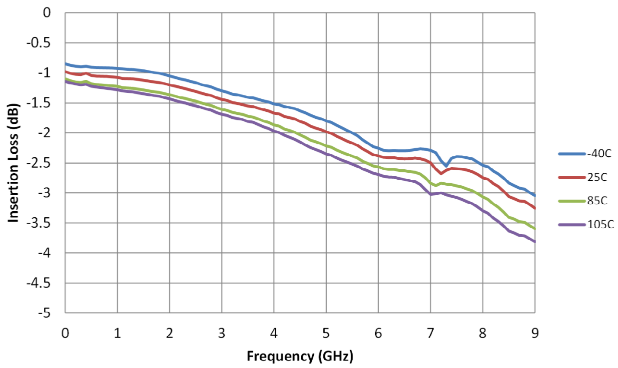


Figure 19. Input Return Loss vs. Attenuation Setting

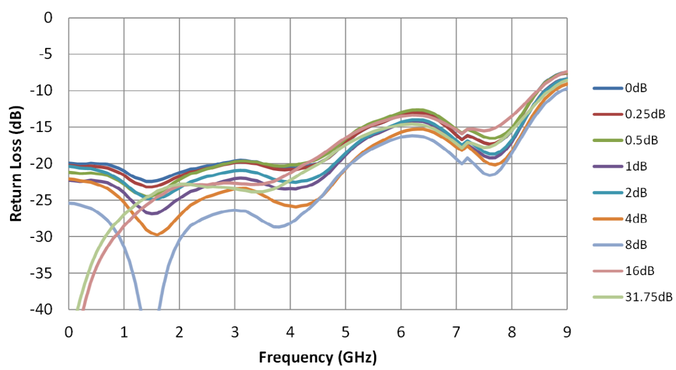


Figure 20. Output Return Loss vs. Attenuation Setting

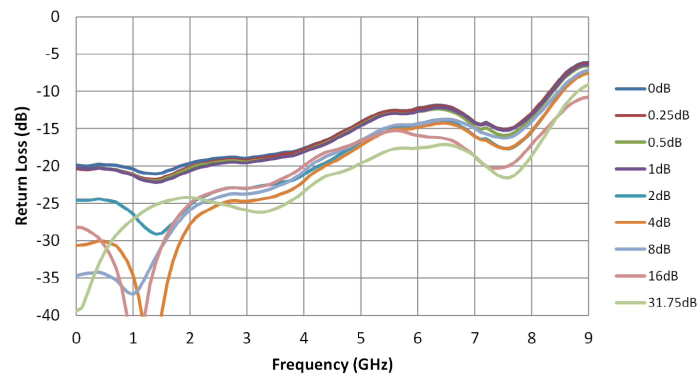


Figure 21. Input Return Loss vs. Temperature for 16 dB Attenuation Setting

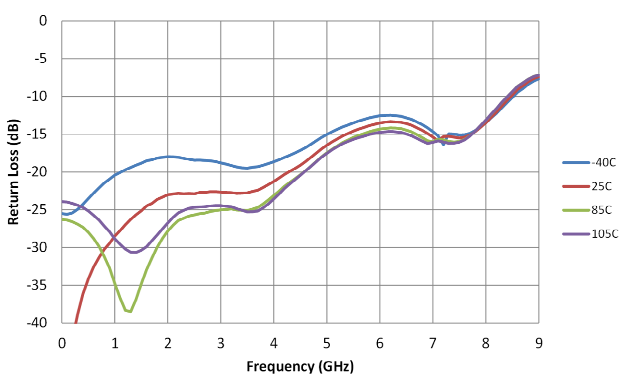
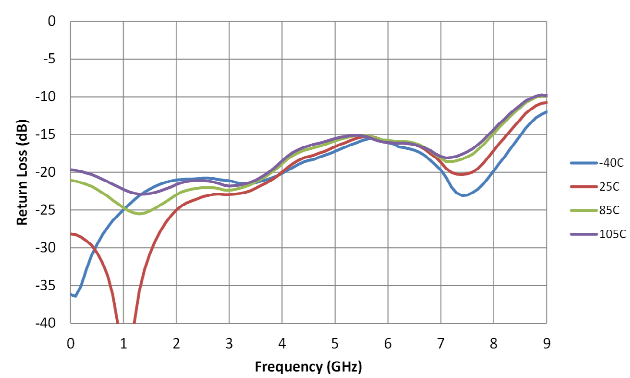


Figure 22. Output Return Loss vs. Temperature for 16 dB Attenuation Setting



Typical Performance Data @ 25°C and V_{DD} = 3.3V unless otherwise specified

Figure 23. Relative Phase Error vs. Attenuation Setting

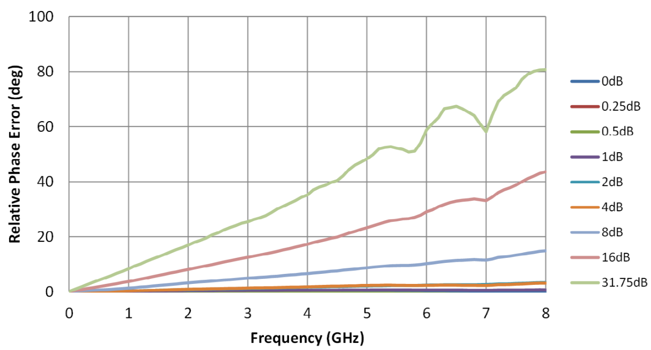


Figure 24. Relative Phase Error for 31.75 dB Attenuation Setting vs. Frequency

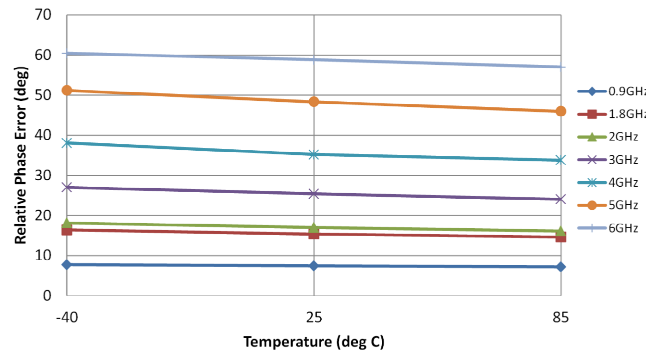


Figure 25. Attenuation Error @ 900 MHz vs. Temperature

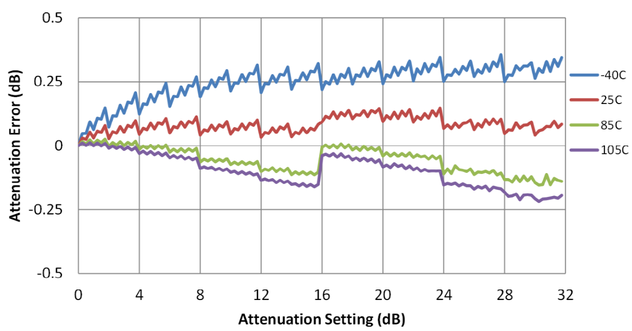


Figure 26. Attenuation Error @ 1800 MHz vs. Temperature

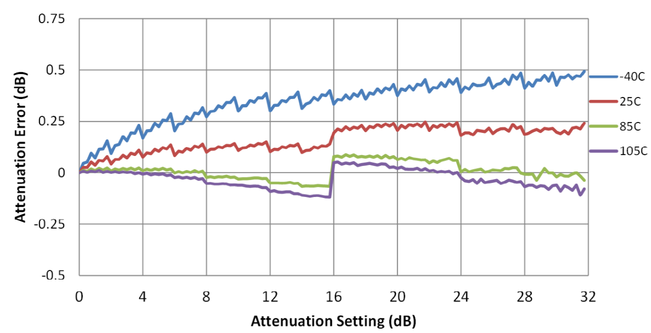


Figure 27. Attenuation Error @ 3000 MHz vs. Temperature

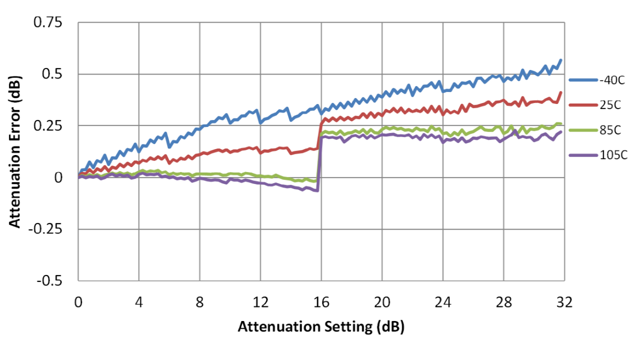
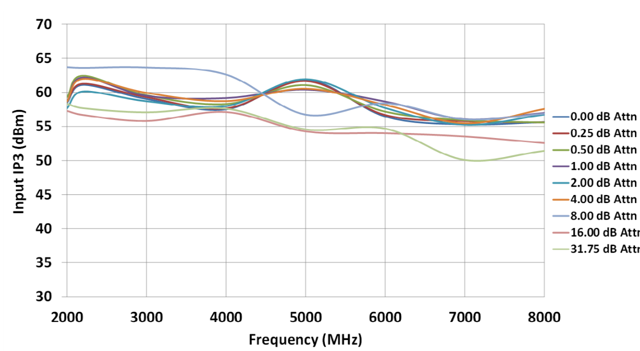


Figure 28. IIP3 vs. Attenuation Setting



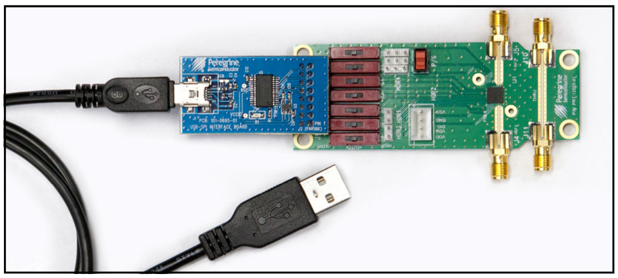
Evaluation Kit

The Digital Attenuator Evaluation Board (EVB) was designed to ease customer evaluation of the PE43705 digital step attenuator. PE43705 EVB supports direct parallel, latched parallel, and serial modes.

Evaluation Kit Setup

Connect the EVB with the USB dongle board and USB cable as shown in *Figure 29*.

Figure 29. Evaluation Kit



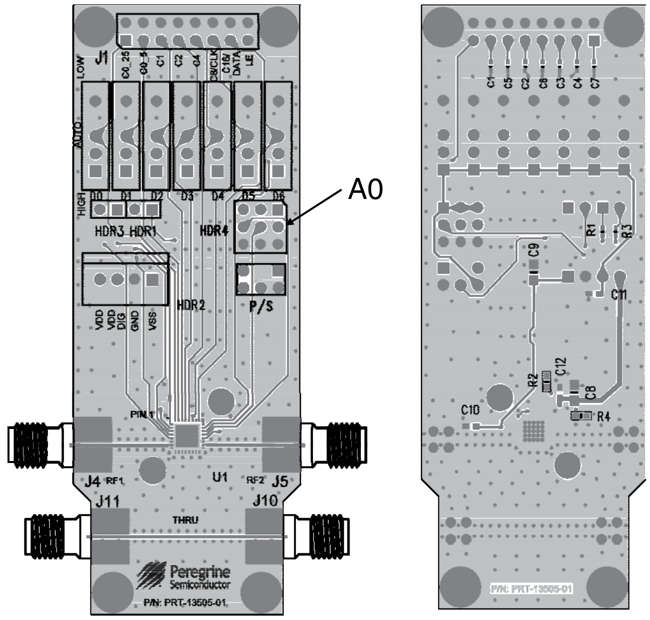
Direct Parallel Programming Procedure

Direct parallel programming is suitable for manual operation without software programming. For manual direct parallel programming, position the parallel/serial (P/S) select switch to the parallel (or left) position. The LE pin of J1 (pin 15) must be tied to HIGH voltage. Switches D0–D6 are SP3T switches that enable the user to manually program the parallel bits. When D0–D6 are toggled to the HIGH position, logic high is presented to the parallel input. When toggled to the LOW position, logic low is presented to the parallel input. Setting D0–D6 to the AUTO position presents as OPEN, which is set for software programming of latched parallel and serial mode. *Table 7* depicts the parallel programming truth table.

Latched Parallel Programming Procedure

For automated latched parallel programming, connect the USB dongle board and cable that is provided with the evaluation kit (EVK) from the USB port of the PC to the J1 header of the PE43705 EVB, and set the D0–D6 SP3T switches to the AUTO position. Position the parallel/serial (P/S) select switch to the parallel (or left) position.

Figure 30. Evaluation Board Layout



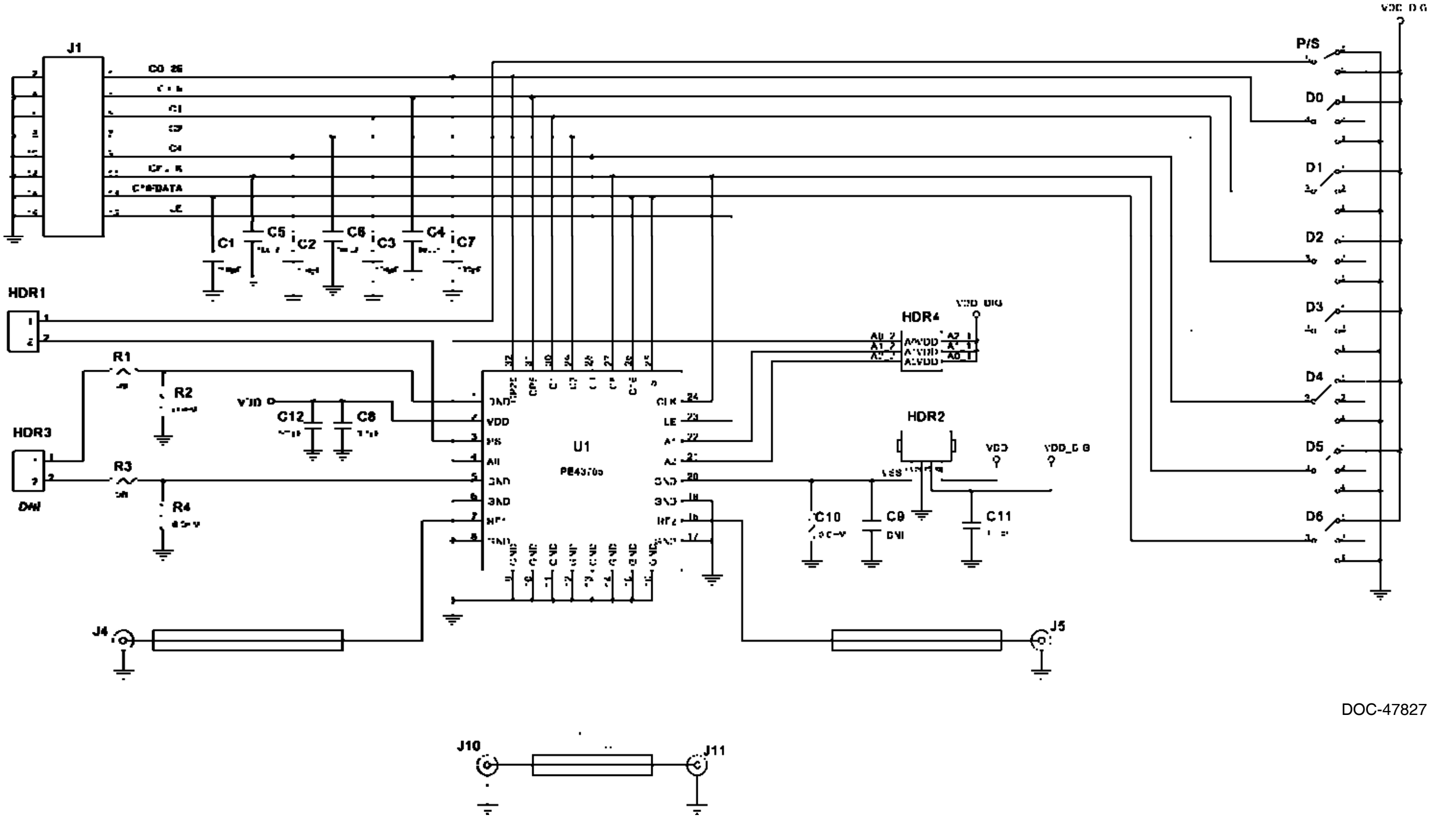
PRT-13505

The evaluation software is written to operate the DSA in parallel mode. Ensure that the software GUI is set to latched parallel mode. Use the software GUI to enable the desired attenuation state. The software GUI automatically programs the DSA each time an attenuation state is enabled.

Serial Addressable Programming Procedure

For automated serial programming, connect the USB dongle board and cable that is provided with the evaluation kit (EVK) from the USB port of the PC to the J1 header of the PE43705 EVB, and set the D0–D6 SP3T switches to the AUTO toggle position. Position the parallel/serial (P/S) select switch to the serial (or right) position. Prior to programming, the user must define an address setting using the HDR4 header pin. Jump the middle row of pins on the HDR4 header (A0–A2) to the lower row of pins to set logic LOW, or jump the middle row of pins to the upper row of pins to set logic HIGH. If the HDR4 pins are left open, then 000 becomes the default address. The software GUI is written to operate the DSA in serial mode. Use the software GUI to enable each setting to the desired attenuation state. The software GUI automatically programs the DSA each time an attenuation state is enabled.

Figure 31. Evaluation Board Schematic



Notes: 1. Use PRT-13505 PCB.
2. CAUTION: Contains parts and assemblies susceptible to damage by electrostatic discharge (ESD).

Figure 32. Package Drawing
32-lead 5x5 QFN

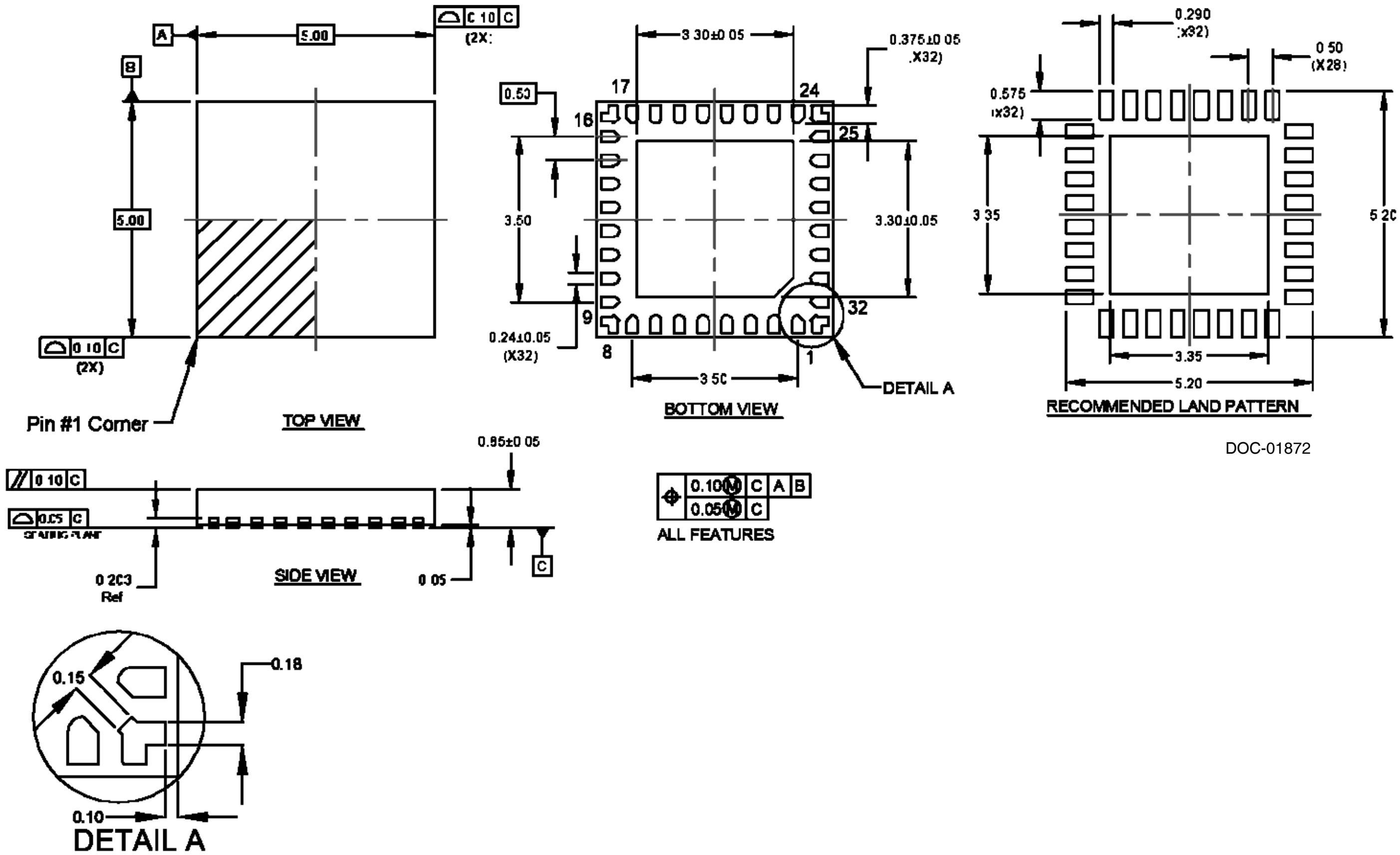
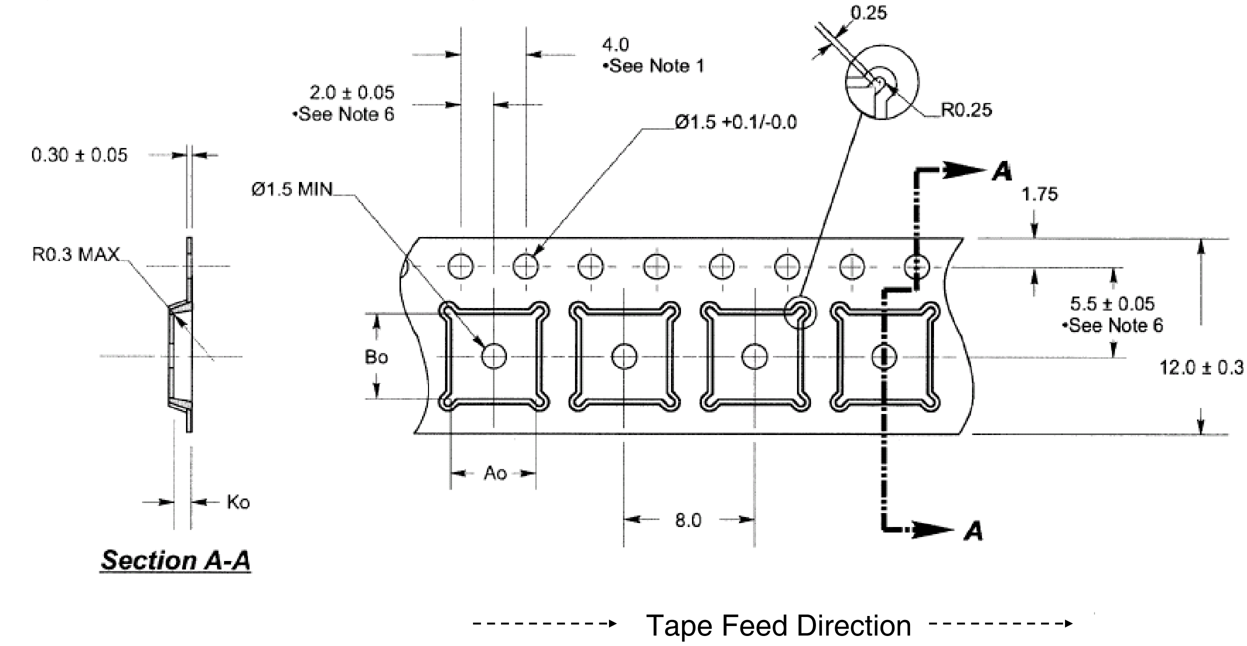


Figure 33. Top Marking Specification

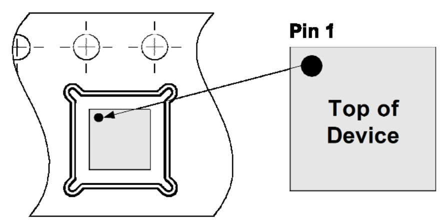
● = Pin 1 designator
YYWW = Date Code, last two digits of the year and work week
ZZZZZZ = Six digits of the lot number

Figure 34. Tape and Reel Drawing



Notes: 1. 10 sprocket hole pitch cumulative tolerance ±.02
2. Camber not to exceed 1 mm in 100 mm
3. Material: PS + C
4. Ao and Bo measured as indicated
5. Ko measured from a plane on the inside bottom of the pocket to the top surface of the carrier
6. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole

Ao = 5.25 mm
Bo = 5.25 mm
Ko = 1.1 mm



Device Orientation in Tape

Table 14. Ordering Information

Order Code	Description	Package	Shipping Method
PE43705B-Z	PE43705 Digital step attenuator	32-lead 5x5 mm QFN	3000 units / T&R
EK43705-12	PE43705 Evaluation kit	Evaluation kit	1 / Box

Sales Contact and Information

For sales and contact information please visit www.psemi.com.