## **FEATURES**

- Max. transparent propagation delay of 900ps
- Min. Master Reset and Enable pulse widths of 100ps
- IEE min. of -98mA
- Industry standard 100K ECL levels
- Extended supply voltage option: VEE = -4.2V to -5.5V
- Voltage and temperature compensation for improved noise immunity
- Internal 75k $\Omega$  input pull-down resistors
- More than 40% faster than Fairchild
- Approximately 30% lower power than Fairchild
- Function and pinout compatible with Fairchild F100K
- Available in 28-pin PLCC package

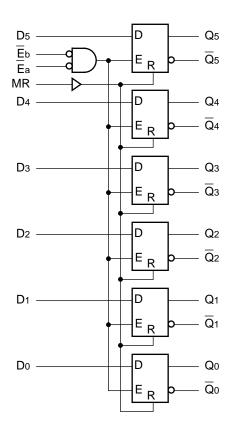
### **PIN NAMES**

Pin	Function					
D0 — D5	Data Inputs					
Ēa, Ēb	Common Enable Inputs (Active LOW)					
MR	Asynchronous Master Reset Input					
Q0 — Q5	Data Outputs					
$\overline{Q}_0 - \overline{Q}_5$	Complementary Data Outputs					
VEES	VEE Substrate					
VCCA	Vcco for ECL Outputs					

## **DESCRIPTION**

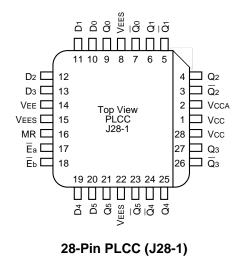
The SY100S350 offers six high-speed D-Latches with both true and complement outputs, and is performance compatible for use with high-performance ECL systems. When both enable signals ( $\overline{E}_a$  and  $\overline{E}_b$ ) are at a logic LOW, the latches are transparent and the input signals( Do–D5) appear at the outputs (Qo–Q5) after a propagation delay. If either or both of the enable signals are at a logic HIGH, then the latches store the last valid data present on its inputs before  $\overline{E}_a$  or  $\overline{E}_b$  went to a logic HIGH. The Master Reset (MR) overrides all other input signals and takes the outputs to a logic LOW state. All inputs have 75k $\Omega$  pull-down resistors.

## **BLOCK DIAGRAM**



M9999-042307 hbwhelp@micrel.com or (408) 955-1690 Micrel, Inc. SY100S350

# **PACKAGE/ORDERING INFORMATION**



**Ordering Information** 

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY100S350JC	J28-1	Commercial	SY100S350JC	Sn-Pb
SY100S350JCTR <sup>(1)</sup>	J28-1	Commercial	SY100S350JC	Sn-Pb
SY100S350JZ <sup>(2)</sup>	J28-1	Commercial	SY100S350JZ with Pb-Free bar-line indicator	Matte-Sn
SY100S350JZTR <sup>(1, 2)</sup>	J28-1	Commercial	SY100S350JZ with Pb-Free bar-line indicator	Matte-Sn

#### Notes:

- 1. Tape and Reel.
- 2. Pb-Free package is recommended for new designs.

# TRUTH TABLE(1)

Each Latch

	Inp	uts		Outp	outs	
Dn	Ēa	Ēb	MR	Qn	Qn	Operating Mode
Н	L	L	L	н	L	Latch
L	L	L	L	L	Н	
X	X	Н	L	Latched <sup>(2)</sup>	Latched <sup>(2)</sup>	
Х	Н	Х	L	Latched <sup>(2)</sup>	Latched <sup>(2)</sup>	
Х	Х	Χ	Н	L	Н	Asynchronous

## NOTES:

- 1. H = HIGH State
  - L = LOW State
  - X = Don't Care
- 2. Retains data that is present before  $\overline{\mathsf{E}}$  positive transition.

# DC ELECTRICAL CHARACTERISTICS

VEE = -4.2V to -5.5V unless otherwise specified; VCC = VCCA = GND

Symbol	Parameter	Min.	Тур.	Max.	Unit	Condition
IIН	Input HIGH Current				μΑ	VIN = VIH (Max.)
	MR	_	_	250		
	Dn	_	_	250		
	Ēa, Ēb	_	_	250		
IEE	Power Supply Current	-98	-78	-49	mA	Inputs Open

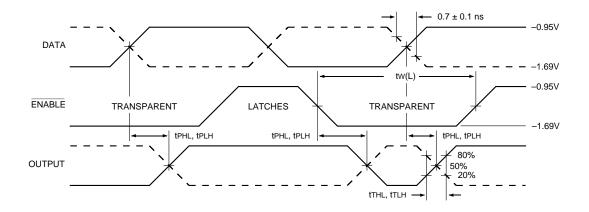
# **AC ELECTRICAL CHARACTERISTICS**

VEE = -4.2V to -5.5V unless otherwise specified; VCC = VCCA = GND

		TA = 0°C		TA = +25°C		TA = +85°C			
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Max.	Unit	Condition
tPLH tPHL	Propagation Delay Dn to Output	300	900	300	900	300	900	ps	
tPLH tPHL	Propagation Delay Ea, Eb to Output	300	1000	300	1000	300	1000	ps	
tPLH tPHL	Propagation Delay MR to Output	300	1200	300	1200	300	1200	ps	
tTLH tTHL	Transition Time 20% to 80%, 80% to 20%	300	900	300	900	300	900	ps	
ts	Set-up Time, Dn to En	500	_	500	_	500	_	ps	
tH	Hold Time, Dn to En	500	_	500	_	500	_	ps	
tr	Release Time, MR to En	1000	_	1000	_	1000	_	ps	
tpw (L)	Pulse Width, Ea, Eb	1000	_	1000	_	1000	_	ps	
tpw (H)	Pulse Width, MR	1000	_	1000	_	1000		ps	

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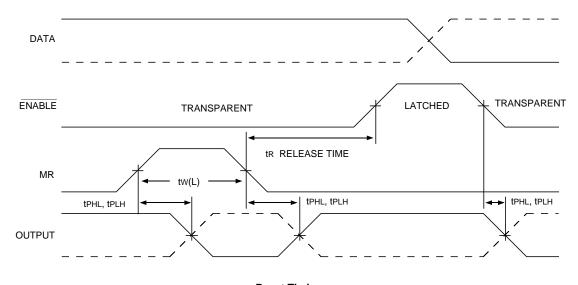
# **TIMING DIAGRAMS**



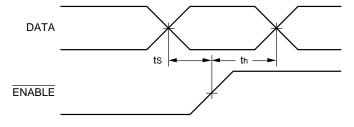
**Enable Timing** 

#### Note:

VEE = -4.2V to -5.5V unless otherwise specified; VCC = VCCA = GND



**Reset Timing** 



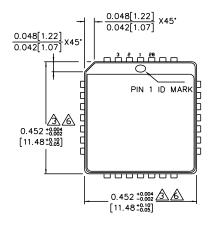
**Data Set-up and Hold Times** 

#### Notes:

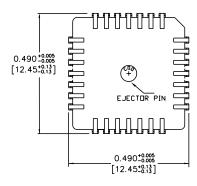
ts is the minimum time before the transition of the clock that information must be present at the data input. the is the minimum time after the transition of the clock that information must remain unchanged at the data input.

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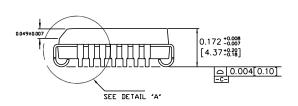
# 28-PIN PLCC (J28-1)



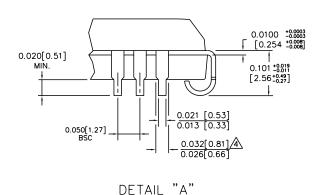
TOP VIEW



BOTTOM VIEW



SIDE VIEW



Rev. A

### NOTES:

DIES:

DIMENSIONS ARE IN INCHES [MM].

CONTROLLING DIMENSION: INCHES.

DIMENSION DOES NOT INCLUDE MOLD FLASH
OR PROTRUSIONS, EITHER OF WHICH SHALL NOT
EXCEED 0.008 [0.203].

LEAD DIMENSION DOES NOT INCLUDE DAMBAR
PROTRUSION.

MAXIMUM AND MINIMUM SPECIFICATIONS ARE
INDICATED AS FOLLOWS: MAX/MIN
PACKACE TOP DIMENSION MAY BE SLICHTLY

PACKAGE TOP DIMENSION MAY BE SLIGHTLY SMALLER THAN BOTTOM DIMENSION.

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