66Watts AEO/ALO25

Total Power: Input Voltages: No. of Outputs:

66 Watts 48V Single

High Efficiency



Special Features

- 2.3" x 0.9" Industry Standard 8th brick outline
- Baseplate or Openframe construction
- Low Ripple and Noise
- Regulation to zero load
- · High Capacitive Load start-up
- Fixed Frequency Switching for EMI predictability
- Industry Standard features: Input UVLO with hysteresis, Enable, OVP, OCP, OTP, Output VoltageTrim, Differential Remote Sense
- Meets Basic Insulation
- EU Directive 2002/95/EC compliant for RoHS

Environmental

Operating Ambient Temperature

Openframe: -40°C to +85°C Ambient Baseplate: -40°C to +100°C Case Storage temperature: -55°C to +125°C MTBF: > 1 Million Hrs

Safety

UL, cUL 60950-1 Recognized TUV EN60950-1 Licensed

Electrical Specs

Input Range Input Surge Input UVLO

Efficiency²

Output

Line / Load Regulation Load Current Noise/Ripple¹ Transient Response

Over Voltage Protection Over Current Protection Over Temperature Protection Switching Frequency Isolation Voltage

Control

Output Voltage Trim Enable 36 to 75 VDC 100V /100ms 33 - 36 V (UVLO ON) 31 - 34 V (UVLO OFF) 93% @ 5 V (typical)

< 0.1% V_O (typical) Up to 25A for Vo \leq 1.8V 20mV_{PK-PK} (typical for Vo \leq 2.5V) 2% typical deviation (50% to 75% Step Load) < 100µs settling time (typ) 130% V_O Typ (autorecovery) 130% $I_{O,max}$ Typ (autorecovery) 115°C average PCB temperature (autorecovery) Fixed Frequency 1500Vdc

±10% V_{O,NOM} TTL compatible (Positive or Negative Logic)



2

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ASIA



Ordering Information

Input Voltage	Output Voltage	Output Current	Efficiency ²	Model Number
36V to 75V	12.0V	4A	93.0%	A(X)O04B48(N) - (6)(S)(L)
36V to 75V	5.0V	12A	92.0%	A(X)O12A48(N) - (6)(S)(L)
36V to 75V	3.3V	20A	91.0%	A(X)O20F48(N) - (6)(S)(L)
36V to 75V	2.5V	25A	90.0%	A(X)O20G48(N) - (6)(S)(L)
36V to 75V	1.8V	25A	88.5%	A(X)O25Y48(N) - (6)(S)(L)
36V to 75V	1.5V	25A	86.5%	A(X)O25M48(N) - (6)(S)(L)
36V to 75V	1.2V	25A	85.5%	A(X)O25K48(N) - (6)(S)(L)

OPTIONS:

(X) : "L" = Open Frame / Low Profile

"E" = Baseplate Construction

(N) : "N" = designates Negative Logic Enable (default is Positive Enable with no suffix "N" required)

(6) : "-6" = 3.7mm nominal pin length (default is 5mm nominal pin length with no suffix "-6" required)

(S) : "-S" = Surface Mount Termination (default is Through Hole Termination with no suffix "-S" required)⁷

(L) : "L" = RoHS compliant (RoHS 6) / "Blank" - RoHS compliant with Lead (PB) in solder exemption (RoHS 5)

Pin Assignment

Single Output

1. +Vin

- 2. Enable (On/Off)
- 3. -Vin
- 4. V_{OUT}
- 5. -Sense
- 6. Trim
- 7. +Sense
- 8. +V_{OUT}

Notes:

- 1. Measured at 20 MHz bandwidth with external 10 μ F tant. capacitor in parallel with 0.1 μ F ceramic capacitor connected across +Vout and -Vout; 220 μ F e-cap or equivalent connected across +Vin and -Vin.
- 2. Efficiency measurements taken at full load, nominal line and $T_{\mbox{\scriptsize A}}$ = 25°C.
- 3. All specifications are typical at nominal line, full load and $T_A = 25^{\circ}C$ unless otherwise noted.
- 4. All specifications subject to change without notice.
- Mechanical drawings are for reference only. Dimensions are in inches [mm]. Pin placement tolerance ± 0.005 [0.127]. Mechanical Tolerance ± 0.02 [0.5], recommended surface mount pads (min: 0.080 x 0.112 [2.03 x 2.84] / max: 0092 x 0.124 [2.34 x 3.15]); through hole pin diameter (Pins 4 & 8) Ø = 0.062 [1.57], others Ø = 0.04 [1.0] (6X).
- 6. Technical Reference Notes should be consulted for detailed information when available.
- 7. AEOxxxxx-Sx series (surface mount terminated with baseplate) are not reflow compatible.
- 8. Warranty 2 yrs.

Astec reserves the right to make changes to the information contained herein without notice and assumes no liability as a result of its use and application. (REV 02: MARCH 7, 2007).



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