Keywords: Jitter, Wander, G.703, Timing Unit, Jitter Attenuator, E1

APPLICATION NOTE 6352

DESIGN CONSIDERATIONS FOR USING THE DS26504 JITTER ATTENUATOR

Abstract: How to use DS26504 Jitter Attenuator to avoid phase slip and wander.

Overview

Building integrated timing supply (**BITS**) is one type of clock used extensively in network synchronization. It is a master timing supply for all deployed equipment within a network that requires synchronization. DS26504 is a BITS clock-recovery element that can be used in these applications. The receiver portion of this device can recover a clock from T1, E1, 64kHz composite clock (64KCC), and 6312kHz synchronization timing interfaces.

One of the important blocks of DS26504 is its Jitter Attenuator which operates without a dedicated crystal and uses MCLK for its operation. A crystal-less jitter attenuator with bypass mode for T1 and E1 operation is included in DS26504.

The jitter attenuator as show in **Figure 1** can be inserted either in the transmit or receive path.

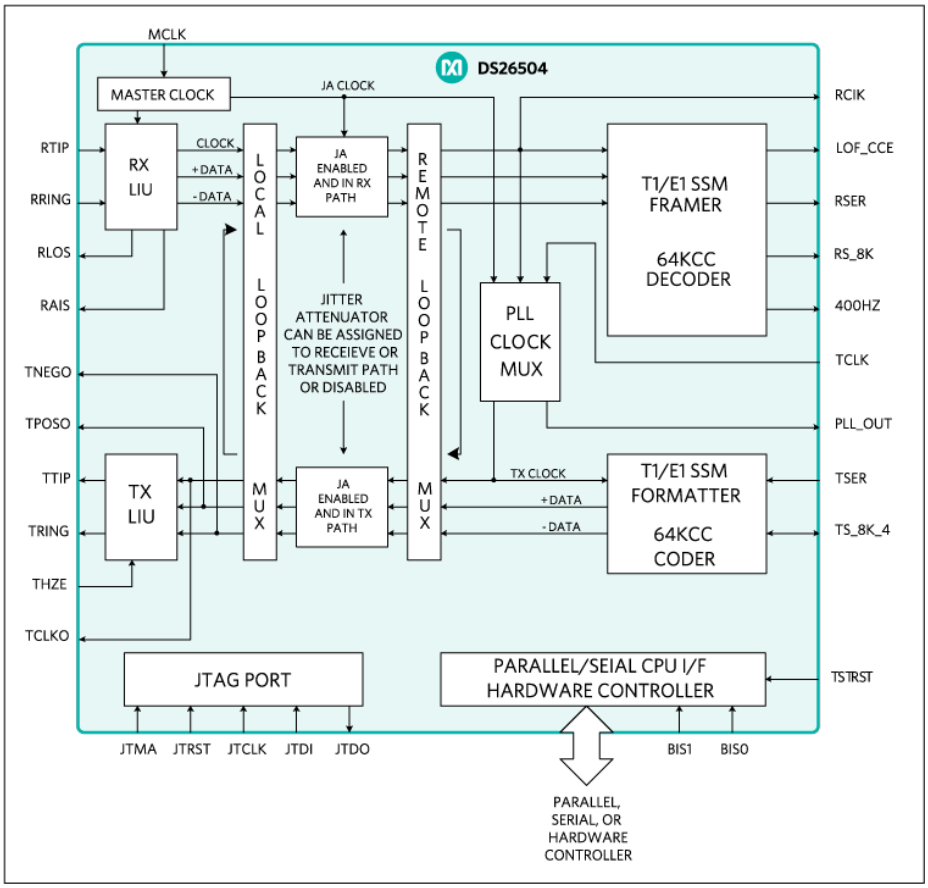

Figure 1. DS26504 block diagram.

Register line interface control 1 (LIC1) (**Figure 2**) allows the customer to select the position of the jitter attenuator (either in Rx or Tx path) and switch the jitter attenuator on or off. Moreover, the jitter attenuator can be set to a depth of either 32 bits or 128 bits through the JABDS bit (LIC1.2). The 128-bit mode is used in applications where large excursions of wander are expected. The 32-bit mode is used in delay-sensitive applications.

Register Name: LIC1
Register Description: Line Interface Control 1
Register Address: 30h

Bit #	7	6	5	4	3	2	1	0
Name	L2	L1	L0	EGL	JAS	JABDS	DJA	TPD
Default	0	0	0	0	0	0	0	0
HW Mode	L2 PIN 13	L1 PIN 12	L0 PIN 11	0	0	0	0	1

Bit 0: Transmit Power-Down (TPD)
0 = powers down the transmitter and three-states the TTIP and TRING pins
1 = normal transmitter operation

Bit 1: Disable Jitter Attenuator (DJA)
0 = jitter attenuator enabled
1 = jitter attenuator disabled

Bit 2/Jitter Attenuator Buffer Depth Select (JABDS)
0 = 128 bits
1 = 32 bits (use for delay-sensitive applications)

Bit 3: Jitter Attenuator Select (JAS)
0 = place the jitter attenuator on the receive side
1 = place the jitter attenuator on the transmit side

Figure 2. Register-line interface Control 1 description.

Note that Physical and electrical characteristics of hierarchical digital interfaces in Figure 2 are defined in G.703 ITU synchronization standard.

In this application note, as shown in **Figure 3**, the DS26504 input signal is indicated as G.703, the master clock for DS26504 is named as MCLK, and the recovered clock from incoming signal is named as RCLK.

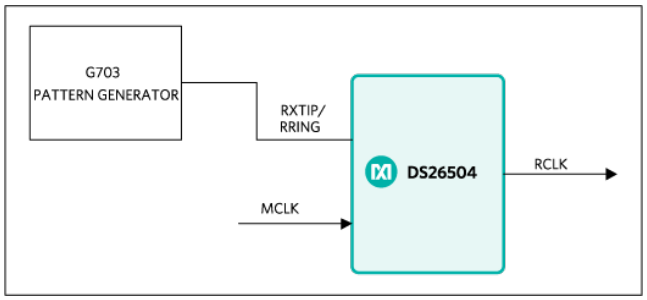

Figure 3. DS26504 system block diagram.

Jitter Attenuator Operation

The jitter attenuator inside DS26504 uses a constant average delay architecture. This means that the difference in frequency between the input clock and the master clock (MCLK) causes the jitter attenuator to select a discrete delay for the output clock. The output-clock delay occurs in 1 UI steps, which happens with every 2ppm of frequency difference. Since the master clock input is normally derived from a crystal oscillator (XO), the master clock frequency shifts with changes in temperature. If the temperature change is large enough, the frequency difference reaches a point where the output clock (RCLK) shifts 1 UI.

In this condition, as show in **Figure 4**, the recovery clock (RCLK) unlocks and locks again, which can be called 'phase slip,' every 2ppm of frequency difference. The same phenomenon occurs if the master clock frequency is stable and the frequency of the input signal changes.

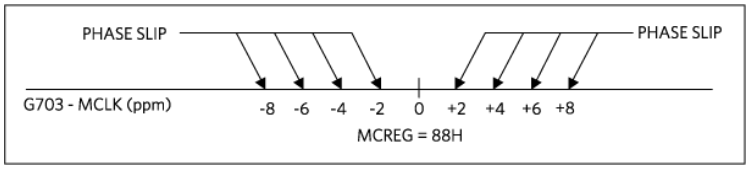

Figure 4. Frequency difference between G.703 and MCLK produce phase slip on RCLK.

In applications such as timing units for telecommunications equipment where system can be synchronized to incoming G.703 signal, BITS input could be disqualified when phase slip occurs and errors are introduced in data communications.

Additionally, if this phase slip occurs during maximum time interval error (MTIE) and time deviation (t_{DEV}) measurements where an observation time up to 20min is used, the tests FAIL.

Thus, it is recommended to keep jitter attenuator off in timing unit applications considering also that jitter cleaning can be managed from the second PLL following BITS, which is generally used in this application to manage other synchronization sources (see **Figure 5**).

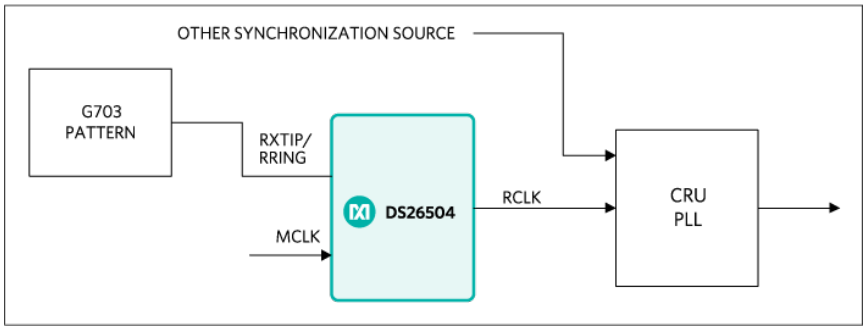

Figure 5. DS26504 in a typical timing unit application.

When the jitter attenuator is not used, due to the input-signal sampling, the recovered signal is affected from high-frequency jitter measured to be in the range of 62.4ns (see **Figure 6**).

Figure 6. High frequency jitter on recovered clock (RCLK) when frequency difference between G.703 and MCLK is greater than 1Hz.

Very small frequency differences, in the range of 1Hz (0.5ppm), between G.703 and MCLK, as show in **Figure 7**, introduces wander (low frequency jitter) on RCLK.

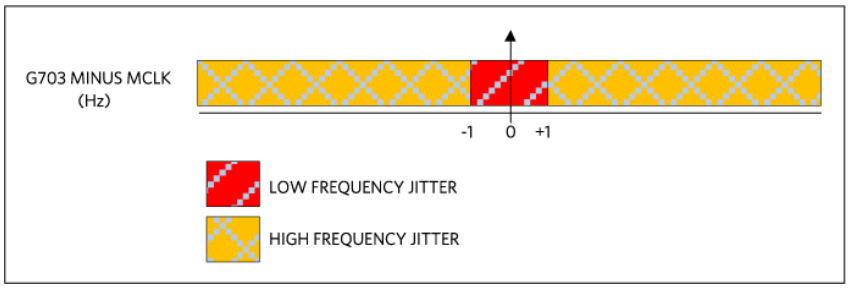

Figure 7. Jitter type change according to frequency difference between G.703 and MCLK.

While the high frequency jitter can be easily removed from the subsequent PLL, its bandwidth is not low enough to remove the wander.

In this corner condition, wander affecting RCLK can produce a failure during maximum time interval error (MTIE) and time deviation (t_{DEV}) tests.

This condition can be avoided by selecting as master clock (MCLK) a signal with a frequency above the expected range of incoming signal. For example, as show in **Figure 8**, assuming an incoming signal of 2.048MHz ±5ppm, to avoid wander the master clock can be selected as 2.048MHz + 15ppm.

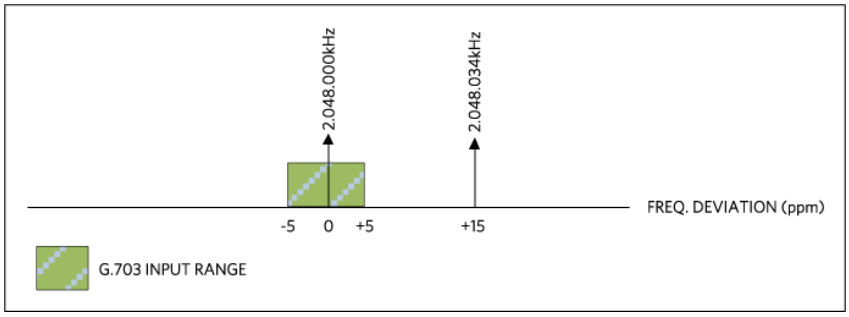

Figure 8. MCLK frequency selection according input signal range can avoid wander on RCLK.

With this arrangement, RCLK is affected from high-frequency jitter that can be easily removed from PLL-following BITS.

Conclusion

- In timing unit application, it is recommended to keep jitter attenuator off to avoid the phase slip described above.
- To avoid wander, with jitter attenuator off, the frequency difference between the G.703 signal and master clock (MCLK) must be larger than 1Hz.

Related Parts		
DS26504	T1/E1/J1/64KCC BITS Element	Free Samples

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