ams AG
Tobelbader Strasse 30
8141 Premstaetten
Austria

T +43 3136 500-0
F +43 3136 525-01
info@ams.com
www.ams.com

Premstaetten, October 20, 2016

Subject: Product Change Notification PCN24-2016
Performance Improvement AS3955

Dear valued customer,

At ams we strive to ship highest quality products with optimized cost/yield factors. We have fixed two issues which affect Power Mode 0 only. Fix a): we have reduced the standby current in Power mode 0. Fix b): we have removed instability at start-up when AS3955 is powered up using the /SS line in Power mode 0.

We have corrected both issues by redesign and will update our production accordingly.
The fixes do not require any modification in system circuitry and design.

1. Reason for redesign Issue a): high current in standby mode in Power mode 0

When the AS3955 is used in low power applications, most commonly Power mode 0 is used. This means that the chip is not always powered when there is no RF field and /SS line is set to HIGH. The state where the AS3955 is not in the RF field and the /SS line is set high is a stand-by mode. During stand-by mode the current drawn from the external supply should be in the nA range.

The problem identified in stand-by mode is: due to a floating node in a block that enables switching of the supply for the digital block in test mode, additional current is drawn from external supply. This can result in the maximum standby current in Power mode 0 being exceeded.

2. Reason for redesign Issue b): Powering up using /SS line in in Power mode 0

The issue that may appear during powering up the AS3955 by pulling the /SS line low in Power mode 0 is that the AS3955 might not start. In this case, a Power-up IRQ is not triggered and the communication with AS3955 via SPI/I2C is not possible. The reason for this is a problem with the reset of a clock switch between two different clock sources. The result is that the chip is not always powered up when /SS line is pulled low and the Power-up IRQ is not triggered.

Corrective action:
The floating node causing issue a) has been eliminated. The reset of the clock switch block, causing issue b) has been corrected.
The changes have been applied with the following new versions:
AS3955A-ATDM
AS3955A-ATDT
AS3955A-AWLT
AS3955A-ASWF
AS3955A-ATWT

These improved versions will replace the existing versions AS3955-ATDM, AS3955-ATDT, AS3955-AWLT, AS3955-ASWF, AS3955-ATWT

Verification / Qualification of the redesign:

- Lab verification
- ATE verification (prior and during mass production)

Affected ordering codes:
AS3955-ATDM
AS3955-ATDT
AS3955-AWLT
AS3955-ASWF
AS3955-ATWT

Timing of change:
November 2016

We apologize for any inconvenience caused by ams AG. If you do have further questions please do not hesitate to contact us.

Please be advised that, unless we receive your written refusal concerning this PCN within 30 days, the PCN shall be deemed accepted.

Best regards,

ams AG
H. Pessl
Director of Operations
Wireless Connectivity & Power management