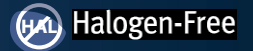# EPC2108 – Enhancement-Mode GaN Power Transistor Half-Bridge with Integrated Synchronous Bootstrap

V_{DS} , 60 V
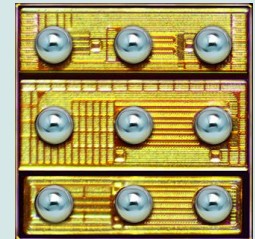
$R_{DS(on)}$, 240 mΩ

I_D , 1.7 A

EPC

EFFICIENT POWER CONVERSION

RoHS Halogen-Free

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR}. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

EPC2108 eGaN® ICs are supplied only in passivated die form with solder bumps
Die Size: 1.35 mm x 1.35 mm

Applications
• High Frequency DC-DC Conversion
• Class-D Audio
• Wireless Power
  (Highly Resonant and Inductive)

Benefits
• Ultra High Efficiency
• Ultra Low $R_{DS(on)}$
• Ultra Low Q_G
• Ultra Small Footprint

DEVICE	\multicolumn{2}{c}{Maximum Ratings}		VALUE	UNIT

DEVICE	PARAMETER		VALUE	UNIT
Q1 & Q2	V_{DS}	Drain-to-Source Voltage (Continuous)	60	V
		Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	72	
	I_D	Continuous (T_A = 25°C, $R_{\theta JA}$ = 60°C/W)	1.7	A
		Pulsed (25°C, T_{PULSE} = 300 μs)	5.5	
	V_{GS}	Gate-to-Source Voltage	6	V
		Gate-to-Source Voltage	−4	
	T_J	Operating Temperature	−40 to 150	°C
	T_{STG}	Storage Temperature	−40 to 150	
Q3	V_{DS}	Drain-to-Source Voltage (Continuous)	100	V
		Drain-to-Source Voltage (up to 10,000 5 ms pulses at 150°C)	120	
	I_D	Continuous (T_A = 25°C, $R_{\theta JA}$= 100°C/W)	0.5	A
		Pulsed (25°C, T_{PULSE} = 300 μs)	0.5	
	V_{GS}	Gate-to-Source Voltage	6	V
		Operating Temperature	−40 to 150	
	T_J	Storage Temperature	−40 to 150	°C
	T_{STG}	Storage Temperature	−40 to 150	

Thermal Characteristics	

	PARAMETER	TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	6	
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board	33	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	81	

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.
See https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details
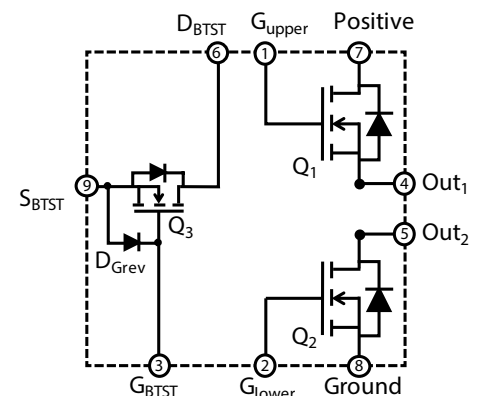
EPC2108 – Detailed Schematic

Static Characteristics (T$_J$= 25°C unless otherwise stated)							
DEVICE	**PARAMETER**		**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
Q1 & Q2	BV$_{DSS}$	Drain-to-Source Voltage	V$_{GS}$ = 0 V, I$_D$ = 0.3 mA	60			V
	I$_{DSS}$	Drain-Source Leakage	V$_{DS}$ = 48 V, V$_{GS}$ = 0 V		0.05	0.25	mA
	I$_{GSS}$	Gate-to-Source Forward Leakage	V$_{GS}$ = 5 V		0.1	1	mA
		Gate-to-Source Reverse Leakage	V$_{GS}$ = -4 V		0.05	0.25	mA
	V$_{GS(TH)}$	Gate Threshold Voltage	V$_{DS}$ = V$_{GS}$, I$_D$ = 0.2 mA	0.8	1.6	2.5	V
	R$_{DS(on)}$	Drain-Source On Resistance	V$_{GS}$ = 5 V, I$_D$ = 2.5 A		150	240	mΩ
	V$_{SD}$	Source-Drain Forward Voltage	I$_S$ = 0.5 A, V$_{GS}$ = 0 V		2.6		V
Q3	BV$_{DSS}$	Drain-to-Source Voltage	V$_{GS}$ = 0 V, I$_D$ = 0.125 mA	100			V
	I$_{DSS}$	Drain-Source Leakage	V$_{DS}$ = 80 V, V$_{GS}$ = 0 V		0.02	0.1	mA
	I$_{GSS}$	Gate-to-Source Forward Leakage	V$_{GS}$ = 5 V		0.1	1	mA
	V$_F$	Source-Gate Forward Voltage	I$_F$ = 0.2 mA, V$_{DS}$ = 0 V			2.7	V
	V$_{GS(TH)}$	Gate Threshold Voltage	V$_{DS}$ = V$_{GS}$, I$_D$ = 0.1 mA	0.8	1.7	2.5	V
	R$_{DS(on)}$	Drain-Source On Resistance	V$_{GS}$ = 5 V, I$_D$ = 0.05 A		2100	3300	mΩ
	V$_{SD}$	Source-Drain Forward Voltage	I$_S$ = 0.1 A, V$_{GS}$ = 0 V		2.9		V

Dynamic Characteristics (T$_J$= 25°C unless otherwise stated)							
DEVICE	**PARAMETER**		**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
Q1	C$_{ISS}$	Input Capacitance	V$_{DS}$ = 30 V, V$_{GS}$ = 0 V		26	31	pF
	C$_{RSS}$	Reverse Transfer Capacitance			0.4		
	C$_{OSS}$	Output Capacitance			12	18	
	C$_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 2)	V$_{DS}$ = 0 to 30 V, V$_{GS}$ = 0 V		20		
	C$_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 3)			24		
	R$_G$	Gate Resistance			0.6		Ω
	Q$_G$	Total Gate Charge	V$_{DS}$ = 30 V, V$_{GS}$ = 5 V, I$_D$ = 2.5 A		240	310	pC
	Q$_{GS}$	Gate to Source Charge			106		
	Q$_{GD}$	Gate to Drain Charge	V$_{DS}$ = 50 V, I$_D$ = 2.5 A		47		
	Q$_{G(TH)}$	Gate Charge at Threshold			71		
	Q$_{OSS}$	Output Charge	V$_{DS}$ = 30 V, V$_{GS}$ = 0 V		710	1070	
	Q$_{RR}$	Source-Drain Recovery Charge			0		
Q2	C$_{ISS}$	Input Capacitance	V$_{DS}$ = 30 V, V$_{GS}$ = 0 V		26	31	pF
	C$_{RSS}$	Reverse Transfer Capacitance			0.4		
	C$_{OSS}$	Output Capacitance			16	24	
	C$_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 2)	V$_{DS}$ = 0 to 30 V, V$_{GS}$ = 0 V		25		
	C$_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 3)			31		
	R$_G$	Gate Resistance			0.6		Ω
	Q$_G$	Total Gate Charge	V$_{DS}$ = 30 V, V$_{GS}$ = 5 V, I$_D$ = 2.5 A		240	310	pC
	Q$_{GS}$	Gate to Source Charge			106		
	Q$_{GD}$	Gate to Drain Charge	V$_{DS}$ = 30 V, I$_D$ = 2.5 A		47		
	Q$_{G(TH)}$	Gate Charge at Threshold			71		
	Q$_{OSS}$	Output Charge	V$_{DS}$ = 30 V, V$_{GS}$ = 0 V		930	1400	
	Q$_{RR}$	Source-Drain Recovery Charge			0		
Q3	C$_{ISS}$	Input Capacitance	V$_{DS}$ = 50 V, V$_{GS}$ = 0 V		7	8.4	pF
	C$_{RSS}$	Reverse Transfer Capacitance			0.02		
	C$_{OSS}$	Output Capacitance			1.6	2.4	
	C$_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 2)	V$_{DS}$ = 0 to 50 V, V$_{GS}$ = 0 V		2.2		
	C$_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 3)			2.7		
	R$_G$	Gate Resistance			4.8		Ω
	Q$_G$	Total Gate Charge	V$_{DS}$ = 50 V, V$_{GS}$ = 5 V, I$_D$ = 0.05 A		44	55	pC
	Q$_{GS}$	Gate to Source Charge			20		
	Q$_{GD}$	Gate to Drain Charge	V$_{DS}$ = 50 V, I$_D$ = 0.05 A		4		
	Q$_{G(TH)}$	Gate Charge at Threshold			18		
	Q$_{OSS}$	Output Charge	V$_{DS}$ = 50 V, V$_{GS}$ = 0 V		134	200	
	Q$_{RR}$	Source-Drain Recovery Charge			0		

Note 2: C$_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C$_{OSS}$ while V$_{DS}$ is rising from 0 to 50% BV$_{DSS}$.
Note 3: C$_{OSS(ER)}$ is a fixed capacitance that gives the same charging time as C$_{OSS}$ while V$_{DS}$ is rising from 0 to 50% BV$_{DSS}$.

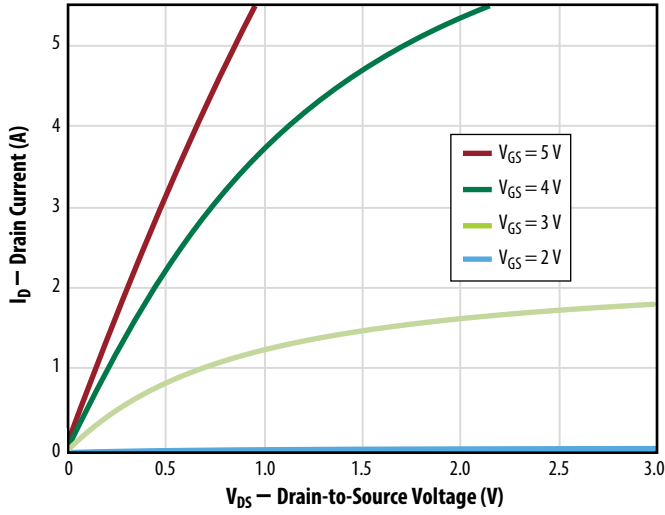**Figure 1a (Q1 & Q2): Typical Output Characteristics at 25°C**

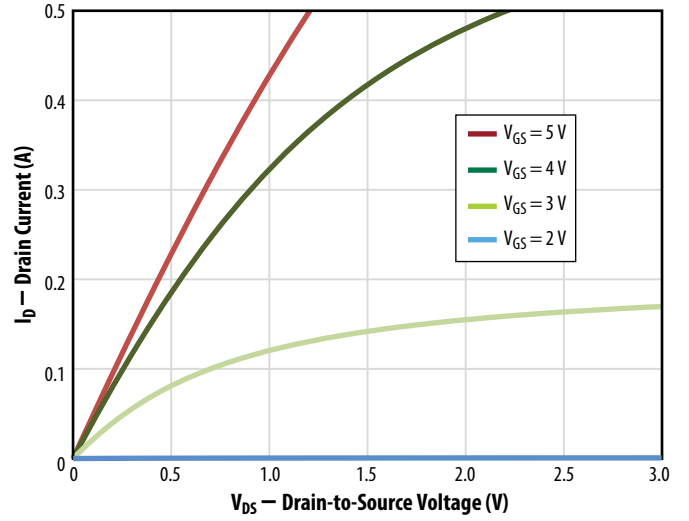**Figure 1b (Q3): Typical Output Characteristics at 25°C**
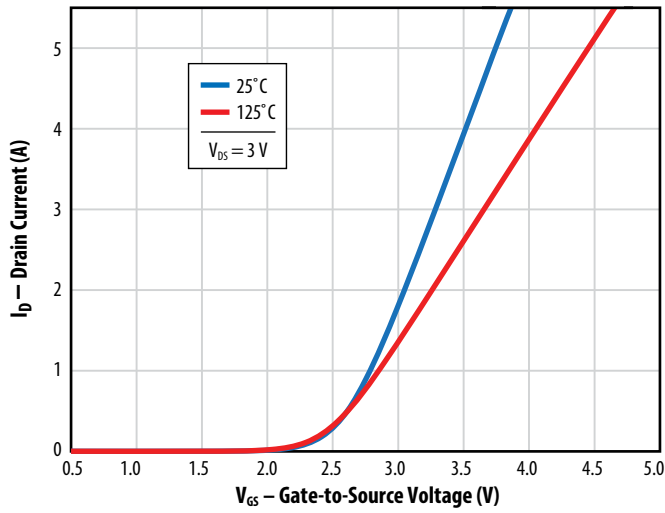

Figure 2a (Q1 & Q2): Transfer Characteristics
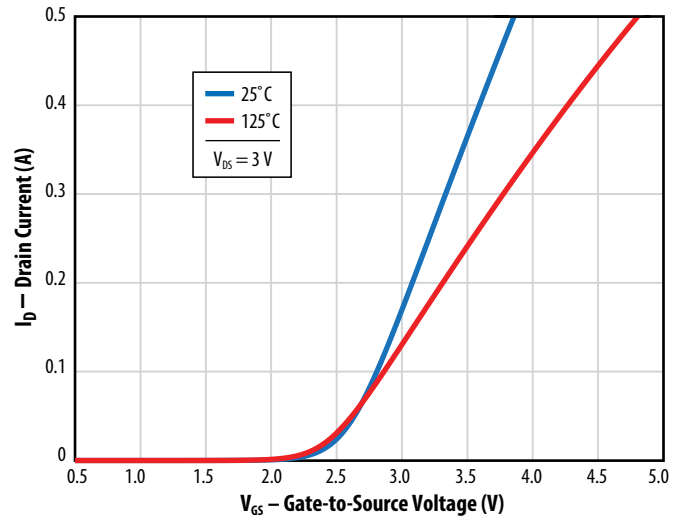

Figure 2b (Q3): Transfer Characteristics

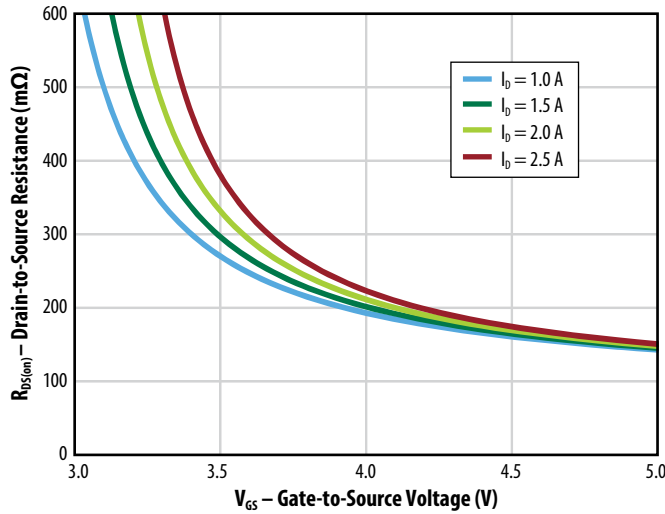**Figure 3a (Q1 & Q2): $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents**

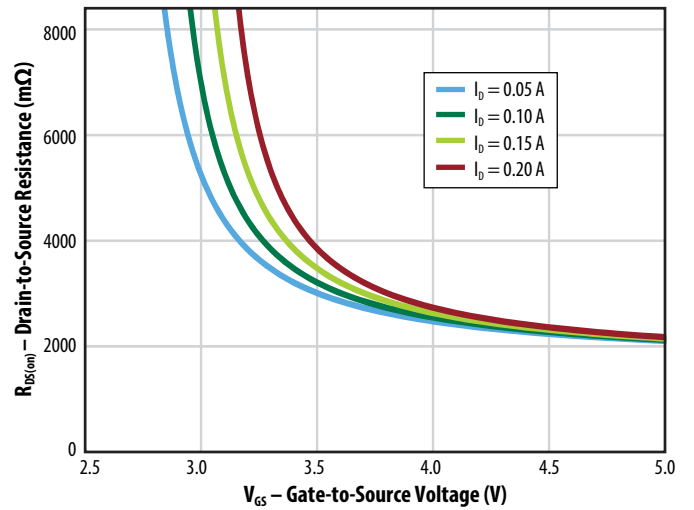**Figure 3b (Q3): $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents**

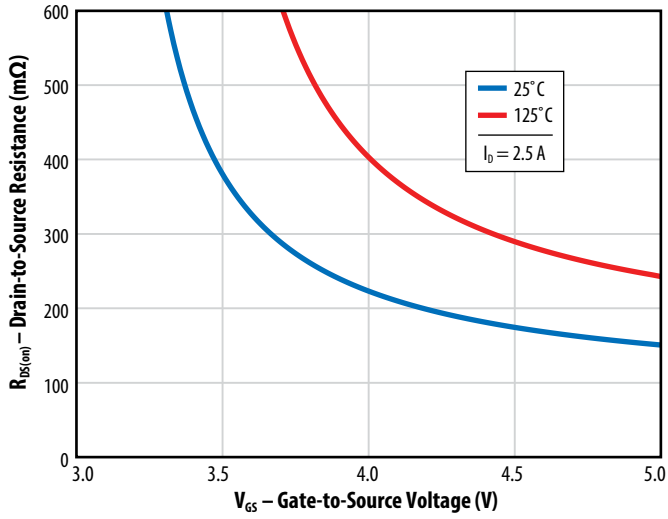**Figure 4a (Q1 & Q2): $R_{DS(on)}$ vs. V_{GS} for Various Temperatures**

Figure 4b (Q3): $R_{DS(on)}$ vs. V_{GS} for Various Temperatures
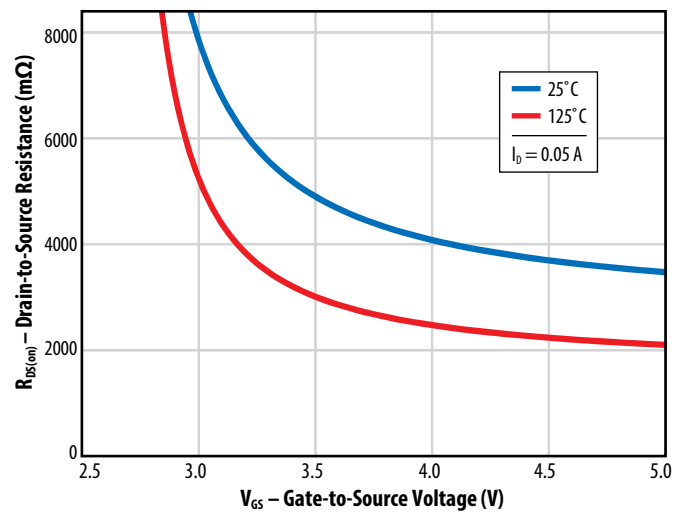
Figure 5a (Q1): Capacitance (Linear Scale)
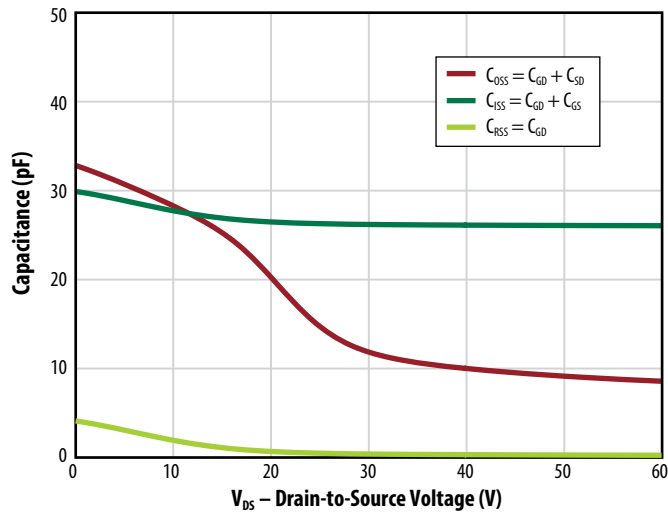
Figure 5b (Q1): Capacitance (Log Scale)
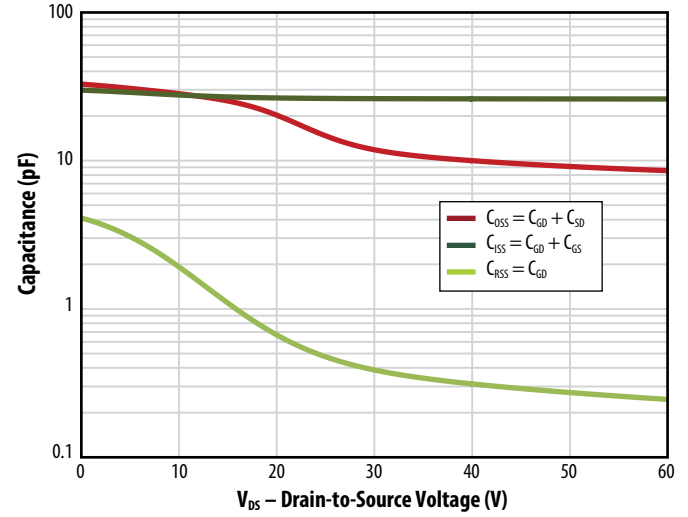
Figure 5c (Q2): Capacitance (Linear Scale)
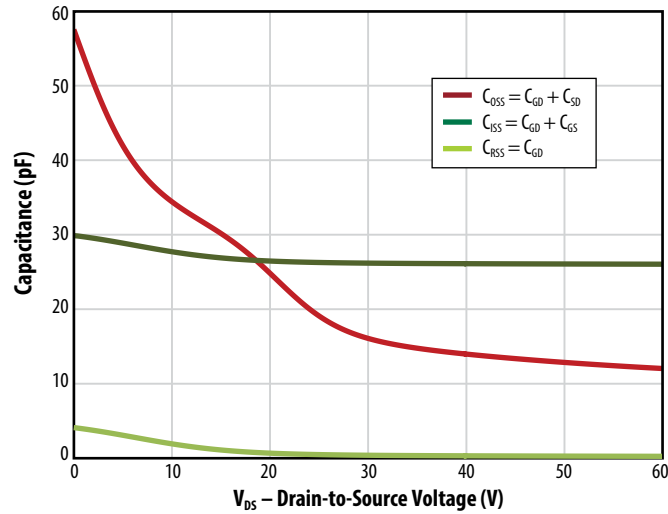
Figure 5d (Q2): Capacitance (Log Scale)
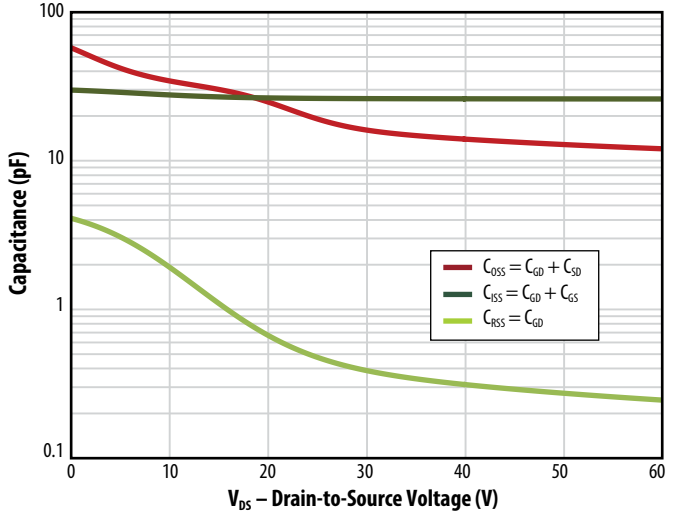
Figure 5e (Q3): Capacitance (Linear Scale)

Legend:
- $C_{OSS} = C_{GD} + C_{SD}$
- $C_{ISS} = C_{GD} + C_{GS}$
- $C_{RSS} = C_{GD}$

X-axis: V_{DS} – Drain-to-Source Voltage (V)
Y-axis: Capacitance (pF)
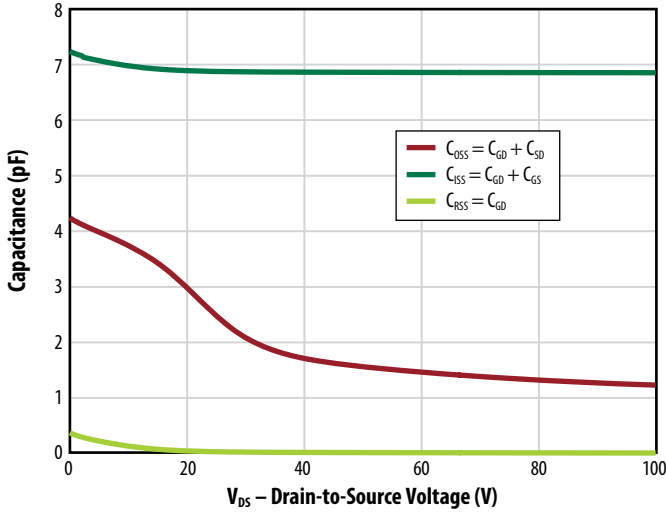
Figure 5f (Q3): Capacitance (Log Scale)

Legend:
- $C_{OSS} = C_{GD} + C_{SD}$
- $C_{ISS} = C_{GD} + C_{GS}$
- $C_{RSS} = C_{GD}$

X-axis: V_{DS} – Drain-to-Source Voltage (V)
Y-axis: Capacitance (pF)
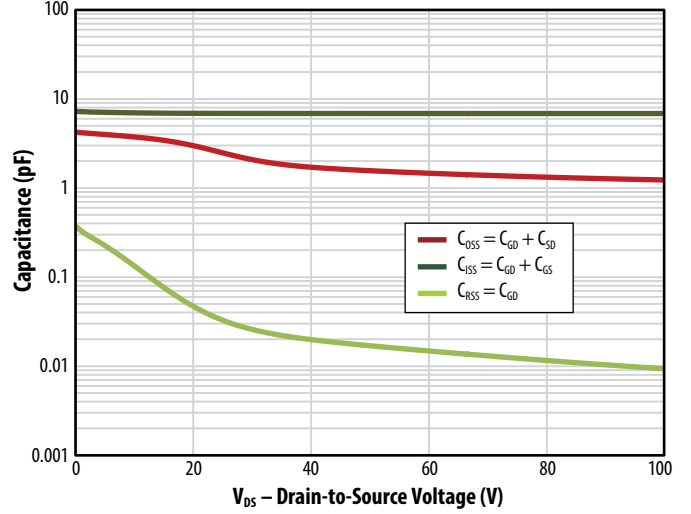
Figure 6a (Q1): Output Charge and C_{OSS} Stored Energy

X-axis: V_{DS} – Drain-to-Source Voltage (V)
Left Y-axis: Q_{OSS} – Output Charge (nC)
Right Y-axis: E_{OSS} – C_{OSS} Stored Energy (μJ)
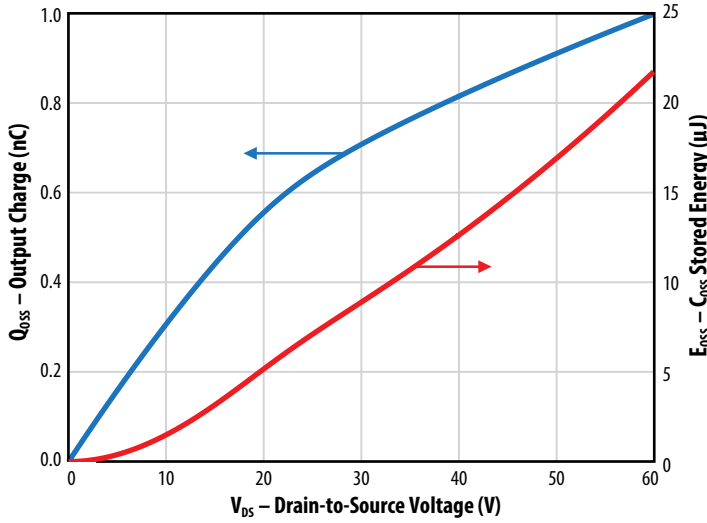
Figure 6b (Q2): Output Charge and C_{OSS} Stored Energy

X-axis: V_{DS} – Drain-to-Source Voltage (V)
Left Y-axis: Q_{OSS} – Output Charge (nC)
Right Y-axis: E_{OSS} – C_{OSS} Stored Energy (μJ)
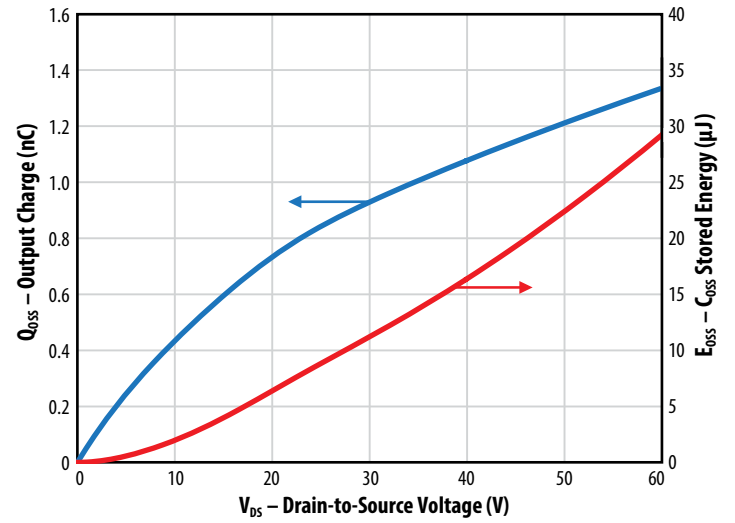
Figure 6c (Q3): Output Charge and C_{OSS} Stored Energy

X-axis: V_{DS} – Drain-to-Source Voltage (V)
Left Y-axis: Q_{OSS} – Output Charge (nC)
Right Y-axis: E_{OSS} – C_{OSS} Stored Energy (μJ)
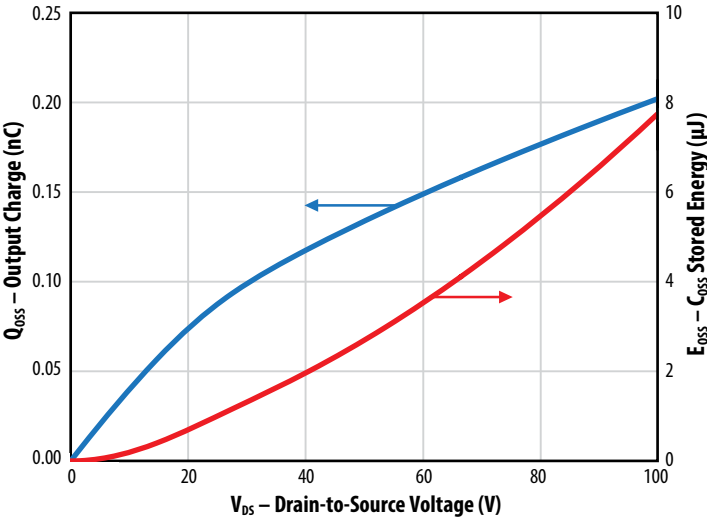
Figure 7a (Q1 & Q2): Gate Charge
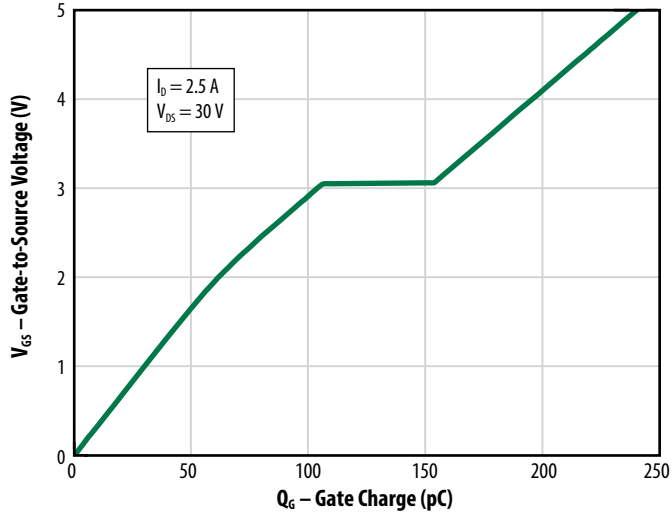
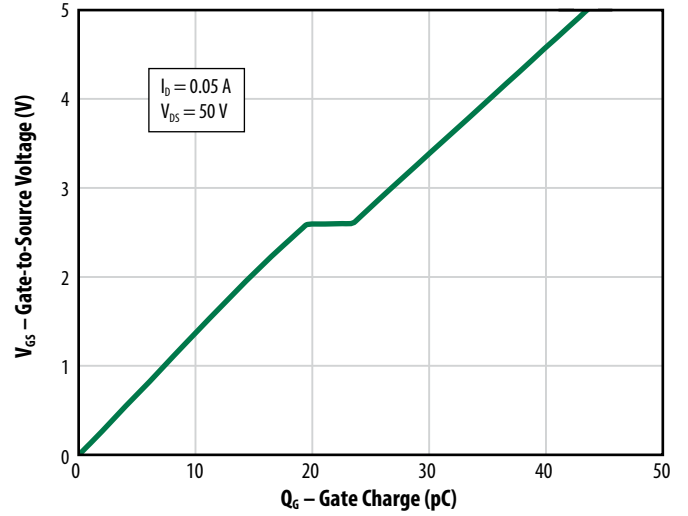**Figure 7b (Q3): Gate Charge**

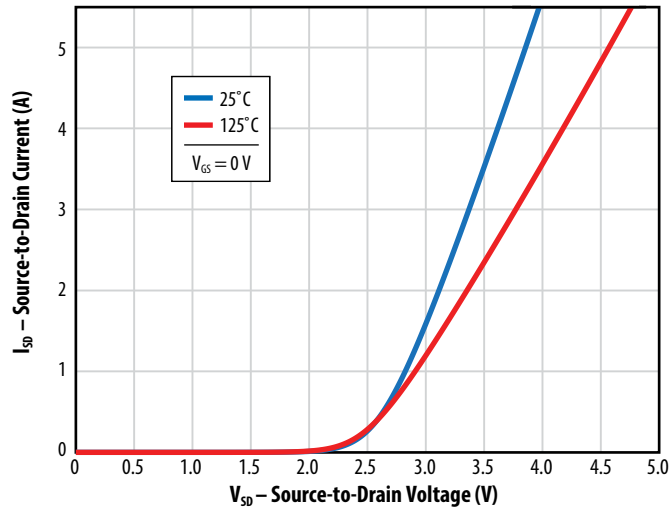**Figure 8a (Q1 & Q2): Reverse Drain-Source Characteristics**

Figure 8b (Q3): Reverse Drain-Source Characteristics
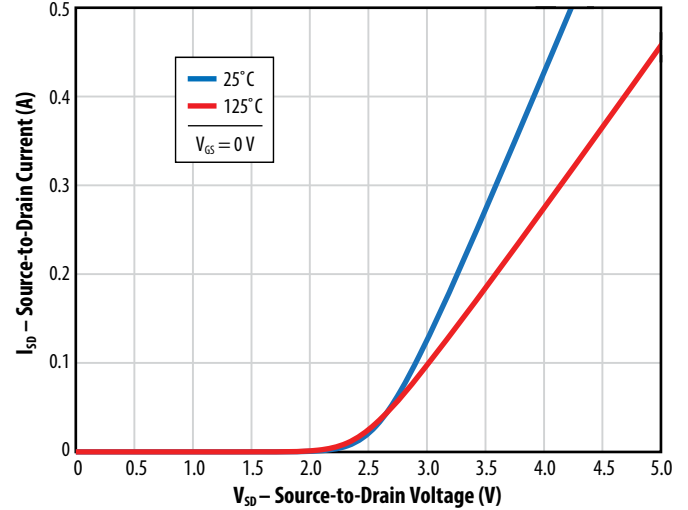

Figure 9a (Q1 & Q2):
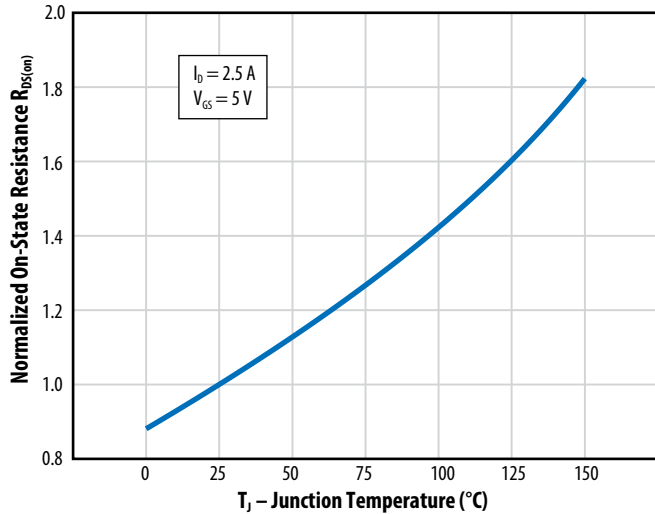**Normalized On-State Resistance vs. Temperature**

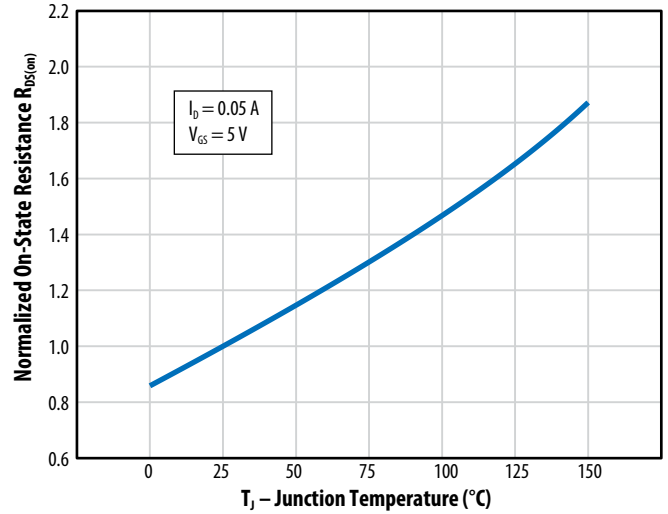**Figure 9b (Q3):**
Normalized On-State Resistance vs. Temperature

Figure 10a (Q1 & Q2):
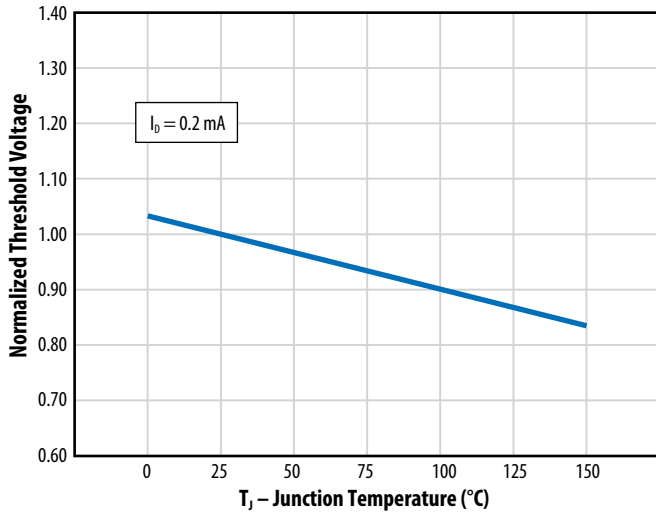**Normalized Threshold Voltage vs. Temperature**

Figure 10b (Q3):
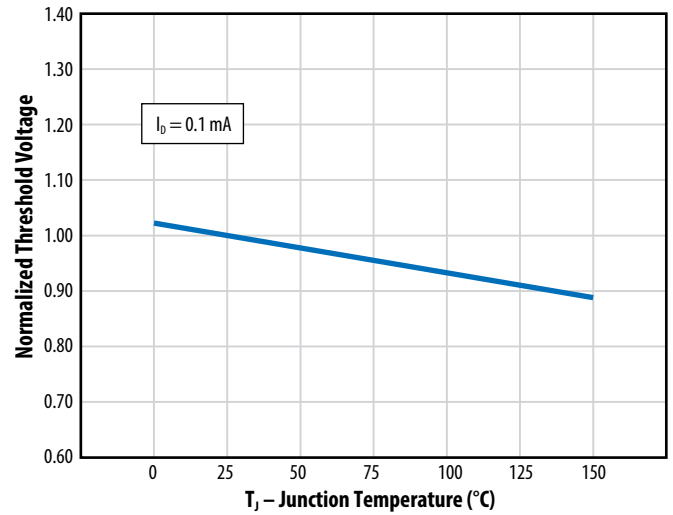**Normalized Threshold Voltage vs. Temperature**

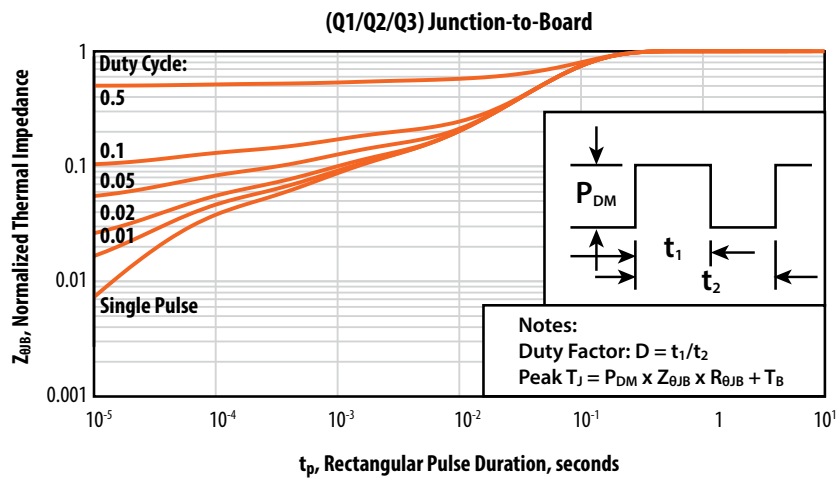
Figure 11a
Transient Thermal
Response Curves

(Q1/Q2/Q3) Junction-to-Board

Notes:
Duty Factor: $D = t_1/t_2$
Peak $T_J = P_{DM} \times Z_{\theta JB} \times R_{\theta JB} + T_B$

Figure 11b
Transient Thermal
Response Curves

(Q1/Q2/Q3) Junction-to-Case

Notes:
Duty Factor: $D = t_1/t_2$
Peak $T_J = P_{DM} \times Z_{\theta JC} \times R_{\theta JC} + T_C$
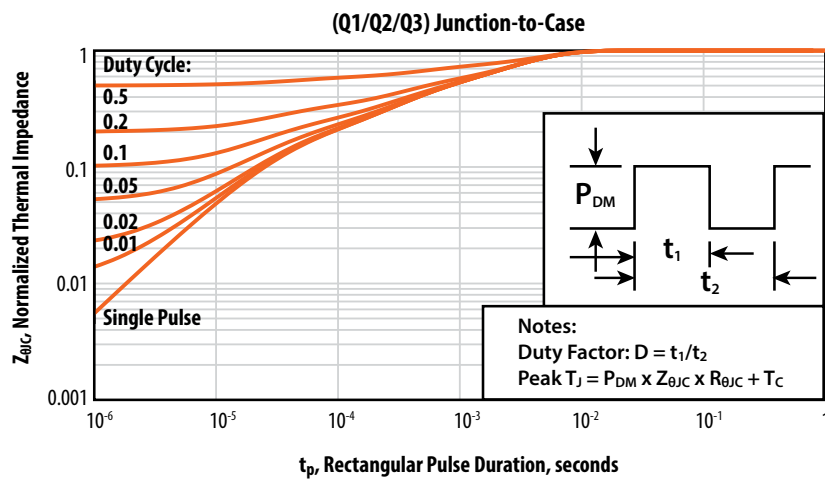
Figure 12 (Q1 & Q2): Safe Operating Area
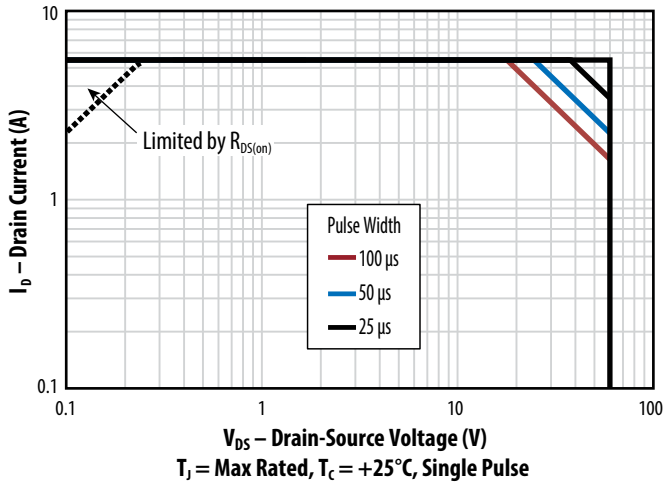

T_J = Max Rated, T_C = +25°C, Single Pulse
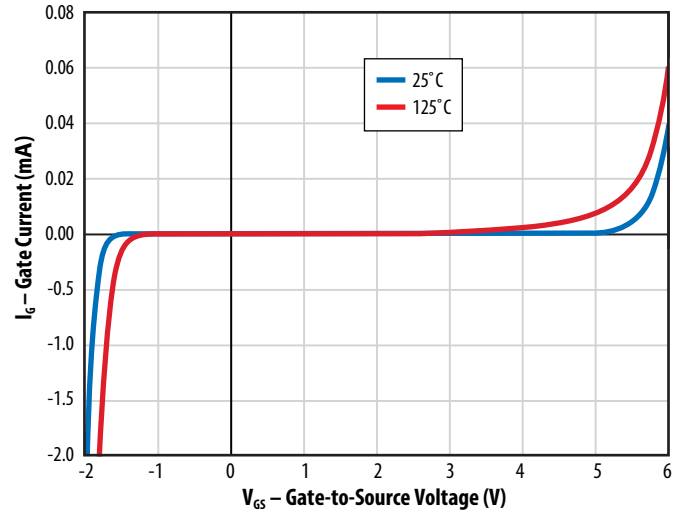
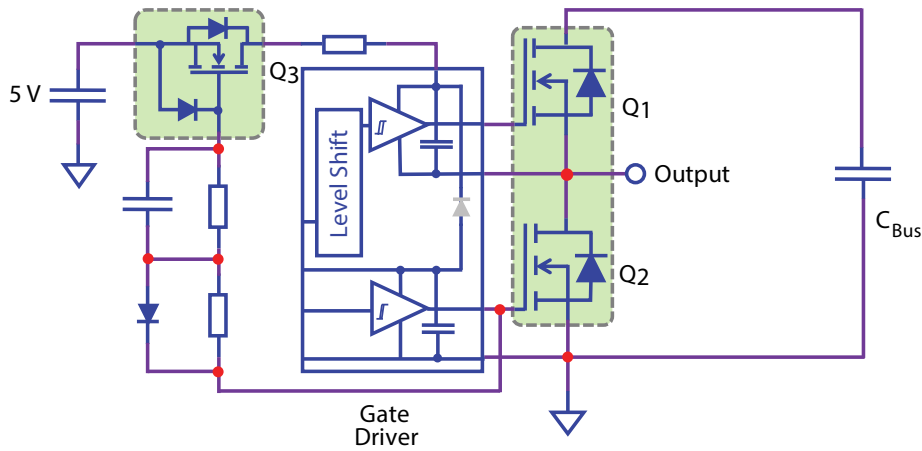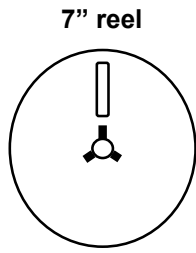## Figure 13 (Q3): Gate-Source Characteristics

Figure 14: Typical Application Circuit

TAPE AND REEL CONFIGURATION

4mm pitch, 8mm wide tape on 7" reel

7" reel

Loaded Tape Feed Direction

Die orientation dot

Pin 1 is under this corner

ZZZZ
YYYY
2108
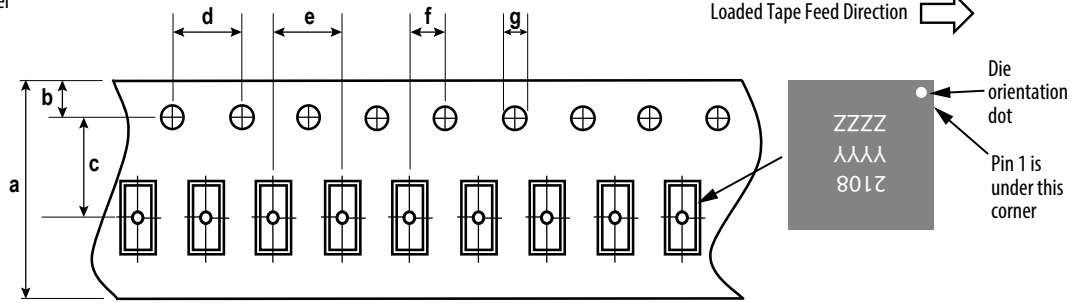
Die is placed into pocket solder bump side down (face side down)

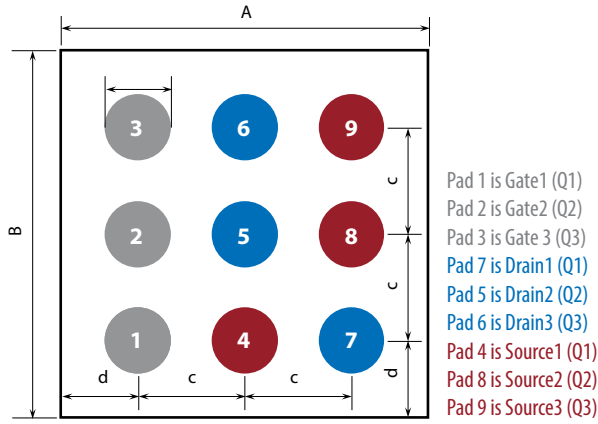| Dimension (mm)	EPC2108 (note 1)		
	target	min	max
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (see note)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (see note)	2.00	1.95	2.05
g	1.5	1.5	1.6

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.
Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

DIE MARKINGS

2108
YYYY
ZZZZ

Die orientation dot

Pin 1 is under this corner
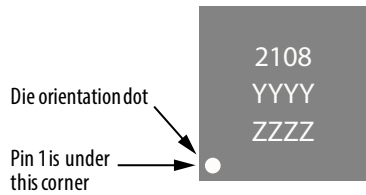
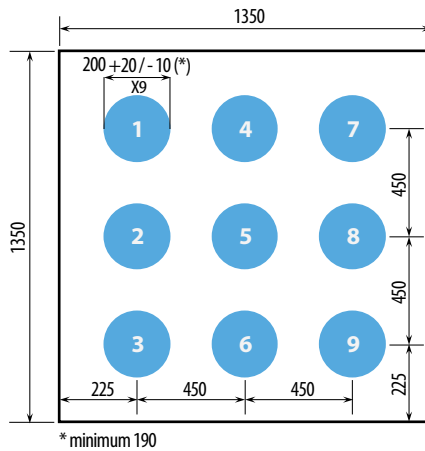| Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2108	2108	YYYY	ZZZZ

DIE OUTLINE
Solder Bump View

Pad 1 is Gate1 (Q1)
Pad 2 is Gate2 (Q2)
Pad 3 is Gate 3 (Q3)
Pad 7 is Drain1 (Q1)
Pad 5 is Drain2 (Q2)
Pad 6 is Drain3 (Q3)
Pad 4 is Source1 (Q1)
Pad 8 is Source2 (Q2)
Pad 9 is Source3 (Q3)

DIM	Micrometers		
	MIN	Nominal	MAX
A	1320	1350	1380
B	1320	1350	1380
c	450	450	450
d	210	225	240
e	187	208	229

Side View

(625)
815 Max
165 +/- 17

Seating Plane
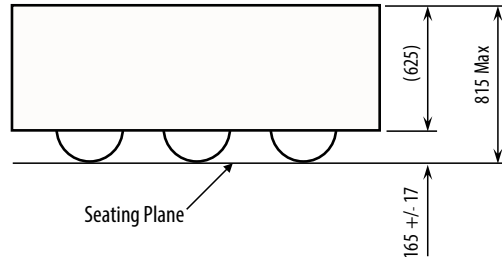
RECOMMENDED LAND PATTERN
(measurements in µm)

1350
200 +20 / -10 (*)
X9
1350
450
450
225   450   450   225

* minimum 190

The land pattern is solder mask defined
Solder mask is 10 µm smaller per side than bump

RECOMMENDED STENCIL DRAWING
(measurements in µm)

1350
250
R60
1350
450
450
225   450   450   225
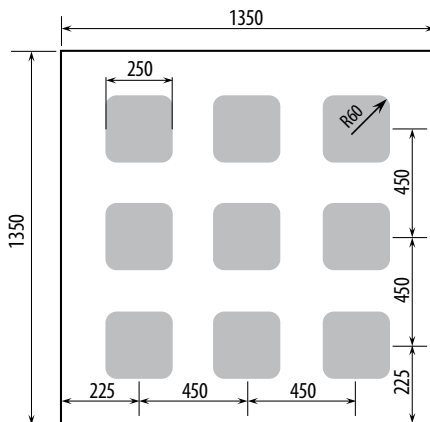
Recommended stencil should be 4 mil (100 µm) thick, must be laser cut, openings per drawing.

Intended for use with SAC305 Type 4 solder, reference 88.5% metals content.

Additional assembly resources available at
https://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx

Information subject to change without notice.
Revised August, 2019