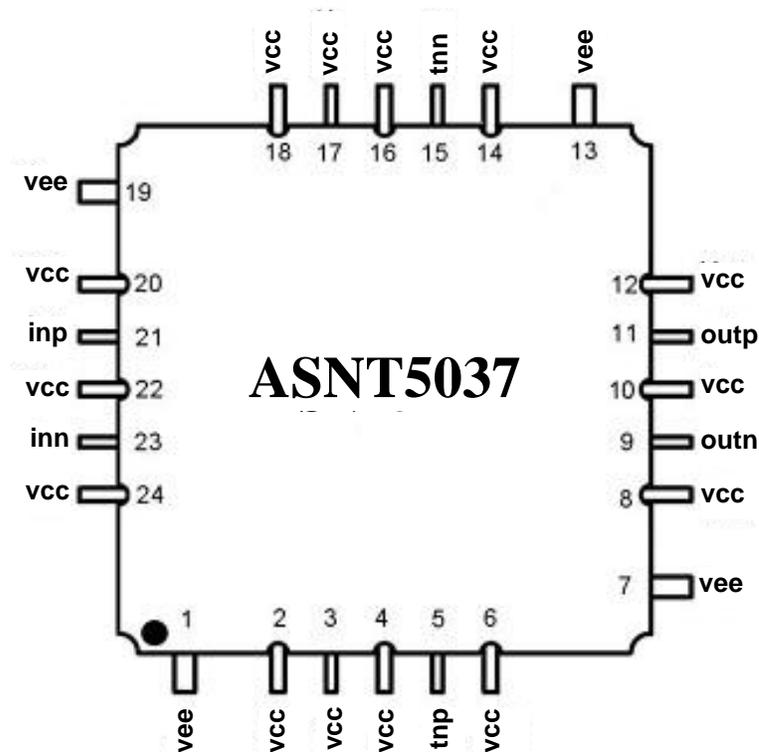# ASNT5037-KMC
DC-28*Gbps* Limiting Amplifier

- Broadband (DC-28*Gbps*) limiting amplifier

- Exhibits low jitter and limited temperature variation over industrial temperature range

- 100*MHz* of bandwidth for the amplitude adjustment tuning port

- Ideal for high speed proof-of-concept prototyping

- Fully differential CML input interfaces

- Fully differential CML output interface with adjustable SE amplitude from 0*V* to 1.1*V*

- Single +3.3*V* or -3.3*V* power supply

- Power consumption: 660*mW*

- Fabricated in SiGe for high performance, yield, and reliability
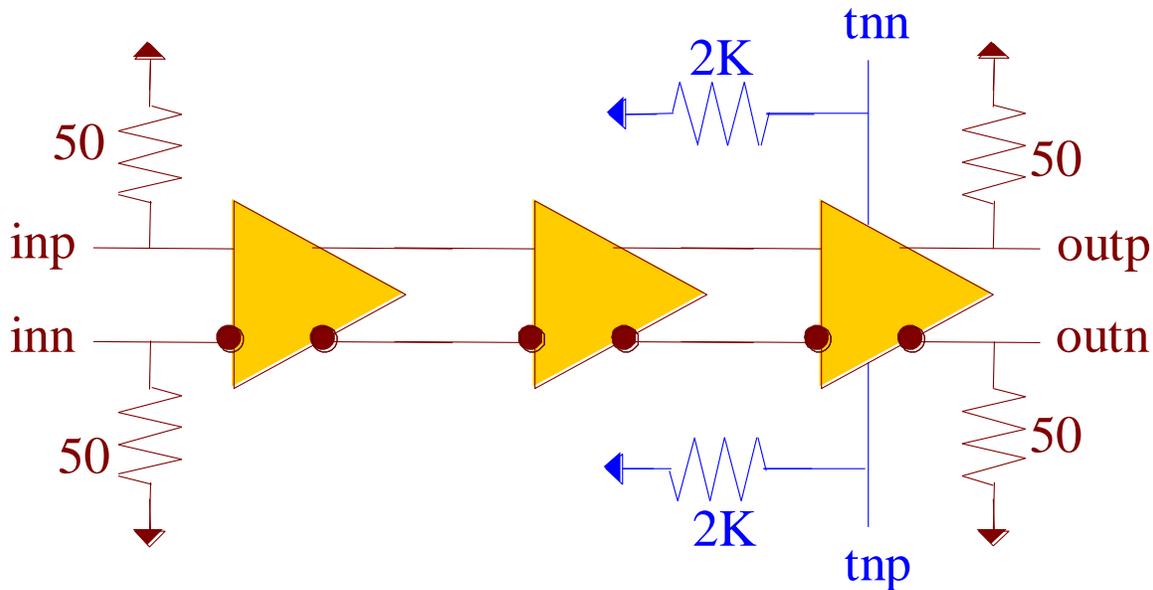
- Custom CQFP 24-pin package

DESCRIPTION

Fig. 1. Functional Block Diagram

The temperature stable ASNT5037-KMC SiGe IC provides extremely low jitter broadband signal amplitude control capability, and is intended for use in high-speed measurement / test equipment. The IC shown in Fig. 1 can process a high-speed data signal inp/inn and deliver a high-speed data output signal outp/outn with its output signal amplitude controlled by tuning ports tnp/tnn. Higher values of tnp and lower values of tnn (or higher values of the differential signal) result in higher output amplitudes.

The part's I/O's support the CML logic interface with on chip 50*Ohm* termination to vcc and may be used differentially, AC/DC coupled, single-ended, or in any combination (see also POWER SUPPLY CONFIGURATION). In the DC-coupling mode, the input signal's common mode voltage should comply with the specifications shown in ELECTRICAL CHARACTERISTICS. In the AC-coupling mode, the input termination provides the required common mode voltage automatically. The differential DC signaling mode is recommended for optimal performance.

Amplitude Control Port

The output amplitude is controlled through a wide-band differential tuning port tnp/tnn. The amplitude control diagram is shown in Fig. 2.
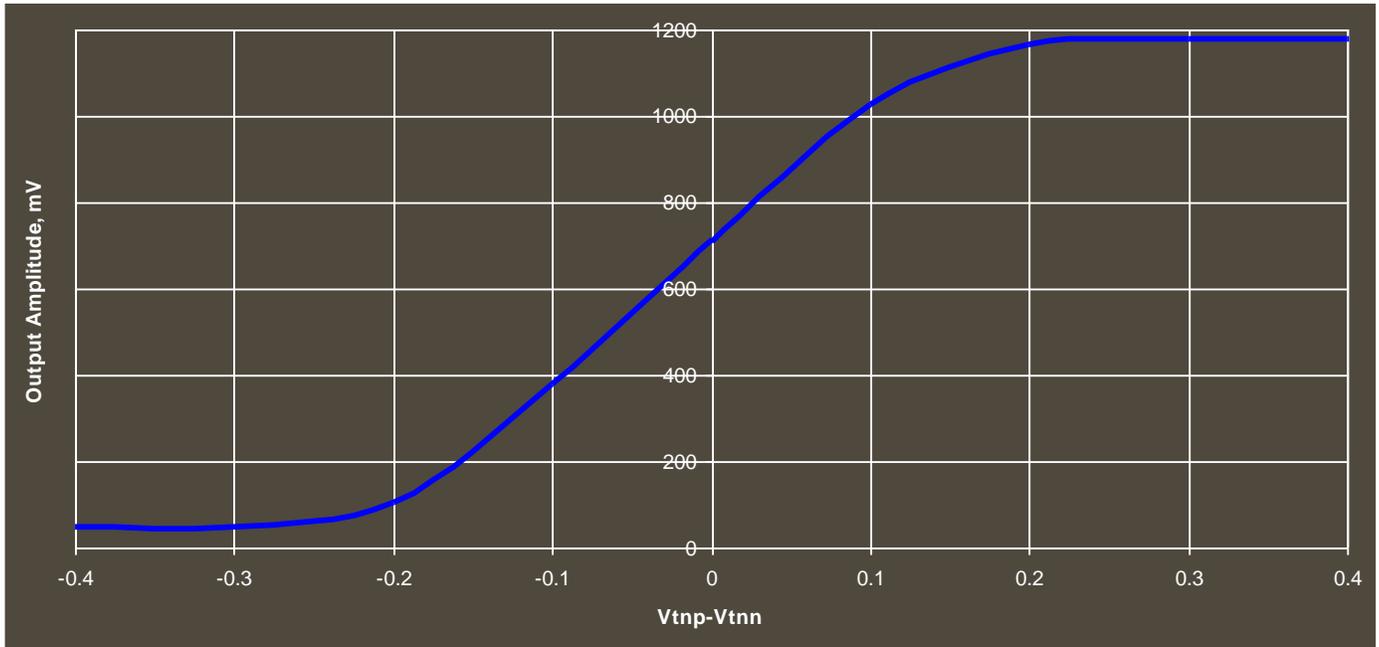
Fig. 2. Amplitude Control Diagram

POWER SUPPLY CONFIGURATION

The part can operate with either a negative supply ($vcc = 0.0V$ = ground and $vee = −3.3V$), or a positive supply ($vcc = +3.3V$ and $vee = 0.0V$ = ground). In case of the positive supply, all I/Os need AC termination when connected to any devices with $50Ohm$ termination to ground. Different PCB layouts will be needed for each different power supply combination.

All the characteristics detailed below assume $vcc = 0.0V$ and vee = -3.3V.

ABSOLUTE MAXIMUM RATINGS

Caution: Exceeding the absolute maximum ratings shown in Table 1 may cause damage to this product and/or lead to reduced reliability. Functional performance is specified over the recommended operating conditions for power supply and temperature only. AC and DC device characteristics at or beyond the absolute maximum ratings are not assumed or implied. All min and max voltage limits are referenced to ground (assumed vcc).

Table 1. Absolute Maximum Ratings

Parameter	Min	Max	Units
Supply Voltage (vee)		-3.6	*V*
Power Consumption		0.7	*W*
RF Input Voltage Swing (SE)		1.0	*V*
Case Temperature		+90	*ºC*
Storage Temperature	-40	+100	*ºC*
Operational Humidity	10	98	*%*
Storage Humidity	10	98	*%*

TERMINAL FUNCTIONS

TERMINAL			DESCRIPTION
Name	No.	Type	
High-Speed I/Os			
inp	21	CML input	Differential high-speed signal inputs with internal SE 50*Ohm* termination to vcc
inn	23		
outp	11	CML output	Differential high-speed signal outputs with internal SE 50*Ohm* termination to vcc. Require external SE 50*Ohm* termination to vcc
outn	9		
tnp	5	CML input	Differential output amplitude control signal with internal 2*KOhm* termination to vcc
tnn	15		
Supply and Termination Voltages			
Name	Description		Pin Number
vcc	Positive power supply (+3.3*V* or 0)		2, 3, 4, 6, 8, 10, 12, 14, 16, 17, 18, 20, 22, 24
vee	Negative power supply (0*V* or -3.3*V*)		1, 7, 13, 19

ELECTRICAL CHARACTERISTICS

PARAMETER	MIN	TYP	MAX	UNIT	COMMENTS
General Parameters					
vee	-3.1	-3.3	-3.5	*V*	±6%
vcc		0.0		*V*	External ground
*I*vee		200		*mA*	
Power consumption		660		*mW*	
Junction temperature	-40	25	125	*°C*	
HS Input Data (inp/inn)					
Data Rate	DC		28	*Gbps*	
Swing	0.05		1.0	*V*	Differential or SE, p-p
CM Voltage Level	vcc-0.8		vcc	*V*	Must match for both inputs
HS Output Data (outp/outn)					
Data Rate	DC		28	*Gbps*	
Logic "1" level		vcc		*V*	
Logic "0" level	vcc-1.1	vcc-0.55	vcc	*V*	With external 50*Ohm* DC termination, and full range of tnp/tnn control signal
Maximum swing		1.1		*V*	
Rise/Fall times	10	12	14	*ps*	20%-80%
Output Jitter			1	*ps*	Peak-to-peak
Duty cycle	45	50	55	*%*	
Tuning port (tnp/tnn)					
Bandwidth	DC		100	*MHz*	
SE voltage level	vcc-550		vcc	*mV*	Half control range, the opposite pin at vcc
SE voltage level	vcc-1100		vcc	*mV*	Full control range, the opposite pin at vcc-0.5*V*
Differential swing	0		1100	*mV*	Peak-peak, full control range
CM Voltage Level	vcc-0.55		vcc	*V*	Must match for both inputs

PACKAGE INFORMATION

The chip die is housed in a custom 24-pin CQFP package shown in Fig. 3. The package provides a center heat slug located on its back side to be used for heat dissipation. ADSANTEC recommends for this section to be soldered to the VCC plain, which is ground for a negative supply, or power for a positive supply.

Fig. 3. CQFP 24-Pin Package Drawing (All Dimensions in mm)

The part's identification label is ASNT5037-KMC. The first 8 characters of the name before the dash identify the bare die including general circuit family, fabrication technology, specific circuit type, and part version while the 3 characters after the dash represent the package's manufacturer, type, and pin out count.

This device complies with the Restriction of Hazardous Substances (RoHS) per 2011/65/EU for all ten substances.

REVISION HISTORY

Revision	Date	Changes
3.5.2	04-2020	Updated Package Information
3.4.2	07-2019	Updated Letterhead
3.4.1	07-2015	Added amplitude control port section
		Revised absolute maximum ratings table
		Revised electrical characteristics
		Revised package information
3.3.1	07-2014	Added description of tnp/tnn ports
3.2.1	03-2013	Revised package pin out drawing
		Revised functional block diagram
		Revised description
		Revised power supply configuration
		Revised absolute maximum ratings
		Revised terminal functions
		Revised electrical characteristics
		Revised package information
		Added mechanical drawing
		Format correction
3.1	02-2012	Revised power supply configuration section
		Revised package information section
3.0	01-2012	Added power supply configuration text
		Added absolute maximum ratings table
		Revised electrical characteristics section
		Revised package information section
2.0	02-2009	Revised electrical characteristics section
		Revised package information section
1.0	01-2009	First release