

## STS7PF30L P-CHANNEL 30V - 0.016Ω - 7A SO-8 STripFET™ II POWER MOSFET

PRELIMINARY DATA

TYPE	$v_{\text{DSS}}$	R <sub>DS(on)</sub>	ID
STS7PF30L	30 V	< 0.021 Ω	7 A

- TYPICAL  $R_{DS}(on) = 0.016\Omega$
- STANDARD OUTLINE FOR EASY AUTOMATED SURFACE MOUNT ASSEMBLY
- LOW THRESHOLD DRIVE

#### DESCRIPTION

This Power Mosfet is the latest development of ST-Microelectronics unique "Single Feature Size<sup>TM</sup>" strip-based process. The resulting transistor shows extremely high packing density for low on-resistance, rugged avalanche characteristics and less critical alignment steps therefore a remarkable manufacturing reproducibility.

#### APPLICATIONS

- BATTERY MANAGEMENT IN NOMADIC EQUIPMENT
- POWER MANAGEMENT IN CELLULAR PHONES





INTERNAL SCHEMATIC DIAGRAM

#### **ABSOLUTE MAXIMUM RATINGS**

Symbol	Parameter	Value	Unit
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	30	V
V <sub>DGR</sub>	Drain-gate Voltage ( $R_{GS} = 20 \text{ k}\Omega$ )	30	V
V <sub>GS</sub>	Gate- source Voltage	±20	V
ID	Drain Current (continuous) at $T_C = 25^{\circ}C$	7	А
ID	Drain Current (continuous) at T <sub>C</sub> = 100°C	4.4	A
I <sub>DM</sub>	Drain Current (pulsed)	28	А
P <sub>TOT</sub>	Total Dissipation at T <sub>C</sub> = 25°C	2.5	W
) Pulse width	limited by safe operating area Note	For the P-CHANNEL MOSFET actual polarit	ty of voltages and

Note: For the P-CHANNEL MOSFET actual polarity of voltages and current has to be reversed

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#### THERMAL DATA

Rthj-amb(#)	Thermal Resistance Junction-ambient Max	50	°C/W
Tj	Maximum Lead Temperature For Soldering Purpose Typ	150	°C
T <sub>stg</sub>	Storage Temperature	–55 to 150	°C

(#) When mounted on 1 inch<sup>2</sup> FR4 Board, 2 oz of Cu and t  $\leq$  10s

# **ELECTRICAL CHARACTERISTICS** (T<sub>J</sub> = 25 °C UNLESS OTHERRWISE SPECIFIED) OFF

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source Breakdown Voltage	$I_D = 250 \ \mu A, \ V_{GS} = 0$	30			V
I <sub>DSS</sub>	Zero Gate Voltage	V <sub>DS</sub> = Max Rating			1	μA
	Drain Current (V <sub>GS</sub> = 0)	$V_{DS}$ = Max Rating, $T_{C}$ = 125 °C			10	μA
I <sub>GSS</sub>	Gate-body Leakage Current (V <sub>DS</sub> = 0)	$V_{GS} = \pm 20V$			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250 \mu A$	1	1.6	2.5	V
R <sub>DS(on)</sub>	Static Drain-source On	$V_{GS} = 10V, I_D = 3.5A$	0.011	0.016	0.021	Ω
	Resistance	$V_{GS}$ = 4.5V, I <sub>D</sub> = 3.5A	0.016	0.022	0.028	Ω

#### DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
9 <sub>fs</sub>	Forward Transconductance	V <sub>DS</sub> = 10V, I <sub>D</sub> = 3.5A		16		S
C <sub>iss</sub>	Input Capacitance	$V_{DS} = 25 \text{ V}, \text{ f} = 1 \text{ MHz}, V_{GS} = 0$		2600		pF
Coss	Output Capacitance			523		pF
C <sub>rss</sub>	Reverse Transfer Capacitance			174		pF

## ELECTRICAL CHARACTERISTICS (CONTINUED)

## SWITCHING ON(2)

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
t <sub>d(on)</sub>	Turn-on Delay Time	V <sub>DD</sub> = 15V, I <sub>D</sub> = 3.5A		68		ns
t <sub>r</sub>	Rise Time	$R_G = 4.7\Omega V_{GS} = 4.5 V$ (Resistive Load, Figure 3)		54		ns
Q <sub>g</sub> Q <sub>gs</sub> Q <sub>gd</sub>	Total Gate Charge Gate-Source Charge Gate-Drain Charge	$V_{DD}$ =15 V, I <sub>D</sub> = 7 A, $V_{GS}$ = 4.5V		28 8.8 12	38	nC nC nC

## SWITCHING OFF(2)

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
t <sub>d(off)</sub> t <sub>f</sub>	Turn-off-Delay Time Fall Time			65 23		ns ns

## SOURCE DRAIN DIODE (2)

Symbol	Parameter	Test Conditions	Min.	Тур.	Max.	Unit
I <sub>SD</sub>	Source-drain Current				7	А
I <sub>SDM</sub> (1)	Source-drain Current (pulsed)				28	А
V <sub>SD</sub> (2)	Forward On Voltage	$I_{SD} = 7 \text{ A}, V_{GS} = 0$			1.2	V
t <sub>rr</sub> Q <sub>rr</sub> I <sub>RRM</sub>	Reverse Recovery Time Reverse Recovery Charge Reverse Recovery Current	$I_{SD}$ = 7A, di/dt = 100A/µs, V <sub>DD</sub> = 24 V, T <sub>j</sub> = 150°C (see test circuit, Figure 5)		40 46 2.3		ns nC A

Note: 1. Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %.
2. Pulse width limited by safe operating area.

### STS7PF30L

Fig. 1: Unclamped Inductive Load Test Circuit



**Fig. 3:** Switching Times Test Circuit For Resistive Load



**Fig. 5:** Test Circuit For Inductive Load Switching And Diode Recovery Times



#### Fig. 2: Unclamped Inductive Waveform



Fig. 4: Gate Charge test Circuit



DIM.		mm		inch			
Dini.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
А			1.75			0.068	
a1	0.1		0.25	0.003		0.009	
a2			1.65			0.064	
a3	0.65		0.85	0.025		0.033	
b	0.35		0.48	0.013		0.018	
b1	0.19		0.25	0.007		0.010	
С	0.25		0.5	0.010		0.019	
c1			45	(typ.)	•		
D	4.8		5.0	0.188		0.196	
E	5.8		6.2	0.228		0.244	
е		1.27			0.050		
e3		3.81			0.150		
F	3.8		4.0	0.14		0.157	
L	0.4		1.27	0.015		0.050	
М			0.6			0.023	

## SO-8 MECHANICAL DATA



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