PRODUCT INFORMATION LETTER

PIL MMS-MMY/14/8345
Dated 17 Feb 2014

PRODUCT IMPROVEMENT for M24SRxx and SRTAG2K-D

Sales Type/product family label	M24SRxx and SRTAG2K-D
Type of change	Product design change
Reason for change	Product improvement
Description	Redesign refined for FWI parameter improvement
Forecasted date of implementation	10-Feb-2014
Forecasted date of samples for customer	10-Feb-2014
Forecasted date for **STMicroelectronics** change Qualification Plan results availability	10-Feb-2014
Involved ST facilities	Design

DOCUMENT APPROVAL

Name	Function
Fidelis, Sylvain	Marketing Manager
Rodrigues, Benoit	Product Manager
Pavano, Rita	Q.A. Manager

life.augmented

PRODUCT / PROCESS CHANGE INFORMATION

PRODUCT IMPROVEMENT for M24SRxx and SRTAG2K-D

What is the change?
This product change information intends to inform you that an improved version of M24SR02, M24SR04, M24SR16, M24SR64 and SRTAG2K-D is now available.

The only parameter change is **FWI** (Frame Waiting time Integer), which value has been improved from FWI = 9 to **FWI = 5**. Datasheet has been updated accordingly, all other parameters are unchanged.

Why?
The strategy of STMicroelectronics Memory Division is to support our customers on a long-term basis. In line with this commitment, these new versions of M24SRxx and SRTAG2K-D will improve the service to our customers.

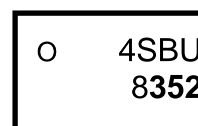
When?
The improved versions of M24SRxx and SRTAG2K-D are available.

How will the change be qualified?
The qualification followed the standard ST Microelectronics Corporate Procedures for Quality & Reliability. The Qualification Reports are included inside this document.

What is the impact of the change?

- **Form**: No change
- **Fit**: No change
- **Function**: FWI (Frame Waiting time Integer) improved from FWI = 9 to FWI = 5

How can the change be seen?
The improved versions of the M24SRxx and SRTAG2K-D are identified from **cut-off date code 352** (Year 201**3**, Week **52**) visible on the device marking, as being:

SO8N	**TSSOP8**	**UFDFPN8**
Example: M24SR64-YMN6T/2	Example: M24SR16-YDW6T/2	Example : M24SR04-YMC6T/2
		
24S64YA K352U	O 4SDYU K352	O 4SBU 8352

Appendix A- Product Change Information

Product family / Commercial products:	M24SRxx and SRTAG2K-D
Customer(s):	All
Type of change:	Product design change
Reason for the change:	Product improvement
Description of the change:	Redesign refined for FWI parameter improvement
Forecast date of the change: (Notification to customer)	Week 06 / 2014
Forecast date of Qualification samples availability for customer(s):	Available
Marking to identify the changed product:	Cut-off date code 352
Product Line(s) and/or Part Number(s):	See Appendix B
Manufacturing location:	Rousset 8 inch wafer fab
Estimated date of first shipment:	Week 10 / 2014 (or earlier upon customer agreement)

Appendix B- Concerned Products

M24SR64-YMN6T/2
M24SR64-YDW6T/2
M24SR64-YMC6T/2
M24SR16-YMN6T/2
M24SR16-YDW6T/2
M24SR16-YMC6T/2
M24SR04-YMN6T/2
M24SR04-YDW6T/2
M24SR04-YMC6T/2
M24SR02-YMN6T/2
M24SR02-YDW6T/2
M24SR02-YMC6T/2
SRTAG2K-DMC6T/2

Appendix C- Qualification Reports

See next pages

QRMMY1218
Qualification report

New product / M24SR64-Y using the CMOSF8H technology in the Rousset 8” Fab

Table 1. Product information

General information	
Commercial product	M24SR64-YMC6T/2 M24SR64-YMN6T/2 M24SR64-YDW6T/2
Product description	Dynamic NFC/RFID tag IC with 64-Kbit EEPROM, NFC Forum Type 4 Tag and I²C interface
Product group	MMS
Product division	MMY - Memory
Silicon process technology	CMOSF8H
Wafer fabrication location	RS8F - ST Rousset 8 inch, France
Electrical Wafer Sort test plant location	ST Rousset, France ST Toa Payoh, Singapore Subcontractor Ardentec, Singapore

Table 2. Package description

Package description	Assembly plant location	Final test plant location
SO8N	ST Shenzhen, China	ST Shenzhen, China
TSSOP8	ST Shenzhen, China	ST Shenzhen, China
UFDFPN8 (MLP8) 2 x 3 mm	ST Calamba, Philippines	ST Calamba, Philippines

Reliability / Qualification assessment: PASS

1 Reliability evaluation overview

1.1 Objectives

This qualification report summarizes the results of the reliability trials that were performed to qualify the new product M24SR64-Y using the CMOSF8H silicon process technology in the ST Rousset 8” diffusion fab.

The CMOSF8H is a new advanced silicon process technology that is already qualified in the ST Rousset 8” fab, and in production for EEPROM products and also for dual interface EEPROM M24LRxx products.

This document serves for the qualification of the named product using the named silicon process technology in the named diffusion fab.

The features covered by this document are:

- I^2C interface:
  - Two-wire I2C serial interface supports 1 MHz protocol
  - Single supply voltage: 2.7 to 5.5
- Contactless interface:
  - NFC Forum Type 4 Tag
  - ISO/IEC 14443 Type A
  - 106 Kbps data rate

The temperature range covered by this document is:

- –40 to 85 °C

1.2 Conclusion

The new product M24SR64-Y using the CMOSF8H silicon process technology in the ST Rousset 8” diffusion fab has passed the reliability requirements and all products described in *Table 1* are qualified.

Refer to *Section 3: Reliability test results* for details on the reliability test results.

2 Device characteristics

Device description

The M24SR64-Y device is a dynamic NFC/RFID tag that can be accessed either from the I^2C or the RF interface. The RF and I2C host can read or write to the same memory, that is why only one host can communicate at a time with the M24SR64-Y. The management of the interface selection is controlled by the M24SR64-Y device itself.

The RF interface is based on the ISO/IEC 14443 Type A standard. The M24SR64-Y is compatible with the NFC Forum Type 4 Tag specifications and supports all corresponding commands.

The I2C interface uses a two-wire serial interface consisting of a bidirectional data line and a clock line. The devices carry a built-in 4-bit device type identifier code in accordance with the I^2C bus definition.

The device behaves as a slave in the I2C protocol.

Refer to the product datasheet for more details.

3 Reliability test results

This section contains a general description of the reliability evaluation strategy. The named products are qualified using the standard STMicroelectronics corporate procedures for quality and reliability.

The product vehicle used for the die qualification is presented in *Table 3*.

Table 3. Product vehicle used for die qualification

Product	Silicon process technology	Wafer fabrication location	Package description	Assembly plant location
M24SR64-Y	CMOSF8H	ST Rousset 8”	CDIP24	Engineering assembly (1)

1. CDIP24 is a ceramic package used only for die-oriented reliability trials.

The product vehicle used for package qualifications is presented in *Table 4*.

Table 4. Product vehicle used for package qualification

<table>
<tr><th>Product</th><th>Silicon process technology</th><th>Wafer fabrication location</th><th>Package description</th><th>Assembly plant location</th></tr>
<tr><td rowspan="6">M24SR64-Y</td><td rowspan="6">CMOSF8H</td><td rowspan="6">ST Rousset 8”</td><td rowspan="2">SO8N</td><td>ST Shenzhen</td></tr>
<tr><td>Subcon Amkor P1</td></tr>
<tr><td rowspan="2">TSSOP8</td><td>ST Shenzhen</td></tr>
<tr><td>Subcon Amkor P1</td></tr>
<tr><td rowspan="2">UFDFPN8 (MLP8)
2 x 3 mm</td><td>ST Calamba</td></tr>
<tr><td>Subcon Amkor P3</td></tr>
</table>

3.1 Reliability test plan and result summary

The reliability test plan and the result summary are presented as follows:

- in *Table 5* for die-oriented tests
- in *Table 6* for SO8N ST Shenzhen package-oriented tests
- in *Table 7* for TSSOP8 ST Shenzhen package-oriented tests
- in *Table 8* for UFDFPN8 (MLP8) 2 x 3 mm ST Calamba package-oriented test

Reliability tests on all other packages are planned, but results are not yet available.

Table 5. Die-oriented reliability test plan and result summary (CDIP8 / Engineering package)[1]

Test	Test short description							
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size		
						M24SR64-Y		
						Lot 1	Lot 2	Lot 3
EDR	High temperature operating life after endurance							
	AEC-Q100-005	1 million E/W cycles at 25 °C then: HTOL 150 °C, 6 V	80	3	1008 hrs	0/80	0/80	0/80
	Data retention after endurance							
	AEC-Q100-005	1 million E/W cycles at 25 °C then: HTSL at 150 °C	80	3	1008 hrs	0/80	0/80	0/80
LTOL	Low temperature operating life							
	JESD22-A108	–40 °C, 6 V	80	3	1008 hrs	0/80	0/80	0/80
WEB	Program/erase endurance cycling + bake							
	Internal spec.	1 million E/W cycles at 25 °C then: Retention bake at 200 °C / 48 hours	80	3	1 Million cycles / 48 hrs	0/80 [2]	0/80 [2]	0/80 [2]
ESD HBM	Electrostatic discharge (human body model)							
	AEC-Q100-002 JESD22-A114	C = 100 pF, R= 1500 Ω pads AC0, AC1	27	3	N/A	Pass 1000 V	Pass 1000 V	Pass 1000 V
		C = 100 pF, R= 1500 Ω Other pads			N/A	Pass 3500 V	Pass 3500 V	Pass 3500 V
ESD MM	Electrostatic discharge (machine model)							
	AEC-Q100-003 JESD22-A115	C = 200 pF, R = 0 Ω	21	3	N/A	Pass 150 V	Pass 150 V	Pass 150 V
LU	Latch-up (current injection and overvoltage stress)							
	AEC-Q100-004 JESD78B	At maximum operating temperature (150 °C)	6	3	N/A	Class II Level A	Class II Level A	Class II Level A

1. See *Table 9: List of terms* for a definition of abbreviations.
2. First rejects after 5 million cycles.

.

Table 6. Package-oriented reliability test plan and result summary (SO8N / ST Shenzhen) [1]

Test	Test short description					Results fail / sample size M24SR64-Y Lot 1
	Method	**Conditions**	**Sample size / lots**	**No. of lots**	**Duration**	
PC	Preconditioning: moisture sensitivity level 1					
	JESD22-A113 J-STD-020D	MSL1, peak temperature at 260 °C, 3 IReflow	1145	1	N/A	0/1145
THB [2]	Temperature humidity bias					
	AEC-Q100-JESD22-A101	85 °C, 85% RH, bias 5.6 V	80	1	1008 hrs	0/80
TC [2]	Temperature cycling					
	AEC-Q100-JESD22-A104	–65 °C / +175 °C	80	1	1000 cycles	0/80
TMSK [2]	Thermal shocks					
	JESD22-A106	–55 °C / +125 °C	25	1	200 shocks	0/25
AC [2]	Autoclave (pressure pot)					
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	1	168 hrs	0/80
HTSL [2]	High temperature storage life					
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	1	1008 hrs	0/80
ELFR [2]	Early failure life rate					
	AEC-Q100-008	HTOL 150 °C, 6V	800	1	48 hrs	0/800
ESD CDM	Electrostatic discharge (charge device model)					
	AEC-Q100-JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500 V

1. See *Table 9: List of terms* for a definition of abbreviations.
2. THB-, TC-, TMSK-, AC-, HTSL- and ELFR- dedicated parts are first subject to preconditioning flow.

Table 7. Package-oriented reliability test plan and result summary (TSSOP8 / ST Shenzhen) (1)

Test	Test short description					
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size M24SR64-Y Lot 1
PC	Preconditioning: moisture sensitivity level 1					
	JESD22-A113 J-STD-020D	MSL1, peak temperature at 260 °C, 3 IReflow	1145	1	N/A	0/1145
THB (2)	Temperature humidity bias					
	AEC-Q100- JESD22-A101	85 °C, 85% RH, bias 5.6 V	80	1	1008 hrs	0/80
TC (2)	Temperature cycling					
	AEC-Q100- JESD22-A104	–65 °C / +175 °C	80	1	1000 cycles	0/80
TMSK (2)	Thermal shocks					
	JESD22-A106	–55 °C / +125 °C	25	1	200 shocks	0/25
AC (2)	Autoclave (pressure pot)					
	AEC-Q100- JESD22-A102	121 °C, 100% RH at 2 ATM	80	1	168 hrs	0/80
HTSL (2)	High temperature storage life					
	AEC-Q100- JESD22-A103	Retention bake at 150 °C	80	1	1008 hrs	0/80
ELFR (2)	Early failure life rate					
	AEC-Q100-008	HTOL 150 °C, 6V	800	1	48 hrs	0/800
ESD CDM	Electrostatic discharge (charge device model)					
	AEC-Q100- JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500 V

1. See *Table 9: List of terms* for a definition of abbreviations.
2. THB-, TC-, TMSK-, AC-, HTSL- and ELFR- dedicated parts are first subject to preconditioning flow.

Table 8. Package-oriented reliability test plan and result summary (UFDFPN8 MLP8 2 x 3 mm / ST Calamba) (1)

Test	Test short description					
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size M24SR64-Y Lot 1
PC	Preconditioning: moisture sensitivity level 1					
	JESD22-A113 J-STD-020D	MSL1, peak temperature at 260 °C, 3 IReflow	345	1	N/A	0/345
THB (2)	Temperature humidity bias					
	AEC-Q100-JESD22-A101	85 °C, 85% RH, bias 5.6 V	80	1	1008 hrs	0/80
TC(2)	Temperature cycling					
	AEC-Q100-JESD22-A104	–65 °C / +175 °C	80	1	1000 cycles	0/80
TMSK (2)	Thermal shocks					
	JESD22-A106	–55 °C / +125 °C	25	1	200 shocks	0/25
AC(2)	Autoclave (pressure pot)					
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	1	168 hrs	0/80
HTSL (2)	High temperature storage life					
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	1	1008 hrs	0/80
ESD CDM	Electrostatic discharge (charge device model)					
	AEC-Q100-JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500 V

1. See *Table 9: List of terms* for a definition of abbreviations.
2. THB-, TC-, TMSK-, AC-, and HTSL- dedicated parts are first subject to preconditioning flow.

4 Applicable and reference documents

- AEC-Q100: Stress test qualification for integrated circuits
- SOP 2.6.10: General product qualification procedure
- SOP 2.6.11: Program management for product qualification
- SOP 2.6.12: Design criteria for product qualification
- SOP 2.6.14: Reliability requirements for product qualification
- SOP 2.6.19: Process maturity level
- SOP 2.6.2: Process qualification and transfer management
- SOP 2.6.20: New process / New product qualification
- SOP 2.6.7: Product maturity level
- SOP 2.6.9: Package and process maturity management in Back End
- SOP 2.7.5: Automotive products definition and status
- JESD22-A101: Steady state temperature humidity bias life test
- JESD22-A102: Accelerated moisture resistance - unbiased autoclave
- JESD22-A103: High temperature storage life
- JESD22-A104: Temperature cycling
- JESD22-A106: Thermal shock
- JESD22-A108: Temperature, bias, and operating life
- JESD22-A113: Preconditioning of nonhermetic surface mount devices prior to reliability testing
- JESD22-A114: Electrostatic discharge (ESD) sensitivity testing human body model (HBM)
- JESD22-A115: Electrostatic discharge (ESD) sensitivity testing machine model (MM)
- JESD78: IC Latch-up test
- J-STD-020D: Moisture/reflow sensitivity classification for nonhermetic solid state surface mount devices

5 Glossary

Table 9. List of terms

Terms	Description
EDR	NVM endurance, data retention and operational life
HTOL	High temperature operating life
LTOL	Low temperature operating life
HTB	High temperature bake
WEB	Program/Erase endurance cycling + bake
ESD HBM	Electrostatic discharge (human body model)
ESD MM	Electrostatic discharge (machine model)
LU	Latch-up
PC	Preconditioning (solder simulation)
THB	Temperature humidity bias
TC	Temperature cycling
TMSK	Thermal shocks
AC	Autoclave (pressure pot)
HTSL	High temperature storage life
ELFR	Early life failure rate
ESD CDM	Electrostatic discharge (charge device model)

6 Revision history

Table 10. Document revision history

Date	Revision	Changes
20-Dec-2013	1	Initial release.
27-Jan-2013	2	Updated list of qualified commercial products in *Table 1*. Added *Table 8: Package-oriented reliability test plan and result summary (UFDFPN8 MLP8 2 x 3 mm / ST Calamba)*.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

ST PRODUCTS ARE NOT DESIGNED OR AUTHORIZED FOR USE IN: (A) SAFETY CRITICAL APPLICATIONS SUCH AS LIFE SUPPORTING, ACTIVE IMPLANTED DEVICES OR SYSTEMS WITH PRODUCT FUNCTIONAL SAFETY REQUIREMENTS; (B) AERONAUTIC APPLICATIONS; (C) AUTOMOTIVE APPLICATIONS OR ENVIRONMENTS, AND/OR (D) AEROSPACE APPLICATIONS OR ENVIRONMENTS. WHERE ST PRODUCTS ARE NOT DESIGNED FOR SUCH USE, THE PURCHASER SHALL USE PRODUCTS AT PURCHASER'S SOLE RISK, EVEN IF ST HAS BEEN INFORMED IN WRITING OF SUCH USAGE, UNLESS A PRODUCT IS EXPRESSLY DESIGNATED BY ST AS BEING INTENDED FOR "AUTOMOTIVE, AUTOMOTIVE SAFETY OR MEDICAL" INDUSTRY DOMAINS ACCORDING TO ST PRODUCT DESIGN SPECIFICATIONS. PRODUCTS FORMALLY ESCC, QML OR JAN QUALIFIED ARE DEEMED SUITABLE FOR USE IN AEROSPACE BY THE CORRESPONDING GOVERNMENTAL AGENCY.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.
Information in this document supersedes and replaces all information previously supplied.
The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2014 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com

QRMMY1335
Qualification report

New product / M24SR16-Y using the CMOSF8H technology in the Rousset 8” Fab

Table 1. Product information

General information	
Commercial product	M24SR16-YMC6T/2 M24SR16-YMN6T/2 M24SR16-YDW6T/2
Product description	Dynamic NFC/RFID tag IC with 16-Kbit EEPROM, NFC Forum Type 4 Tag and I²C interface
Product group	MMS
Product division	MMY - Memory
Silicon process technology	CMOSF8H
Wafer fabrication location	RS8F - ST Rousset 8 inch, France
Electrical Wafer Sort test plant location	ST Rousset, France ST Toa Payoh, Singapore Subcontractor Ardentec, Singapore

Table 2. Package description

Package description	Assembly plant location	Final test plant location
SO8N	ST Shenzhen, China	ST Shenzhen, China
TSSOP8	ST Shenzhen, China	ST Shenzhen, China
UFDFPN8 (MLP8) 2 x 3 mm	ST Calamba, Philippines	ST Calamba, Philippines

Reliability / Qualification assessment: PASS

1 Reliability evaluation overview

1.1 Objectives

This qualification report summarizes the results of the reliability trials that were performed to qualify the new product M24SR16-Y using the CMOSF8H silicon process technology in the ST Rousset 8” diffusion fab.

The CMOSF8H is a new advanced silicon process technology that is already qualified in the ST Rousset 8” fab, and in production for EEPROM products and also for dual interface EEPROM M24LRxx products.

This document serves for the qualification of the named product using the named silicon process technology in the named diffusion fab.

The features covered by this document are:

- I^2C interface:
  - Two-wire I^2C serial interface supports 1 MHz protocol
  - Single supply voltage: 2.7 to 5.5 V
- Contactless interface:
  - NFC Forum Type 4 Tag
  - ISO/IEC 14443 Type A
  - 106 Kbps data rate

The temperature range covered by this document is:

- –40 to 85 °C

1.2 Conclusion

The new product M24SR16-Y using the CMOSF8H silicon process technology in the ST Rousset 8” diffusion fab has passed the reliability requirements and all products described in *Table 1* are qualified.

Refer to *Section 3: Reliability test results* for details on the reliability test results.

2 Device characteristics

Device description

The M24SR16-Y device is a dynamic NFC/RFID tag that can be accessed either from the I2C or the RF interface. The RF and I2C host can read or write to the same memory, that is why only one host can communicate at a time with the M24SR16-Y. The management of the interface selection is controlled by the M24SR16-Y device itself.

The RF interface is based on the ISO/IEC 14443 Type A standard. The M24SR16-Y is compatible with the NFC Forum Type 4 Tag specifications and supports all corresponding commands.

The I2C interface uses a two-wire serial interface consisting of a bidirectional data line and a clock line. The devices carry a built-in 4-bit device type identifier code in accordance with the I^2C bus definition.

The device behaves as a slave in the I2C protocol.

Refer to the product datasheet for more details.

3 Reliability test results

This section contains a general description of the reliability evaluation strategy. The named products are qualified using the standard STMicroelectronics corporate procedures for quality and reliability.

The product vehicle used for the die qualification is presented in *Table 3*.

Table 3. Product vehicle used for die qualification

Product	Silicon process technology	Wafer fabrication location	Package description	Assembly plant location
M24SR16-Y	CMOSF8H	ST Rousset 8”	CDIP24	Engineering assembly (1)

1. CDIP24 is a ceramic package used only for die-oriented reliability trials.

The package qualifications were mainly obtained by similarity. The product vehicle used for package qualifications is presented in *Table 4*.

Table 4. Product vehicle used for package qualification

<table>
<tr><th>Product</th><th>Silicon process technology</th><th>Wafer fabrication location</th><th>Package description</th><th>Assembly plant location</th></tr>
<tr><td rowspan="6">M24SR64-Y (1)</td><td rowspan="6">CMOSF8H</td><td rowspan="6">ST Rousset 8”</td><td rowspan="2">SO8N</td><td>ST Shenzhen</td></tr>
<tr><td>Subcon Amkor P1</td></tr>
<tr><td rowspan="2">TSSOP8</td><td>ST Shenzhen</td></tr>
<tr><td>Subcon Amkor P1</td></tr>
<tr><td rowspan="2">UFDFPN8 (MLP8)
2 x 3 mm</td><td>ST Calamba</td></tr>
<tr><td>Subcon Amkor P3</td></tr>
</table>

1. Larger memory array using the same silicon process technology in the same diffusion fab. Package qualification results of M24SR64-Y are applicable to M24SR16-Y.

3.1 Reliability test plan and result summary

The reliability test plan and the result summary are presented as follows:

- in *Table 5* for die-oriented tests
- in *Table 6* for SO8N ST Shenzhen package-oriented tests
- in *Table 7* for TSSOP8 ST Shenzhen package-oriented tests
- in *Table 8* for UFDFPN8 (MLP8) 2 x 3 mm ST Calamba package-oriented tests

Reliability tests on all other packages are planned, but results are not yet available.

Table 5. Die-oriented reliability test plan and result summary (CDIP8 / Engineering package)[1]

Test	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size M24SR16-Y Lot 1	Lot 2	Lot 3
EDR	High temperature operating life after endurance							
	AEC-Q100-005	1 million E/W cycles at 25 °C then: HTOL 150 °C, 6 V	80	3	1008 hrs	0/80	0/80	0/80
	Data retention after endurance							
	AEC-Q100-005	1 million E/W cycles at 25 °C then: HTSL at 150 °C	80	3	1008 hrs	0/80	0/80	0/80
LTOL	Low temperature operating life							
	JESD22-A108	–40 °C, 6 V	80	3	1008 hrs	0/80	0/80	0/80
WEB	Program/erase endurance cycling + bake							
	Internal spec.	1 million E/W cycles at 25 °C then: Retention bake at 200 °C / 48 hours	80	3	1 Million cycles / 48 hrs	0/80 [2]	0/80 [2]	0/80 [2]
ESD HBM	Electrostatic discharge (human body model)							
	AEC-Q100-002 JESD22-A114	C = 100 pF, R= 1500 Ω pads AC0, AC1	27	3	N/A	Pass 1000 V	Pass 1000 V	Pass 1000 V
		C = 100 pF, R= 1500 Ω Other pads			N/A	Pass 3500 V	Pass 3500 V	Pass 3500 V
ESD MM	Electrostatic discharge (machine model)							
	AEC-Q100-003 JESD22-A115	C = 200 pF, R = 0 Ω	21	3	N/A	Pass 150 V	Pass 150 V	Pass 150 V
LU	Latch-up (current injection and overvoltage stress)							
	AEC-Q100-004 JESD78B	At maximum operating temperature (150 °C)	6	3	N/A	Class II Level A	Class II Level A	Class II Level A

1. See *Table 9: List of terms* for a definition of abbreviations.
2. First rejects after 5 million cycles.

.

Table 6. Package-oriented reliability test plan and result summary (SO8N / ST Shenzhen) [1]

Test	Test short description					
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size M24SR64-Y [2] Lot 1
PC	Preconditioning: moisture sensitivity level 1					
	JESD22-A113 J-STD-020D	MSL1, peak temperature at 260 °C, 3 IReflow	1145	1	N/A	0/1145
THB [3]	Temperature humidity bias					
	AEC-Q100-JESD22-A101	85 °C, 85% RH, bias 5.6 V	80	1	1008 hrs	0/80
TC [3]	Temperature cycling					
	AEC-Q100-JESD22-A104	–65 °C / +175 °C	80	1	1000 cycles	0/80
TMSK [3]	Thermal shocks					
	JESD22-A106	–55 °C / +125 °C	25	1	200 shocks	0/25
AC [3]	Autoclave (pressure pot)					
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	1	168 hrs	0/80
HTSL [3]	High temperature storage life					
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	1	1008 hrs	0/80
ELFR [3]	Early failure life rate					
	AEC-Q100-008	HTOL 150 °C, 6V	800	1	48 hrs	0/800
ESD CDM	Electrostatic discharge (charge device model)					
	AEC-Q100-JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500 V

1. See *Table 9: List of terms* for a definition of abbreviations.
2. Larger memory array using the same silicon process technology in the same diffusion fab. Package qualification results of M24SR64-Y are applicable to M24SR16-Y.
3. THB-, TC-, TMSK-, AC-, HTSL- and ELFR- dedicated parts are first subject to preconditioning flow.

Table 7. Package-oriented reliability test plan and result summary (TSSOP8 / ST Shenzhen) (1)

Test	Test short description					
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size M24SR64-Y (2) Lot 1
PC	Preconditioning: moisture sensitivity level 1					
	JESD22-A113 J-STD-020D	MSL1, peak temperature at 260 °C, 3 IReflow	1145	1	N/A	0/1145
THB (3)	Temperature humidity bias					
	AEC-Q100-JESD22-A101	85 °C, 85% RH, bias 5.6 V	80	1	1008 hrs	0/80
TC (3)	Temperature cycling					
	AEC-Q100-JESD22-A104	–65 °C / +175 °C	80	1	1000 cycles	0/80
TMSK (3)	Thermal shocks					
	JESD22-A106	–55 °C / +125 °C	25	1	200 shocks	0/25
AC (3)	Autoclave (pressure pot)					
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	1	168 hrs	0/80
HTSL (3)	High temperature storage life					
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	1	1008 hrs	0/80
ELFR (3)	Early failure life rate					
	AEC-Q100-008	HTOL 150 °C, 6V	800	1	48 hrs	0/800
ESD CDM	Electrostatic discharge (charge device model)					
	AEC-Q100-JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500 V

1. See *Table 9: List of terms* for a definition of abbreviations.
2. Larger memory array using the same silicon process technology in the same diffusion fab. Package qualification results of M24SR64-Y are applicable to M24SR16-Y.
3. THB-, TC-, TMSK-, AC-, HTSL- and ELFR- dedicated parts are first subject to preconditioning flow.

Table 8. Package-oriented reliability test plan and result summary (UFDFPN8 MLP8 2 x 3 mm / ST Calamba) (1)

Test	Test short description					
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size M24SR64-Y (2) Lot 1
PC	Preconditioning: moisture sensitivity level 1					
	JESD22-A113 J-STD-020D	MSL1, peak temperature at 260 °C, 3 IReflow	345	1	N/A	0/345
THB (3)	Temperature humidity bias					
	AEC-Q100-JESD22-A101	85 °C, 85% RH, bias 5.6 V	80	1	1008 hrs	0/80
TC (3)	Temperature cycling					
	AEC-Q100-JESD22-A104	–65 °C / +175 °C	80	1	1000 cycles	0/80
TMSK (3)	Thermal shocks					
	JESD22-A106	–55 °C / +125 °C	25	1	200 shocks	0/25
AC (3)	Autoclave (pressure pot)					
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	1	168 hrs	0/80
HTSL (3)	High temperature storage life					
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	1	1008 hrs	0/80
ESD CDM	Electrostatic discharge (charge device model)					
	AEC-Q100-JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500 V

1. See *Table 9: List of terms* for a definition of abbreviations.
2. Larger memory array using the same silicon process technology in the same diffusion fab. Package qualification results of M24SR64-Y are applicable to M24SR16-Y.
3. THB-, TC-, TMSK-, AC-, and HTSL- dedicated parts are first subject to preconditioning flow.

4 Applicable and reference documents

- AEC-Q100: Stress test qualification for integrated circuits
- SOP 2.6.10: General product qualification procedure
- SOP 2.6.11: Program management fro product qualification
- SOP 2.6.12: Design criteria for product qualification
- SOP 2.6.14: Reliability requirements for product qualification
- SOP 2.6.19: Process maturity level
- SOP 2.6.2: Process qualification and transfer management
- SOP 2.6.20: New process / New product qualification
- SOP 2.6.7: Product maturity level
- SOP 2.6.9: Package and process maturity management in Back End
- SOP 2.7.5: Automotive products definition and status
- JESD22-A101: Steady state temperature humidity bias life test
- JESD22-A102: Accelerated moisture resistance - unbiased autoclave
- JESD22-A103: High temperature storage life
- JESD22-A104: Temperature cycling
- JESD22-A106: Thermal shock
- JESD22-A108: Temperature, bias, and operating life
- JESD22-A113: Preconditioning of nonhermetic surface mount devices prior to reliability testing
- JESD22-A114: Electrostatic discharge (ESD) sensitivity testing human body model (HBM)
- JESD22-A115: Electrostatic discharge (ESD) sensitivity testing machine model (MM)
- JESD78: IC Latch-up test
- J-STD-020D: Moisture/reflow sensitivity classification for nonhermetic solid state surface mount devices

5 Glossary

Table 9. List of terms

Terms	Description
EDR	NVM endurance, data retention and operational life
HTOL	High temperature operating life
LTOL	Low temperature operating life
HTB	High temperature bake
WEB	Program/Erase endurance cycling + bake
ESD HBM	Electrostatic discharge (human body model)
ESD MM	Electrostatic discharge (machine model)
LU	Latch-up
PC	Preconditioning (solder simulation)
THB	Temperature humidity bias
TC	Temperature cycling
TMSK	Thermal shocks
AC	Autoclave (pressure pot)
HTSL	High temperature storage life
ELFR	Early life failure rate
ESD CDM	Electrostatic discharge (charge device model)

6 Revision history

Table 10. Document revision history

Date	Revision	Changes
19-Dec-2013	1	Initial release.
27-Jan-2013	2	Updated list of qualified commercial products in *Table 1*. Added *Table 8: Package-oriented reliability test plan and result summary (UFDFPN8 MLP8 2 x 3 mm / ST Calamba)*.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

ST PRODUCTS ARE NOT DESIGNED OR AUTHORIZED FOR USE IN: (A) SAFETY CRITICAL APPLICATIONS SUCH AS LIFE SUPPORTING, ACTIVE IMPLANTED DEVICES OR SYSTEMS WITH PRODUCT FUNCTIONAL SAFETY REQUIREMENTS; (B) AERONAUTIC APPLICATIONS; (C) AUTOMOTIVE APPLICATIONS OR ENVIRONMENTS, AND/OR (D) AEROSPACE APPLICATIONS OR ENVIRONMENTS. WHERE ST PRODUCTS ARE NOT DESIGNED FOR SUCH USE, THE PURCHASER SHALL USE PRODUCTS AT PURCHASER’S SOLE RISK, EVEN IF ST HAS BEEN INFORMED IN WRITING OF SUCH USAGE, UNLESS A PRODUCT IS EXPRESSLY DESIGNATED BY ST AS BEING INTENDED FOR “AUTOMOTIVE, AUTOMOTIVE SAFETY OR MEDICAL” INDUSTRY DOMAINS ACCORDING TO ST PRODUCT DESIGN SPECIFICATIONS. PRODUCTS FORMALLY ESCC, QML OR JAN QUALIFIED ARE DEEMED SUITABLE FOR USE IN AEROSPACE BY THE CORRESPONDING GOVERNMENTAL AGENCY.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.
Information in this document supersedes and replaces all information previously supplied.
The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2014 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com

life.augmented

QRMMY1336
Qualification report

New product / M24SR04-Y using the CMOSF8H technology in the Rousset 8” Fab

Table 1. Product information

General information	
Commercial product	M24SR04-YMC6T/2 M24SR04-YMN6T/2 M24SR04-YDW6T/2
Product description	Dynamic NFC/RFID tag IC with 4-Kbit EEPROM, NFC Forum Type 4 Tag and I²C interface
Product group	MMS
Product division	MMY - Memory
Silicon process technology	CMOSF8H
Wafer fabrication location	RS8F - ST Rousset 8 inch, France
Electrical Wafer Sort test plant location	ST Rousset, France ST Toa Payoh, Singapore Subcontractor Ardentec, Singapore

Table 2. Package description

Package description	Assembly plant location	Final test plant location
SO8N	ST Shenzhen, China	ST Shenzhen, China
TSSOP8	ST Shenzhen, China	ST Shenzhen, China
UFDFPN8 (MLP8) 2 x 3 mm	ST Calamba, Philippines	ST Calamba, Philippines

Reliability / Qualification assessment: PASS

1 Reliability evaluation overview

1.1 Objectives

This qualification report summarizes the results of the reliability trials that were performed to qualify the new product M24SR04-Y using the CMOSF8H silicon process technology in the ST Rousset 8” diffusion fab.

The CMOSF8H is a new advanced silicon process technology that is already qualified in the ST Rousset 8” fab, and in production for EEPROM products and also for dual interface EEPROM M24LRxx products.

This document serves for the qualification of the named product using the named silicon process technology in the named diffusion fab.

The features covered by this document are:

- I^2C interface:
  - Two-wire I^2C serial interface supports 1 MHz protocol
  - Single supply voltage: 2.7 to 5.5 V
- Contactless interface:
  - NFC Forum Type 4 Tag
  - ISO/IEC 14443 Type A
  - 106 Kbps data rate

The temperature range covered by this document is:

- –40 to 85 °C

1.2 Conclusion

The new product M24SR04-Y using the CMOSF8H silicon process technology in the ST Rousset 8” diffusion fab has passed the reliability requirements and all products described in *Table 1* are qualified.

Refer to *Section 3: Reliability test results* for details on the reliability test results.

2 Device characteristics

Device description

The M24SR04-Y device is a dynamic NFC/RFID tag that can be accessed either from the I^2C or the RF interface. The RF and I^2C host can read or write to the same memory, that is why only one host can communicate at a time with the M24SR04-Y. The management of the interface selection is controlled by the M24SR04-Y device itself.

The RF interface is based on the ISO/IEC 14443 Type A standard. The M24SR04-Y is compatible with the NFC Forum Type 4 Tag specifications and supports all corresponding commands.

The I^2C interface uses a two-wire serial interface consisting of a bidirectional data line and a clock line. The devices carry a built-in 4-bit device type identifier code in accordance with the I^2C bus definition.

The device behaves as a slave in the I^2C protocol.

Refer to the product datasheet for more details.

3 Reliability test results

This section contains a general description of the reliability evaluation strategy. The named products are qualified using the standard STMicroelectronics corporate procedures for quality and reliability.

The product vehicle used for the die qualification is presented in *Table 3*.

Table 3. Product vehicle used for die qualification

Product	Silicon process technology	Wafer fabrication location	Package description	Assembly plant location
M24SR04-Y	CMOSF8H	ST Rousset 8”	CDIP24	Engineering assembly (1)

1. CDIP24 is a ceramic package used only for die-oriented reliability trials.

The package qualifications were mainly obtained by similarity. The product vehicle used for package qualifications is presented in *Table 4*.

Table 4. Product vehicle used for package qualification

<table>
<tr><th>Product</th><th>Silicon process technology</th><th>Wafer fabrication location</th><th>Package description</th><th>Assembly plant location</th></tr>
<tr><td rowspan="6">M24SR64-Y (1)</td><td rowspan="6">CMOSF8H</td><td rowspan="6">ST Rousset 8”</td><td rowspan="2">SO8N</td><td>ST Shenzhen</td></tr>
<tr><td>Subcon Amkor P1</td></tr>
<tr><td rowspan="2">TSSOP8</td><td>ST Shenzhen</td></tr>
<tr><td>Subcon Amkor P1</td></tr>
<tr><td rowspan="2">UFDFPN8 (MLP8) 2 x 3 mm</td><td>ST Calamba</td></tr>
<tr><td>Subcon Amkor P3</td></tr>
</table>

1. Larger memory array using the same silicon process technology in the same diffusion fab. Package qualification results of M24SR64-Y are applicable to M24SR04-Y.

3.1 Reliability test plan and result summary

The reliability test plan and the result summary are presented as follows:

- in *Table 5* for die-oriented tests
- in *Table 6* for SO8N ST Shenzhen package-oriented tests
- in *Table 7* for TSSOP8 ST Shenzhen package-oriented tests
- in *Table 8* for UFDFPN8 (MLP8) 2 x 3 mm ST Calamba package-oriented tests

Reliability tests on all other packages are planned, but results are not yet available.

Table 5. Die-oriented reliability test plan and result summary (CDIP8 / Engineering package)(1)

Test	Test short description							
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size		
						M24SR04-Y		
						Lot 1	Lot 2	Lot 3
EDR	High temperature operating life after endurance							
	AEC-Q100-005	1 million E/W cycles at 25 °C then: HTOL 150 °C, 6 V	80	3	1008 hrs	0/80	0/80	0/80
	Data retention after endurance							
	AEC-Q100-005	1 million E/W cycles at 25 °C then: HTSL at 150 °C	80	3	1008 hrs	0/80	0/80	0/80
LTOL	Low temperature operating life							
	JESD22-A108	–40 °C, 6 V	80	3	1008 hrs	0/80	0/80	0/80
WEB	Program/erase endurance cycling + bake							
	Internal spec.	1 million E/W cycles at 25 °C then: Retention bake at 200 °C / 48 hours	80	3	1 Million cycles / 48 hrs	0/80 (2)	0/80 (2)	0/80 (2)
ESD HBM	Electrostatic discharge (human body model)							
	AEC-Q100-002 JESD22-A114	C = 100 pF, R= 1500 Ω pads AC0, AC1	27	3	N/A	Pass 1000 V	Pass 1000 V	Pass 1000 V
		C = 100 pF, R= 1500 Ω Other pads			N/A	Pass 3500 V	Pass 3500 V	Pass 3500 V
ESD MM	Electrostatic discharge (machine model)							
	AEC-Q100-003 JESD22-A115	C = 200 pF, R = 0 Ω	21	3	N/A	Pass 150 V	Pass 150 V	Pass 150 V
LU	Latch-up (current injection and overvoltage stress)							
	AEC-Q100-004 JESD78B	At maximum operating temperature (150 °C)	6	3	N/A	Class II Level A	Class II Level A	Class II Level A

1. See *Table 9: List of terms* for a definition of abbreviations.
2. First rejects after 5 million cycles.

.

Table 6. Package-oriented reliability test plan and result summary (SO8N / ST Shenzhen) (1)

Test	Test short description					
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size M24SR64-Y (2) Lot 1
PC	Preconditioning: moisture sensitivity level 1					
	JESD22-A113 J-STD-020D	MSL1, peak temperature at 260 °C, 3 IReflow	1145	1	N/A	0/1145
THB (3)	Temperature humidity bias					
	AEC-Q100-JESD22-A101	85 °C, 85% RH, bias 5.6 V	80	1	1008 hrs	0/80
TC (3)	Temperature cycling					
	AEC-Q100-JESD22-A104	–65 °C / +175 °C	80	1	1000 cycles	0/80
TMSK (3)	Thermal shocks					
	JESD22-A106	–55 °C / +125 °C	25	1	200 shocks	0/25
AC (3)	Autoclave (pressure pot)					
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	1	168 hrs	0/80
HTSL (3)	High temperature storage life					
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	1	1008 hrs	0/80
ELFR (3)	Early failure life rate					
	AEC-Q100-008	HTOL 150 °C, 6V	800	1	48 hrs	0/800
ESD CDM	Electrostatic discharge (charge device model)					
	AEC-Q100-JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500 V

1. See *Table 9: List of terms* for a definition of abbreviations.
2. Larger memory array using the same silicon process technology in the same diffusion fab. Package qualification results of M24SR64-Y are applicable to M24SR04-Y.
3. THB-, TC-, TMSK-, AC-, HTSL- and ELFR- dedicated parts are first subject to preconditioning flow.

Table 7. Package-oriented reliability test plan and result summary (TSSOP8 / ST Shenzhen) (1)

Test	Test short description					Results fail / sample size M24SR64-Y (2) Lot 1
	Method	Conditions	Sample size / lots	No. of lots	Duration	
PC	Preconditioning: moisture sensitivity level 1					
	JESD22-A113 J-STD-020D	MSL1, peak temperature at 260 °C, 3 IReflow	1145	1	N/A	0/1145
THB (3)	Temperature humidity bias					
	AEC-Q100-JESD22-A101	85 °C, 85% RH, bias 5.6 V	80	1	1008 hrs	0/80
TC (3)	Temperature cycling					
	AEC-Q100-JESD22-A104	–65 °C / +175 °C	80	1	1000 cycles	0/80
TMSK (3)	Thermal shocks					
	JESD22-A106	–55 °C / +125 °C	25	1	200 shocks	0/25
AC (3)	Autoclave (pressure pot)					
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	1	168 hrs	0/80
HTSL (3)	High temperature storage life					
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	1	1008 hrs	0/80
ELFR (3)	Early failure life rate					
	AEC-Q100-008	HTOL 150 °C, 6V	800	1	48 hrs	0/800
ESD CDM	Electrostatic discharge (charge device model)					
	AEC-Q100-JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500 V

1. See *Table 9: List of terms* for a definition of abbreviations.
2. Larger memory array using the same silicon process technology in the same diffusion fab. Package qualification results of M24SR64-Y are applicable to M24SR04-Y.
3. THB-, TC-, TMSK-, AC-, HTSL- and ELFR- dedicated parts are first subject to preconditioning flow.

Table 8. Package-oriented reliability test plan and result summary (UFDFPN8 MLP8 2 x 3 mm / ST Calamba) (1)

Test	Test short description					
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size M24SR64-Y (2) Lot 1
PC	Preconditioning: moisture sensitivity level 1					
	JESD22-A113 J-STD-020D	MSL1, peak temperature at 260 °C, 3 IReflow	345	1	N/A	0/345
THB (3)	Temperature humidity bias					
	AEC-Q100-JESD22-A101	85 °C, 85% RH, bias 5.6 V	80	1	1008 hrs	0/80
TC (3)	Temperature cycling					
	AEC-Q100-JESD22-A104	–65 °C / +175 °C	80	1	1000 cycles	0/80
TMSK (3)	Thermal shocks					
	JESD22-A106	–55 °C / +125 °C	25	1	200 shocks	0/25
AC (3)	Autoclave (pressure pot)					
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	1	168 hrs	0/80
HTSL (3)	High temperature storage life					
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	1	1008 hrs	0/80
ESD CDM	Electrostatic discharge (charge device model)					
	AEC-Q100-JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500 V

1. See *Table 9: List of terms* for a definition of abbreviations.
2. Larger memory array using the same silicon process technology in the same diffusion fab. Package qualification results of M24SR64-Y are applicable to M24SR04-Y.
3. THB-, TC-, TMSK-, AC- and HTSL- dedicated parts are first subject to preconditioning flow.

4 Applicable and reference documents

- AEC-Q100: Stress test qualification for integrated circuits
- SOP 2.6.10: General product qualification procedure
- SOP 2.6.11: Program management fro product qualification
- SOP 2.6.12: Design criteria for product qualification
- SOP 2.6.14: Reliability requirements for product qualification
- SOP 2.6.19: Process maturity level
- SOP 2.6.2: Process qualification and transfer management
- SOP 2.6.20: New process / New product qualification
- SOP 2.6.7: Product maturity level
- SOP 2.6.9: Package and process maturity management in Back End
- SOP 2.7.5: Automotive products definition and status
- JESD22-A101: Steady state temperature humidity bias life test
- JESD22-A102: Accelerated moisture resistance - unbiased autoclave
- JESD22-A103: High temperature storage life
- JESD22-A104: Temperature cycling
- JESD22-A106: Thermal shock
- JESD22-A108: Temperature, bias, and operating life
- JESD22-A113: Preconditioning of nonhermetic surface mount devices prior to reliability testing
- JESD22-A114: Electrostatic discharge (ESD) sensitivity testing human body model (HBM)
- JESD22-A115: Electrostatic discharge (ESD) sensitivity testing machine model (MM)
- JESD78: IC Latch-up test
- J-STD-020D: Moisture/reflow sensitivity classification for nonhermetic solid state surface mount devices

5 Glossary

Table 9. List of terms

Terms	Description
EDR	NVM endurance, data retention and operational life
HTOL	High temperature operating life
LTOL	Low temperature operating life
HTB	High temperature bake
WEB	Program/Erase endurance cycling + bake
ESD HBM	Electrostatic discharge (human body model)
ESD MM	Electrostatic discharge (machine model)
LU	Latch-up
PC	Preconditioning (solder simulation)
THB	Temperature humidity bias
TC	Temperature cycling
TMSK	Thermal shocks
AC	Autoclave (pressure pot)
HTSL	High temperature storage life
ELFR	Early life failure rate
ESD CDM	Electrostatic discharge (charge device model)

6 Revision history

Table 10. Document revision history

Date	Revision	Changes
20-Dec-2013	1	Initial release.
27-Jan-2013	2	Updated list of qualified commercial products in *Table 1*. Added *Table 8: Package-oriented reliability test plan and result summary (UFDFPN8 MLP8 2 x 3 mm / ST Calamba)*.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

ST PRODUCTS ARE NOT DESIGNED OR AUTHORIZED FOR USE IN: (A) SAFETY CRITICAL APPLICATIONS SUCH AS LIFE SUPPORTING, ACTIVE IMPLANTED DEVICES OR SYSTEMS WITH PRODUCT FUNCTIONAL SAFETY REQUIREMENTS; (B) AERONAUTIC APPLICATIONS; (C) AUTOMOTIVE APPLICATIONS OR ENVIRONMENTS, AND/OR (D) AEROSPACE APPLICATIONS OR ENVIRONMENTS. WHERE ST PRODUCTS ARE NOT DESIGNED FOR SUCH USE, THE PURCHASER SHALL USE PRODUCTS AT PURCHASER’S SOLE RISK, EVEN IF ST HAS BEEN INFORMED IN WRITING OF SUCH USAGE, UNLESS A PRODUCT IS EXPRESSLY DESIGNATED BY ST AS BEING INTENDED FOR “AUTOMOTIVE, AUTOMOTIVE SAFETY OR MEDICAL” INDUSTRY DOMAINS ACCORDING TO ST PRODUCT DESIGN SPECIFICATIONS. PRODUCTS FORMALLY ESCC, QML OR JAN QUALIFIED ARE DEEMED SUITABLE FOR USE IN AEROSPACE BY THE CORRESPONDING GOVERNMENTAL AGENCY.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.
Information in this document supersedes and replaces all information previously supplied.
The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2014 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com

life.augmented

QRMMY1337
Qualification report

New product / M24SR02-Y using the CMOSF8H technology in the Rousset 8” Fab

Table 1. Product information

General information	
Commercial product	M24SR02-YMC6T/2 M24SR02-YMN6T/2 M24SR02-YDW6T/2
Product description	Dynamic NFC/RFID tag IC with 2-Kbit EEPROM, NFC Forum Type 4 Tag and I²C interface
Product group	MMS
Product division	MMY - Memory
Silicon process technology	CMOSF8H
Wafer fabrication location	RS8F - ST Rousset 8 inch, France
Electrical Wafer Sort test plant location	ST Rousset, France ST Toa Payoh, Singapore Subcontractor Ardentec, Singapore

Table 2. Package description

Package description	Assembly plant location	Final test plant location
SO8N	ST Shenzhen, China	ST Shenzhen, China
TSSOP8	ST Shenzhen, China	ST Shenzhen, China
UFDFPN8 (MLP8) 2 x 3 mm	ST Calamba, Philippines	ST Calamba, Philippines

Reliability / Qualification assessment: PASS

1 Reliability evaluation overview

1.1 Objectives

This qualification report summarizes the results of the reliability trials that were performed to qualify the new product M24SR02-Y using the CMOSF8H silicon process technology in the ST Rousset 8” diffusion fab.

The CMOSF8H is a new advanced silicon process technology that is already qualified in the ST Rousset 8” fab, and in production for EEPROM products and also for dual interface EEPROM M24LRxx products.

This document serves for the qualification of the named product using the named silicon process technology in the named diffusion fab.

The features covered by this document are:

- I^2C interface:
  - Two-wire I^2C serial interface supports 1 MHz protocol
  - Single supply voltage: 2.7 to 5.5 V
- Contactless interface:
  - NFC Forum Type 4 Tag
  - ISO/IEC 14443 Type A
  - 106 Kbps data rate

The temperature range covered by this document is:

- –40 to 85 °C

1.2 Conclusion

The new product M24SR02-Y using the CMOSF8H silicon process technology in the ST Rousset 8” diffusion fab has passed the reliability requirements and all products described in *Table 1* are qualified.

Refer to *Section 3: Reliability test results* for details on the reliability test results.

2 Device characteristics

Device description

The M24SR02-Y device is a dynamic NFC/RFID tag that can be accessed either from the I^2C or the RF interface. The RF and I^2C host can read or write to the same memory, that is why only one host can communicate at a time with the M24SR02-Y. The management of the interface selection is controlled by the M24SR02-Y device itself.

The RF interface is based on the ISO/IEC 14443 Type A standard. The M24SR02-Y is compatible with the NFC Forum Type 4 Tag specifications and supports all corresponding commands.

The I^2C interface uses a two-wire serial interface consisting of a bidirectional data line and a clock line. The devices carry a built-in 4-bit device type identifier code in accordance with the I^2C bus definition.

The device behaves as a slave in the I^2C protocol.

Refer to the product datasheet for more details.

3 Reliability test results

This section contains a general description of the reliability evaluation strategy. The named products are qualified using the standard STMicroelectronics corporate procedures for quality and reliability.

The product vehicle used for the die qualification is presented in *Table 3*.

Table 3. Product vehicle used for die qualification

Product	Silicon process technology	Wafer fabrication location	Package description	Assembly plant location
M24SR02-Y	CMOSF8H	ST Rousset 8”	CDIP24	Engineering assembly [1]

1. CDIP24 is a ceramic package used only for die-oriented reliability trials.

The package qualifications were mainly obtained by similarity. The product vehicle used for package qualifications is presented in *Table 4*.

Table 4. Product vehicle used for package qualification

Product	Silicon process technology	Wafer fabrication location	Package description	Assembly plant location
M24SR64-Y [1]	CMOSF8H	ST Rousset 8”	SO8N	ST Shenzhen
				Subcon Amkor P1
			TSSOP8	ST Shenzhen
				Subcon Amkor P1
			UFDFPN8 (MLP8) 2 x 3 mm	ST Calamba
				Subcon Amkor P3

1. Larger memory array using the same silicon process technology in the same diffusion fab. Package qualification results of M24SR64-Y are applicable to M24SR02-Y.

3.1 Reliability test plan and result summary

The reliability test plan and the result summary are presented as follows:

- in *Table 5* for die-oriented tests
- in *Table 6* for SO8N ST Shenzhen package-oriented tests
- in *Table 7* for TSSOP8 ST Shenzhen package-oriented tests
- in *Table 8* for UFDFPN8 (MLP8) 2 x 3 mm ST Calamba package-oriented tests

Reliability tests on all other packages are planned, but results are not yet available.

Table 5. Die-oriented reliability test plan and result summary (CDIP8 / Engineering package)[1]

Test	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size M24SR02-Y Lot 1	Lot 2	Lot 3
EDR	High temperature operating life after endurance							
	AEC-Q100-005	1 million E/W cycles at 25 °C then: HTOL 150 °C, 6 V	80	3	1008 hrs	0/80	0/80	0/80
	Data retention after endurance							
	AEC-Q100-005	1 million E/W cycles at 25 °C then: HTSL at 150 °C	80	3	1008 hrs	0/80	0/80	0/80
LTOL	Low temperature operating life							
	JESD22-A108	–40 °C, 6 V	80	3	1008 hrs	0/80	0/80	0/80
WEB	Program/erase endurance cycling + bake							
	Internal spec.	1 million E/W cycles at 25 °C then: Retention bake at 200 °C / 48 hours	80	3	1 Million cycles / 48 hrs	0/80 [2]	0/80 [2]	0/80 [2]
ESD HBM	Electrostatic discharge (human body model)							
	AEC-Q100-002 JESD22-A114	C = 100 pF, R= 1500 Ω pads AC0, AC1	27	3	N/A	Pass 1000 V	Pass 1000 V	Pass 1000 V
		C = 100 pF, R= 1500 Ω Other pads			N/A	Pass 3500 V	Pass 3500 V	Pass 3500 V
ESD MM	Electrostatic discharge (machine model)							
	AEC-Q100-003 JESD22-A115	C = 200 pF, R = 0 Ω	21	3	N/A	Pass 150 V	Pass 150 V	Pass 150 V
LU	Latch-up (current injection and overvoltage stress)							
	AEC-Q100-004 JESD78B	At maximum operating temperature (150 °C)	6	3	N/A	Class II Level A	Class II Level A	Class II Level A

1. See *Table 9: List of terms* for a definition of abbreviations.
2. First rejects after 5 million cycles.

.

Table 6. Package-oriented reliability test plan and result summary (SO8N / ST Shenzhen) (1)

Test	Test short description					
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size M24SR64-Y (2) Lot 1
PC	Preconditioning: moisture sensitivity level 1					
	JESD22-A113 J-STD-020D	MSL1, peak temperature at 260 °C, 3 IReflow	1145	1	N/A	0/1145
THB (3)	Temperature humidity bias					
	AEC-Q100-JESD22-A101	85 °C, 85% RH, bias 5.6 V	80	1	1008 hrs	0/80
TC (3)	Temperature cycling					
	AEC-Q100-JESD22-A104	–65 °C / +175 °C	80	1	1000 cycles	0/80
TMSK (3)	Thermal shocks					
	JESD22-A106	–55 °C / +125 °C	25	1	200 shocks	0/25
AC (3)	Autoclave (pressure pot)					
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	1	168 hrs	0/80
HTSL (3)	High temperature storage life					
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	1	1008 hrs	0/80
ELFR (3)	Early failure life rate					
	AEC-Q100-008	HTOL 150 °C, 6V	800	1	48 hrs	0/800
ESD CDM	Electrostatic discharge (charge device model)					
	AEC-Q100-JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500 V

1. See *Table 9: List of terms* for a definition of abbreviations.
2. Larger memory array using the same silicon process technology in the same diffusion fab. Package qualification results of M24SR64-Y are applicable to M24SR02-Y.
3. THB-, TC-, TMSK-, AC-, HTSL- and ELFR- dedicated parts are first subject to preconditioning flow.

Table 7. Package-oriented reliability test plan and result summary (TSSOP8 / ST Shenzhen) [(1)]

Test	Test short description					
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size M24SR64-Y [(2)] Lot 1
PC	Preconditioning: moisture sensitivity level 1					
	JESD22-A113 J-STD-020D	MSL1, peak temperature at 260 °C, 3 IReflow	1145	1	N/A	0/1145
THB (3)	Temperature humidity bias					
	AEC-Q100-JESD22-A101	85 °C, 85% RH, bias 5.6 V	80	1	1008 hrs	0/80
TC (3)	Temperature cycling					
	AEC-Q100-JESD22-A104	–65 °C / +175 °C	80	1	1000 cycles	0/80
TMSK (3)	Thermal shocks					
	JESD22-A106	–55 °C / +125 °C	25	1	200 shocks	0/25
AC (3)	Autoclave (pressure pot)					
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	1	168 hrs	0/80
HTSL (3)	High temperature storage life					
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	1	1008 hrs	0/80
ELFR (3)	Early failure life rate					
	AEC-Q100-008	HTOL 150 °C, 6V	800	1	48 hrs	0/800
ESD CDM	Electrostatic discharge (charge device model)					
	AEC-Q100-JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500 V

1. See *Table 9: List of terms* for a definition of abbreviations.
2. Larger memory array using the same silicon process technology in the same diffusion fab. Package qualification results of M24SR64-Y are applicable to M24SR02-Y.
3. THB-, TC-, TMSK-, AC-, HTSL- and ELFR- dedicated parts are first subject to preconditioning flow.

Table 8. Package-oriented reliability test plan and result summary (UFDFPN8 MLP8 2 x 3 mm / ST Calamba) [1]

Test	Test short description					Results fail / sample size M24SR64-Y [2] Lot 1
	Method	**Conditions**	**Sample size / lots**	**No. of lots**	**Duration**	**Lot 1**
PC	Preconditioning: moisture sensitivity level 1					
	JESD22-A113 J-STD-020D	MSL1, peak temperature at 260 °C, 3 IReflow	345	1	N/A	0/345
THB [3]	Temperature humidity bias					
	AEC-Q100-JESD22-A101	85 °C, 85% RH, bias 5.6 V	80	1	1008 hrs	0/80
TC [3]	Temperature cycling					
	AEC-Q100-JESD22-A104	–65 °C / +175 °C	80	1	1000 cycles	0/80
TMSK [3]	Thermal shocks					
	JESD22-A106	–55 °C / +125 °C	25	1	200 shocks	0/25
AC [3]	Autoclave (pressure pot)					
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	1	168 hrs	0/80
HTSL [3]	High temperature storage life					
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	1	1008 hrs	0/80
ESD CDM	Electrostatic discharge (charge device model)					
	AEC-Q100-JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500 V

1. See *Table 9: List of terms* for a definition of abbreviations.
2. Larger memory array using the same silicon process technology in the same diffusion fab. Package qualification results of M24SR64-Y are applicable to M24SR02-Y.
3. THB-, TC-, TMSK-, AC- and HTSL- dedicated parts are first subject to preconditioning flow.

4 Applicable and reference documents

- AEC-Q100: Stress test qualification for integrated circuits
- SOP 2.6.10: General product qualification procedure
- SOP 2.6.11: Program management fro product qualification
- SOP 2.6.12: Design criteria for product qualification
- SOP 2.6.14: Reliability requirements for product qualification
- SOP 2.6.19: Process maturity level
- SOP 2.6.2: Process qualification and transfer management
- SOP 2.6.20: New process / New product qualification
- SOP 2.6.7: Product maturity level
- SOP 2.6.9: Package and process maturity management in Back End
- SOP 2.7.5: Automotive products definition and status
- JESD22-A101: Steady state temperature humidity bias life test
- JESD22-A102: Accelerated moisture resistance - unbiased autoclave
- JESD22-A103: High temperature storage life
- JESD22-A104: Temperature cycling
- JESD22-A106: Thermal shock
- JESD22-A108: Temperature, bias, and operating life
- JESD22-A113: Preconditioning of nonhermetic surface mount devices prior to reliability testing
- JESD22-A114: Electrostatic discharge (ESD) sensitivity testing human body model (HBM)
- JESD22-A115: Electrostatic discharge (ESD) sensitivity testing machine model (MM)
- JESD78: IC Latch-up test
- J-STD-020D: Moisture/reflow sensitivity classification for nonhermetic solid state surface mount devices

5 Glossary

Table 9. List of terms

Terms	Description
EDR	NVM endurance, data retention and operational life
HTOL	High temperature operating life
LTOL	Low temperature operating life
HTB	High temperature bake
WEB	Program/Erase endurance cycling + bake
ESD HBM	Electrostatic discharge (human body model)
ESD MM	Electrostatic discharge (machine model)
LU	Latch-up
PC	Preconditioning (solder simulation)
THB	Temperature humidity bias
TC	Temperature cycling
TMSK	Thermal shocks
AC	Autoclave (pressure pot)
HTSL	High temperature storage life
ELFR	Early life failure rate
ESD CDM	Electrostatic discharge (charge device model)

6 Revision history

Table 10. Document revision history

Date	Revision	Changes
19-Dec-2013	1	Initial release.
28-Jan-2013	2	Updated list of qualified commercial products in *Table 1*. Added *Table 8: Package-oriented reliability test plan and result summary (UFDFPN8 MLP8 2 x 3 mm / ST Calamba)*

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

ST PRODUCTS ARE NOT DESIGNED OR AUTHORIZED FOR USE IN: (A) SAFETY CRITICAL APPLICATIONS SUCH AS LIFE SUPPORTING, ACTIVE IMPLANTED DEVICES OR SYSTEMS WITH PRODUCT FUNCTIONAL SAFETY REQUIREMENTS; (B) AERONAUTIC APPLICATIONS; (C) AUTOMOTIVE APPLICATIONS OR ENVIRONMENTS, AND/OR (D) AEROSPACE APPLICATIONS OR ENVIRONMENTS. WHERE ST PRODUCTS ARE NOT DESIGNED FOR SUCH USE, THE PURCHASER SHALL USE PRODUCTS AT PURCHASER’S SOLE RISK, EVEN IF ST HAS BEEN INFORMED IN WRITING OF SUCH USAGE, UNLESS A PRODUCT IS EXPRESSLY DESIGNATED BY ST AS BEING INTENDED FOR “AUTOMOTIVE, AUTOMOTIVE SAFETY OR MEDICAL” INDUSTRY DOMAINS ACCORDING TO ST PRODUCT DESIGN SPECIFICATIONS. PRODUCTS FORMALLY ESCC, QML OR JAN QUALIFIED ARE DEEMED SUITABLE FOR USE IN AEROSPACE BY THE CORRESPONDING GOVERNMENTAL AGENCY.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.
Information in this document supersedes and replaces all information previously supplied.
The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2014 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com

life.augmented

QRMMY1404
Qualification report

New product / SRTAG2K-D using the CMOSF8H technology in the Rousset 8” Fab

Table 1. Product information

General information	
Commercial product	SRTAG2K-DMC6T/2
Product description	NFC Forum Type 4 Tag IC with 2-Kbit EEPROM and RF Session digital output
Product group	MMS
Product division	MMY - Memory
Silicon process technology	CMOSF8H
Wafer fabrication location	RS8F - ST Rousset 8 inch, France
Electrical Wafer Sort test plant location	ST Rousset, France ST Toa Payoh, Singapore Subcontractor Ardentec, Singapore

Table 2. Package description

Package description	Assembly plant location	Final test plant location
UFDFPN8 (MLP8) 2 x 3 mm	ST Calamba, Philippines	ST Calamba, Philippines

Reliability / Qualification assessment: PASS

1 Reliability evaluation overview

1.1 Objectives

This qualification report summarizes the results of the reliability trials that were performed to qualify the new product SRTAG2K-D using the CMOSF8H silicon process technology in the ST Rousset 8” diffusion fab.

The CMOSF8H is a new advanced silicon process technology that is already qualified in the ST Rousset 8” fab, and in production for EEPROM products and also for dual interface EEPROM M24LRxx products.

This document serves for the qualification of the named product using the named silicon process technology in the named diffusion fab.

The features covered by this document are:

- Contactless interface:
  - NFC Forum Type 4 Tag
  - ISO/IEC 14443 Type A
  - 106 Kbps data rate

The temperature range covered by this document is:

- –40 to 85 °C

1.2 Conclusion

The new product SRTAG2K-D using the CMOSF8H silicon process technology in the ST Rousset 8” diffusion fab has passed the reliability requirements and all products described in *Table 1* are qualified.

Refer to *Section 3: Reliability test results* for details on the reliability test results.

2 Device characteristics

Device description

The SRTAG2K-D device is a dynamic NFC/RFID tag that can be accessed from the RF interface. The RF interface is based on the ISO/IEC 14443 Type A standard.
The SRTAG2K-D is compatible with the NFC Forum Type 4 Tag specifications and supports all corresponding commands.

Refer to the product datasheet for more details.

3 Reliability test results

This section contains a general description of the reliability evaluation strategy. The named products are qualified using the standard STMicroelectronics corporate procedures for quality and reliability.

The product vehicle used for the die qualification is presented in *Table 3*.

Table 3. Product vehicle used for die qualification

Product	Silicon process technology	Wafer fabrication location	Package description	Assembly plant location
M24SR02-Y (1)	CMOSF8H	ST Rousset 8”	CDIP24	Engineering assembly (2)

1. Die-oriented reliability trials of M24SR02-Y are applicable to SRTAG2K-D (same design core, same silicon process technology).
2. CDIP24 is a ceramic package used only for die-oriented reliability trials.

The package qualifications were mainly obtained by similarity. The product vehicle used for package qualifications is presented in *Table 4*.

Table 4. Product vehicle used for package qualification

Product	Silicon process technology	Wafer fabrication location	Package description	Assembly plant location
M24SR64-Y (1)	CMOSF8H	ST Rousset 8”	UFDFPN8 (MLP8) 2 x 3 mm	ST Calamba Subcon Amkor P3

1. Larger memory array using the same silicon process technology in the same diffusion fab. Package qualification results of M24SR64-Y are applicable to SRTAG2K-D.

3.1 Reliability test plan and result summary

The reliability test plan and the result summary are presented as follows:

- in *Table 5* for die-oriented tests
- in *Table 6* for UFDFPN8 (MLP8) 2 x 3 mm ST Calamba package-oriented tests

Table 5. Die-oriented reliability test plan and result summary (CDIP8 / Engineering package)[1]

Test	Test short description							
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size M24SR02-Y [2]		
						Lot 1	Lot 2	Lot 3
EDR	High temperature operating life after endurance							
	AEC-Q100-005	1 million E/W cycles at 25 °C then: HTOL 150 °C, 6 V	80	3	1008 hrs	0/80	0/80	0/80
	Data retention after endurance							
	AEC-Q100-005	1 million E/W cycles at 25 °C then: HTSL at 150 °C	80	3	1008 hrs	0/80	0/80	0/80
LTOL	Low temperature operating life							
	JESD22-A108	–40 °C, 6 V	80	3	1008 hrs	0/80	0/80	0/80
WEB	Program/erase endurance cycling + bake							
	Internal spec.	1 million E/W cycles at 25 °C then: Retention bake at 200 °C / 48 hours	80	3	1 Million cycles / 48 hrs	0/80 [3]	0/80 [3]	0/80 [3]
ESD HBM	Electrostatic discharge (human body model)							
	AEC-Q100-002 JESD22-A114	C = 100 pF, R= 1500 Ω pads AC0, AC1	27	3	N/A	Pass 1000 V	Pass 1000 V	Pass 1000 V
		C = 100 pF, R= 1500 Ω Other pads			N/A	Pass 3500 V	Pass 3500 V	Pass 3500 V
ESD MM	Electrostatic discharge (machine model)							
	AEC-Q100-003 JESD22-A115	C = 200 pF, R = 0 Ω	21	3	N/A	Pass 150 V	Pass 150 V	Pass 150 V
LU	Latch-up (current injection and overvoltage stress)							
	AEC-Q100-004 JESD78B	At maximum operating temperature (150 °C)	6	3	N/A	Class II Level A	Class II Level A	Class II Level A

1. See *Table 7: List of terms* for a definition of abbreviations.
2. Die-oriented reliability trials of M24SR02-Y are applicable to SRTAG2K-D (same design core, same silicon process technology).
3. First rejects after 5 million cycles.

.

Table 6. Package-oriented reliability test plan and result summary (UFDFPN8 MLP8 2 x 3 mm / ST Calamba) (1)

Test	Test short description					
	Method	Conditions	Sample size / lots	No. of lots	Duration	Results fail / sample size M24SR64-Y (2) Lot 1
PC	Preconditioning: moisture sensitivity level 1					
	JESD22-A113 J-STD-020D	MSL1, peak temperature at 260 °C, 3 IReflow	345	1	N/A	0/345
THB (3)	Temperature humidity bias					
	AEC-Q100-JESD22-A101	85 °C, 85% RH, bias 5.6 V	80	1	1008 hrs	0/80
TC (3)	Temperature cycling					
	AEC-Q100-JESD22-A104	–65 °C / +175 °C	80	1	1000 cycles	0/80
TMSK (3)	Thermal shocks					
	JESD22-A106	–55 °C / +125 °C	25	1	200 shocks	0/25
AC (3)	Autoclave (pressure pot)					
	AEC-Q100-JESD22-A102	121 °C, 100% RH at 2 ATM	80	1	168 hrs	0/80
HTSL (3)	High temperature storage life					
	AEC-Q100-JESD22-A103	Retention bake at 150 °C	80	1	1008 hrs	0/80
ESD CDM	Electrostatic discharge (charge device model)					
	AEC-Q100-JESD22-C101	Field induced charging method	18	1	N/A	Pass >1500 V

1. See *Table 7: List of terms* for a definition of abbreviations.
2. Larger memory array using the same silicon process technology in the same diffusion fab. Package qualification results of M24SR64-Y are applicable to SRTAG2K-D.
3. THB-, TC-, TMSK-, AC- and HTSL- dedicated parts are first subject to preconditioning flow.

4 Applicable and reference documents

- AEC-Q100: Stress test qualification for integrated circuits
- SOP 2.6.10: General product qualification procedure
- SOP 2.6.11: Program management fro product qualification
- SOP 2.6.12: Design criteria for product qualification
- SOP 2.6.14: Reliability requirements for product qualification
- SOP 2.6.19: Process maturity level
- SOP 2.6.2: Process qualification and transfer management
- SOP 2.6.20: New process / New product qualification
- SOP 2.6.7: Product maturity level
- SOP 2.6.9: Package and process maturity management in Back End
- SOP 2.7.5: Automotive products definition and status
- JESD22-A101: Steady state temperature humidity bias life test
- JESD22-A102: Accelerated moisture resistance - unbiased autoclave
- JESD22-A103: High temperature storage life
- JESD22-A104: Temperature cycling
- JESD22-A106: Thermal shock
- JESD22-A108: Temperature, bias, and operating life
- JESD22-A113: Preconditioning of nonhermetic surface mount devices prior to reliability testing
- JESD22-A114: Electrostatic discharge (ESD) sensitivity testing human body model (HBM)
- JESD22-A115: Electrostatic discharge (ESD) sensitivity testing machine model (MM)
- JESD78: IC Latch-up test
- J-STD-020D: Moisture/reflow sensitivity classification for nonhermetic solid state surface mount devices

5 Glossary

Table 7. List of terms

Terms	Description
EDR	NVM endurance, data retention and operational life
HTOL	High temperature operating life
LTOL	Low temperature operating life
HTB	High temperature bake
WEB	Program/Erase endurance cycling + bake
ESD HBM	Electrostatic discharge (human body model)
ESD MM	Electrostatic discharge (machine model)
LU	Latch-up
PC	Preconditioning (solder simulation)
THB	Temperature humidity bias
TC	Temperature cycling
TMSK	Thermal shocks
AC	Autoclave (pressure pot)
HTSL	High temperature storage life
ELFR	Early life failure rate
ESD CDM	Electrostatic discharge (charge device model)

6 Revision history

Table 8. Document revision history

Date	Revision	Changes
29-Jan-2014	1	Initial release.

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

ST PRODUCTS ARE NOT DESIGNED OR AUTHORIZED FOR USE IN: (A) SAFETY CRITICAL APPLICATIONS SUCH AS LIFE SUPPORTING, ACTIVE IMPLANTED DEVICES OR SYSTEMS WITH PRODUCT FUNCTIONAL SAFETY REQUIREMENTS; (B) AERONAUTIC APPLICATIONS; (C) AUTOMOTIVE APPLICATIONS OR ENVIRONMENTS, AND/OR (D) AEROSPACE APPLICATIONS OR ENVIRONMENTS. WHERE ST PRODUCTS ARE NOT DESIGNED FOR SUCH USE, THE PURCHASER SHALL USE PRODUCTS AT PURCHASER’S SOLE RISK, EVEN IF ST HAS BEEN INFORMED IN WRITING OF SUCH USAGE, UNLESS A PRODUCT IS EXPRESSLY DESIGNATED BY ST AS BEING INTENDED FOR “AUTOMOTIVE, AUTOMOTIVE SAFETY OR MEDICAL” INDUSTRY DOMAINS ACCORDING TO ST PRODUCT DESIGN SPECIFICATIONS. PRODUCTS FORMALLY ESCC, QML OR JAN QUALIFIED ARE DEEMED SUITABLE FOR USE IN AEROSPACE BY THE CORRESPONDING GOVERNMENTAL AGENCY.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.
Information in this document supersedes and replaces all information previously supplied.
The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2014 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com

Document Revision History

Date	Rev.	Description of the Revision
January 28, 2014	1.00	Document creation

Source Documents & Reference Documents

Source document Title	**Rev.:**	**Date:**

Please Read Carefully:

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries(“ST”) reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST’s terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

UNLESS OTHERWISE SET FORTH IN ST’S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND / OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.

ST PRODUCTS ARE NOT DESIGNED OR AUTHORIZED FOR USE IN: (A) SAFETY CRITICAL APPLICATIONS SUCH AS LIFE SUPPORTING, ACTIVE IMPLANTED DEVICES OR SYSTEMS WITH PRODUCT FUNCTIONAL SAFETY REQUIREMENTS; (B) AERONAUTIC APPLICATIONS; (C) AUTOMOTIVE APPLICATIONS OR ENVIRONMENTS, AND/OR (D) AEROSPACE APPLICATIONS OR ENVIRONMENTS. WHERE ST PRODUCTS ARE NOT DESIGNED FOR SUCH USE, THE PURCHASER SHALL USE PRODUCTS AT PURCHASER’S SOLE RISK, EVEN IF ST HAS BEEN INFORMED IN WRITING OF SUCH USAGE, UNLESS A PRODUCT IS EXPRESSLY DESIGNATED BY ST AS BEING INTENDED FOR “AUTOMOTIVE, AUTOMOTIVE SAFETY OR MEDICAL” INDUSTRY DOMAINS ACCORDING TO ST PRODUCT DESIGN SPECIFICATIONS. PRODUCTS FORMALLY ESCC, QML OR JAN QUALIFIED ARE DEEMED SUITABLE FOR USE IN AEROSPACE BY THE CORRESPONDING GOVERNMENTAL AGENCY.

RESTRICTIONS OF USE AND CONFIDENTIALITY OBLIGATIONS:

THIS DOCUMENT AND ITS ANNEXES CONTAIN ST PROPRIETARY AND CONFIDENTIAL INFORMATION. THE DISCLOSURE, DISTRIBUTION, PUBLICATION OF WHATSOEVER NATURE OR USE FOR ANY OTHER PURPOSE THAN PROVIDED IN THIS DOCUMENT OF ANY INFORMATION CONTAINED IN THIS DOCUMENT AND ITS ANNEXES IS SUBMITTED TO ST PRIOR EXPRESS AUTHORIZATION. ANY UNAUTHORIZED REVIEW, USE, DISCLOSURE OR DISTRIBUTION OF SUCH INFORMATION IS EXPRESSLY PROHIBITED.

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners

© 2014 STMicroelectronics - All rights reserved.

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

www.st.com