CHANGE NOTIFICATION

Analog Devices, Inc.
1630 McCarthy Blvd., Milpitas CA
(408) 432-1900

March 06, 2018 PCN_030618

Dear Sir/Madam:

Subject: Notification of Change to LTC4360-1, LTC4360-2 Datasheet

Please be advised that Analog Devices, Inc. Milpitas, California has made a minor change to the LTC4360-1, LTC4360-2 product datasheet to facilitate improvement in our manufacturing capability. The changes are shown on the attached page of the marked up datasheet. There was no change in form, fit, function, quality or reliability of the product. The product shipped after May 06, 2018 will be tested to the new limits.

Should you have any questions or concerns please contact your local Analog Devices sales representatives or you may contact me at 408-432-1900 ext. 2077, or by e-mail at JASON.HU@ANALOG.COM. If I do not hear from you by May 06, 2018, we will consider this change to be approved by your company.

Sincerely,

Jason Hu
Quality Assurance Engineer

For questions on this PCN, please contact Jason Hu or you may send an email to your regional contacts below or contact your local ADI sales representatives.			
Americas: PCN_Americas@analog.com	**Europe:** PCN_Europe@analog.com	**Japan:**	PCN_Japan@analog.com
		Rest of Asia:	PCN_ROA@analog.com

new parameter

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. V_{IN} = 5V, $V_{\overline{ON}}$ = 0V (LTC4360-1) unless otherwise noted.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Supplies							
V_{IN}	Input Voltage Range		●	2.5		80	V
$V_{IN(UVL)}$	Input Undervoltage Lockout	V_{IN} Rising	●	1.8	2.1	2.45	V
I_{IN}	Input Supply Current	LTC4360-1 $V_{\overline{ON}}$ = 0V, LTC4360-2	●		220	400	µA
		LTC4360-1 $V_{\overline{ON}}$ = 2.5V	●		1.5	10	µA
Thresholds							
$V_{IN(OV)}$	IN Pin Overvoltage Threshold	V_{IN} Rising	●	5.684	5.8	5.916	V
$V_{IN(OVL)}$	IN Pin Overvoltage Recovery Threshold	V_{IN} Falling	●	5.51	5.7	5.85	V
ΔV_{OV}	Overvoltage Hysteresis		●	25	100	~~200~~ 300	mV
External Gate Drive							
ΔV_{GATE}	External N-Channel MOSFET Gate Drive ($V_{GATE} - V_{OUT}$)	2.5V ≤ V_{IN} < 3V, I_{GATE} = –1µA 3V ≤ V_{IN} < 5.5V, I_{GATE} = –1µA	● ●	3.5 4.5	4.5 6	6 7.9	V V
$V_{GATE(TH)}$	GATE High Threshold for $\overline{PWRGD}$ Status	V_{IN} = 3.3V V_{IN} = 5V	● ●	5.7 6.7	6.3 7.2	6.8 7.8	V V
$I_{GATE(UP)}$	GATE Pull-Up Current	V_{GATE} = 1V	●	–5	–10	–15	µA
$V_{GATE(UP)}$	GATE Ramp-Up	V_{GATE} = 1V to 7V	●	1.5	3	4.5	V/ms
$I_{GATE(FST)}$	GATE Fast Pull-Down Current	Fast Turn-Off, V_{IN} = 6V, V_{GATE} = 9V	●	15	30	60	mA
$I_{GATE(DN)}$	GATE Pull-Down Current	$V_{\overline{ON}}$ = 2.5V, V_{GATE} = 9V (LTC4360-1)	●	10	40	80	µA
Input Pins							
$I_{OUT(IN)}$	OUT Input Current	V_{OUT} = 5V, $V_{\overline{ON}}$ = 0V V_{OUT} = 5V, $V_{\overline{ON}}$ = 2.5V	● ●	5	10 0	20 ±3	µA µA
$V_{\overline{ON}(TH)}$	$\overline{ON}$ Input Threshold	(LTC4360-1)	●	0.4		1.5	V
$I_{\overline{ON}}$	$\overline{ON}$ Pull-Down Current	$V_{\overline{ON}}$ = 2.5V (LTC4360-1)	●	2.5	5	10	µA
Output Pins							
$V_{GATEP(CLP)}$	IN to GATEP Clamp Voltage	V_{IN} = 8V to 80V (LTC4360-2)	●	5	5.8	7.5	V
R_{GATEP}	GATEP Resistive Pull-down	V_{GATEP} = 3V (LTC4360-2)	●	0.8	2	3.2	MΩ
$V_{\overline{PWRGD}(OL)}$	$\overline{PWRGD}$ Output Low Voltage	V_{IN} = 5V, $I_{\overline{PWRGD}}$ = 3mA	●		0.23	0.4	V
$R_{\overline{PWRGD}}$	$\overline{PWRGD}$ Pull-Up Resistance to OUT	V_{IN} = 6.5V, $V_{\overline{PWRGD}}$ = 1V	●	250	500	800	kΩ
Delay							
t_{ON}	GATE On Delay	V_{IN} High to I_{GATE} = –5µA	●	50	130	200	ms
t_{OFF}	GATE Off Propagation Delay	V_{IN} = Step 5V to 6.5V to $\overline{PWRGD}$ High	●		0.25	1	µs
$t_{\overline{PWRGD}}$	$\overline{PWRGD}$ Delay	V_{IN} = Step 5V to 6.5V V_{GATE} > $V_{GATE(TH)}$ to $\overline{PWRGD}$ Low	● ●	 25	0.25 65	1 100	µs ms
$t_{\overline{ON}(OFF)}$	$\overline{ON}$ High to GATE Off	$V_{\overline{ON}}$ = Step 0V to 2.5V (LTC4360-1)	●		2	5	µs

Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: All currents into device pins are positive; all currents out of device pins are negative. All voltages are referenced to GND unless otherwise specified.

Note 3: An internal clamp limits V_{GATE} to a minimum of 4.5V above V_{OUT}. Driving this pin to voltages beyond this clamp may damage the device.