Product Change Notification / SYST-18WLHI601

Date:

20-Jan-2023

Product Category:

8-bit Microcontrollers

PCN Type:

Document Change

Notification Subject:

Data Sheet - AVR128DB28/32/48/64 Data Sheet

Affected CPNs:

SYST-18WLHI601_Affected_CPN_01202023.pdf
SYST-18WLHI601_Affected_CPN_01202023.csv

Notification Text:

SYST-18WLHI601

Microchip has released a new Datasheet for the AVR128DB28/32/48/64 Data Sheet of devices. If you are using one of these devices please read the document located at AVR128DB28/32/48/64 Data Sheet.

Notification Status: Final

Description of Change:

Document	• General improvement of the documentation and its structure • Updated terminology used throughout the data sheet: – Master is replaced by host – Slave is replaced by client Features
Features	• The Flash write/erase endurance is 1,000 cycles
Pinout	• Added “RESET” to PF6 pin
Hardware Guidelines	• Connection for Power Supply section: – Primary decoupling capacitor (C1) changed to 100 nF – Additional decoupling capacitor added (C3) for system with fast transients • Connection for RESET section: – Added section for UPDI enable using High-Voltage override • Connection for UPDI Programming section:

	– Added section for new UPDI connector (UPDI Connector v2)
Power Supply	• Update to block diagram (AVDD and VDD internal connections) • Update to table with pin descriptions
AVR® CPU	• Update to block diagram (broken arrow) • Added single cycle ALU operation to “Instruction Execution Timing” • Update to the Extended Memory Pointer section • More detailed description of CCP section • Update to RAMPZ register description
Memories	• Updated the memory map image • Update to SRAM table • Update to SIGROW section, Signature Row register Device ID n • Update to CRCSRC bit field and • Update to EESAVE bit of the System Configuration 0 fuse – EEPROM is saved during a chip erase regardless of whether the device is locked or not
Peripherals and Architecture	• Update to Interrupt Vector Mapping section, Interrupt Vector Mapping table • Update to SYSCFG section, Device Revision ID Register description – MAJOR bit field contains the major revision for the device. 0x01 = A, 0x02 = B, and so on.
NVMCTRL	• Update to Features section • Update to Interrupts section (table)
CLKCTRL	• Update to block diagram • Update to Main Clock Selection and Prescaler section, caution text • Auto-Tune section is replaced by new section Manual Tuning and Auto-Tune and all the text is replaced • Update to Clock Failure Detection section • Update to 32.768 kHz Crystal Oscillator Control A register and “Note” added to LowPower Mode bit • Update to External High-Frequency Oscillator Control A register
SLPCTRL	• Update to Voltage Regulator Configuration section (table)

	• Update to Sleep Modes section • Added Configuration Change Protection section • Update to Voltage Regulator Control Register – Update to HTLLEN bit description and “Warning” – Update to PMODE bit field description
RSTCTRL	• Updated sections: – Initialization – Block Diagram – Power-On Reset (POR) – Reset Sources
CPUINT	• Update to Functional Description section • Update to Control A register
EVSYS	• Update to Channel n Generator Selection register
PORT	• Update to Initialization section • Update to Multi-Pin Configuration section • Update to Virtual Ports section • Update to Multi-Pin Configuration register • Update to Pin n Control register
MVIO	• Update to Operation section: – Update to Power Sequencing section
BOD	• Update to Control B register
WDT	• Update to Operation section: – Update to Normal Mode section – Update to Window Mode section
TCA	• Update to Overview section, Timer/Counter Clock Logic figure in the Block Diagram sub-section • Update to Functional Description section: – Update to Frequency Waveform Generation section – Update to Split Mode - Two 8-Bit Timer/Counters section • Update to Control C register

	• Update to Event Control register • Update to Temporary Bits for 16-Bit Access register • Update to Counter Register - Normal Mode register • Update to Control C - Split Mode register
TCB	• Update to Functional Description section: – Update to Initialization section • Update to Single-Shot Mode sub-section and to the EDGE bit description in the TCB.EVCTRL register – When the EDGE bit of the TCB.EVCTRL register is written to “1” or “0” • Update to Output section • Update to 32-Bit Input Capture section
TCD	• Update to Function Description section, Programmable Output Events sub-section
RTC	• Update to RTC Functional Description section, Configure RTC sub-section • Update to PIT Functional Description section, Initialization sub-section
USART	• Update to Transmit Data Register Low Byte register • Update to Transmit Data Register High Byte register
TWI	• Update to the TWI Basic Operation section • Updated registers: – Control A – Dual Mode Control Configuration – Master Control A – Master Control B – Client Control B
CCL	• Updated sections: – Truth Table Logic – Truth Table Inputs Selection – Clock Source Settings • Updated registers: – LUTn Control A

	– TRUTHn
AC	• Update to INTMODE bit field description of the AC Interrupt Control (ACn.INTCTRL) Register
ADC	• Updated sections: – Starting a Conversion – Temperature Measurement
DAC	• Updated the DAC Block Diagram • Updated sections: – Features – DAC Output – Operation • Updated the DAC Block Diagram • Update to DATA register
OPAMP	• Updated sections: – Input Voltage Range – Offset Calibration – Application Usage
UPDI	• Added section Addressing the Program Memory Space • Updated sections: – UPDI UART – One-Wire Enable • Updated registers: – Status A – ASI Key Status – ASI Reset Request – ASI Control A – ASI System Status – ASI CRC Status
Electrical Characteristics	• Entire section updated based on validation data

	• Updated the Memory Programming Specifications – The Flash memory cell endurance changed to 1k – Table notes added • Updates to the TWI Section
Characteristics Graphs	• Section added
Ordering Information	• Added note regarding automotive parts
Package Drawings	• Added wettable flank packages • Correction to 64-pin VQFN package drawing • Added Package Marking Information section

Impacts to Data Sheet: None

Reason for Change: To Improve Productivity

Change Implementation Status: Complete

Date Document Changes Effective: 20 Jan 2023

NOTE: Please be advised that this is a change to the document only the product has not been changed.

Markings to Distinguish Revised from Unrevised Devices: N/A

Attachments:

AVR128DB28/32/48/64 Data Sheet

Please contact your local Microchip sales office with questions or concerns regarding this notification.

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Affected Catalog Part Numbers (CPN)

AVR128DB28-E/SP
AVR128DB28-E/SS
AVR128DB28-E/SO
AVR128DB28-I/SP
AVR128DB28-I/SS
AVR128DB28-I/SO
AVR128DB28T-I/SS
AVR128DB28T-I/SO
AVR128DB28T-E/SS
AVR128DB28T-E/SO
AVR128DB32-E/RXB
AVR128DB32-E/PT
AVR128DB32-I/RXB
AVR128DB32-I/PT
AVR128DB32T-I/RXB
AVR128DB32T-I/PT
AVR128DB32T-E/RXB
AVR128DB32T-E/PT
AVR128DB48-E/6LX
AVR128DB48-E/PT
AVR128DB48-I/6LX
AVR128DB48-I/PT
AVR128DB48T-I/6LX
AVR128DB48T-I/PT
AVR128DB48T-E/6LX
AVR128DB48T-E/PT
AVR128DB64-E/MR
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AVR128DB64-I/MR
AVR128DB64-I/PT
AVR128DB64T-I/MR
AVR128DB64T-I/PT
AVR128DB64T-E/MR
AVR128DB64T-E/PT