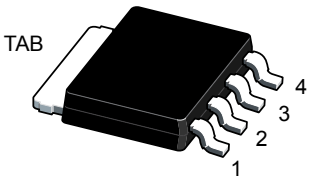
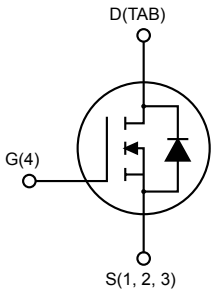
STK130N4LF7AG

Datasheet

Automotive N-channel 40 V, 2.4 mΩ typ., 100 A, STripFET F7 Power MOSFET in an LFPAK 5x6 package



LFPAK 5x6



G4S123DTAB_LFPAK

Features

Order code	V_{DS}	$R_{DS(on)}$ max.	I_D
STK130N4LF7AG	40 V	3.0 mΩ	100 A

- AEC-Q101 qualified
- Among the lowest $R_{DS(on)}$ on the market
- Excellent FoM (figure of merit)
- Low C_{rss}/C_{iss} ratio for EMI immunity
- High avalanche ruggedness

Applications

- Switching applications

Description

This N-channel Power MOSFET utilizes STripFET F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Product status link
STK130N4LF7AG

Product summary	
Order code	STK130N4LF7AG
Marking	130N4LF7
Package	LFPAK 5x6
Packing	Tape and reel

1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	40	V
V_{GS}	Gate-source voltage	±20	V
I_D	Drain current (continuous) at T_C = 25 °C (1)	100	A
	Drain current (continuous) at T_C = 100 °C	93	A
I_{DM}(2)	Drain current (pulsed)	400	A
P_{TOT}	Total power dissipation at T_C = 25 °C	105	W
I_{AV}	Avalanche current, repetitive or not repetitive (pulse width limited by maximum junction temperature)	32	A
E_{AS}	Single pulse avalanche energy (starting T_J = 25 °C, I_D = I_{AV}, V_{DD} = 25 V)	250	mJ
T_j	Operating junction temperature range	-55 to 175	°C
T_{stg}	Storage temperature range		

1. *Drain current is limited by package, the current capability of the silicon is 130 A at 25 °C.*
2. *Pulse width limited by safe operating area.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJB}(1)	Thermal resistance, junction-to-board	31.3	°C/W
R_{thJC}	Thermal resistance, junction-to-case	1.43	°C/W

1. *When mounted on FR-4 board of 1 inch², 2oz Cu, t < 10 s.*

2 Electrical characteristics

(T_C = 25 °C unless otherwise specified)

Table 3. On/off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V, I_D = 1 mA	40			V
I_{DSS}	Zero gate voltage drain current	V_{GS} = 0 V, V_{DS} = 40 V			1	µA
I_{GSS}	Gate-body leakage current	V_{GS} = 20 V, V_{DS} = 0 V			100	nA
$V_{GS(th)}$	Gate threshold voltage	V_{DS} = V_{GS}, I_D = 250 µA	1.5		2.5	V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 10 V, I_D = 50 A		2.4	3.0	mΩ
		V_{GS} = 4.5 V, I_D = 50 A		4	6.0	mΩ

Table 4. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	V_{DS} = 25 V, f = 1 MHz, V_{GS}= 0 V	-	1850	-	pF
C_{oss}	Output capacitance		-	520	-	pF
C_{rss}	Reverse transfer capacitance		-	33	-	pF
Q_g	Total gate charge	V_{DD} = 20 V, I_D = 100 A, V_{GS} = 0 to 10 V (see Figure 13. Test circuit for gate charge behavior)	-	26	-	nC
Q_{gs}	Gate-source charge		-	7.5	-	nC
Q_{gd}	Gate-drain charge		-	4.5	-	nC

Table 5. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	V_{DD} = 20 V, I_D = 50 A, R_G = 4.7 Ω, V_{GS} = 10 V (see Figure 12. Test circuit for resistive load switching times and Figure 17. Switching time waveform)	-	9.5	-	ns
t_r	Rise time		-	3.2	-	ns
$t_{d(off)}$	Turn-off delay time		-	30	-	ns
t_f	Fall time		-	12	-	ns

Table 6. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD} (1)	Forward on voltage	I_{SD} = 100 A, V_{GS} = 0 V	-		1.2	V
t_{rr}	Reverse recovery time	I_D = 100 A, di/dt = 100 A/µs V_{DD} = 32 V (see Figure 14. Test circuit for inductive load switching and diode recovery times)	-	14		ns
Q_{rr}	Reverse recovery charge		-	15		nC
I_{RRM}	Reverse recovery current		-	1		A

1. *Pulsed: pulse duration = 300 µs, duty cycle 1.5%*

2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

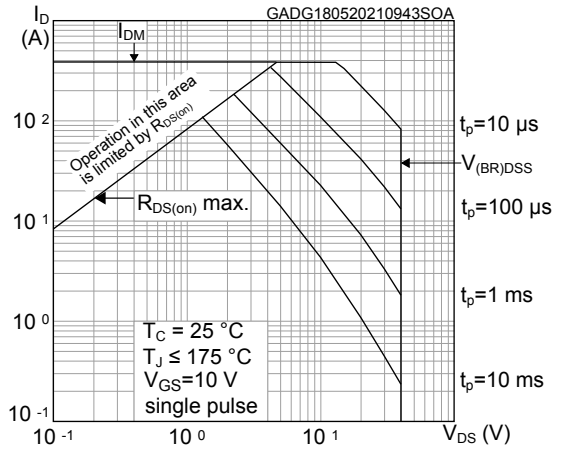


Figure 2. Normalized transient thermal impedance

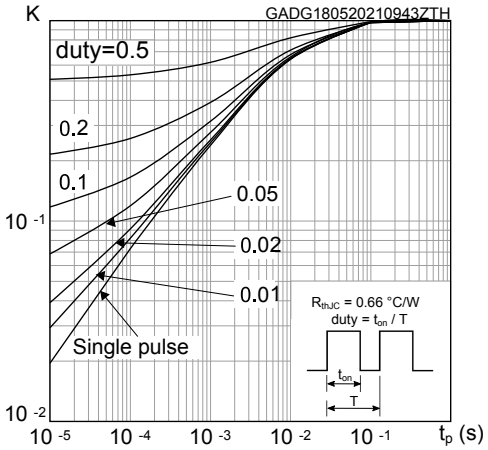


Figure 3. Typical output characteristics

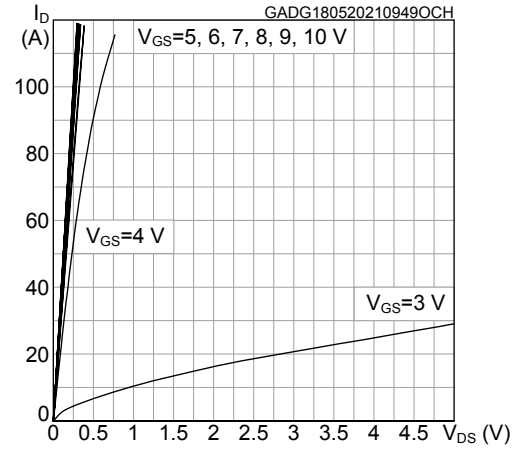


Figure 4. Typical transfer characteristics

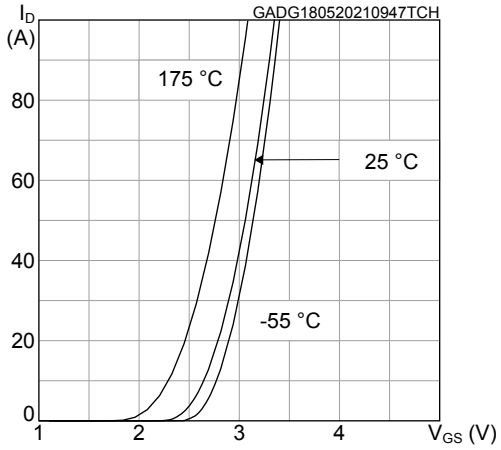


Figure 5. Typical gate charge characteristics

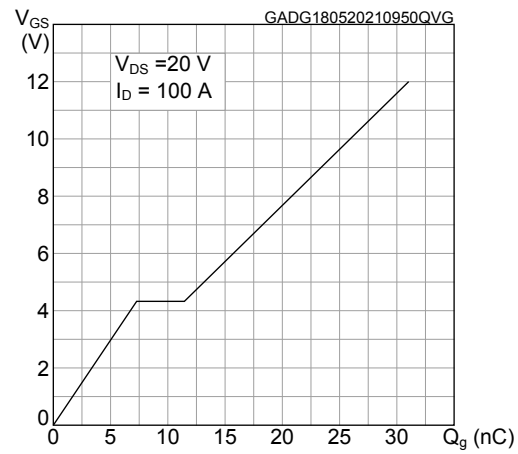


Figure 6. Typical drain-source on-resistance

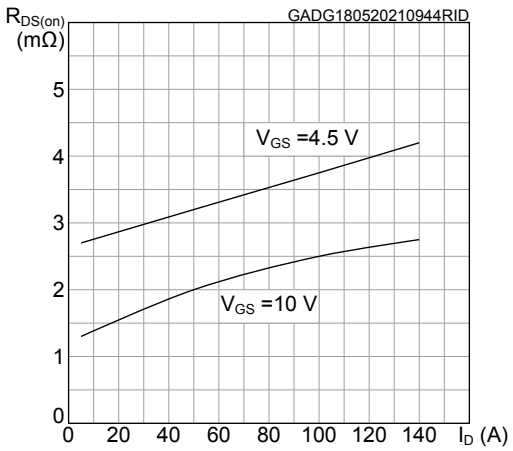


Figure 7. Typical capacitance characteristics

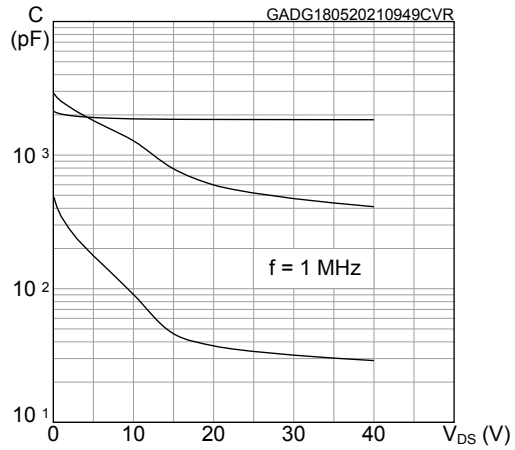


Figure 8. Normalized gate threshold vs temperature

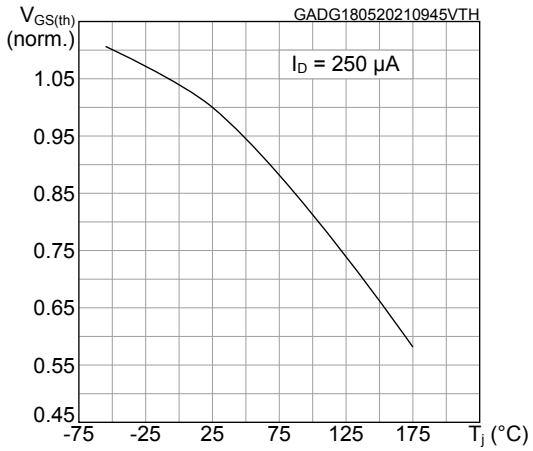


Figure 9. Normalized on-resistance vs temperature

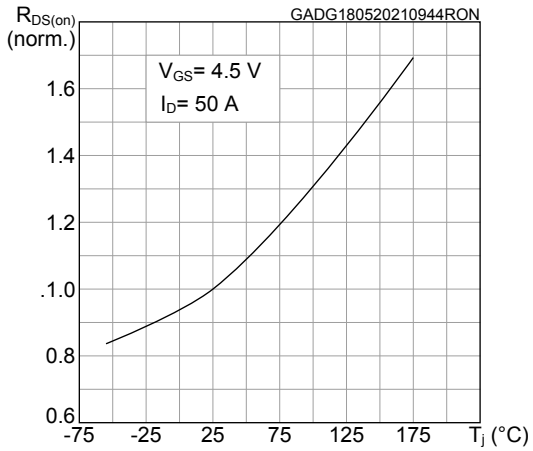


Figure 10. Normalized breakdown voltage vs temperature

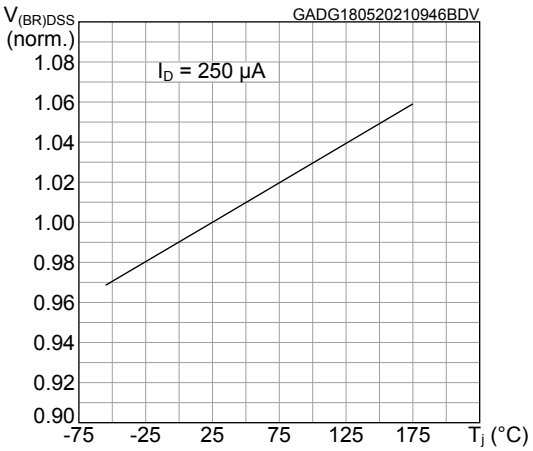
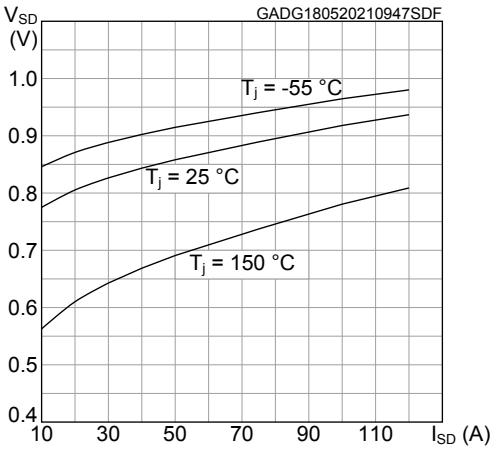


Figure 11. Typical reverse diode forward characteristics



3 Test circuits

Figure 12. Test circuit for resistive load switching times

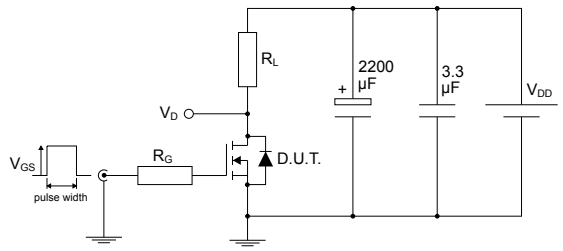


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Figure 13. Test circuit for gate charge behavior

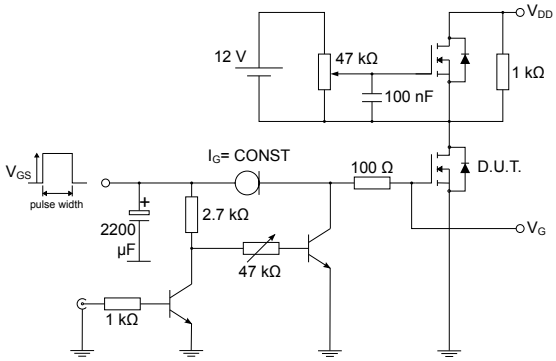

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Figure 14. Test circuit for inductive load switching and diode recovery times

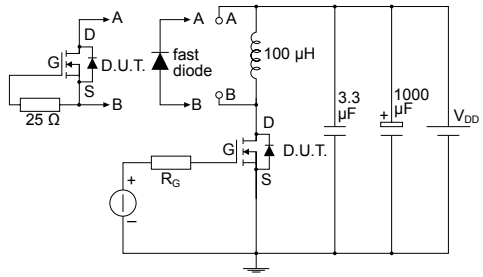

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Figure 15. Unclamped inductive load test circuit

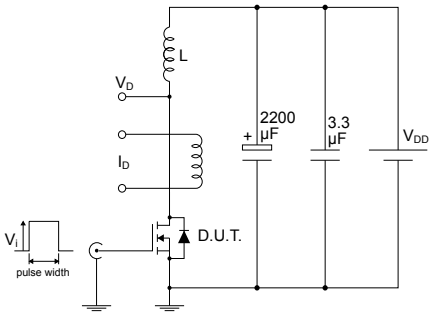

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Figure 16. Unclamped inductive waveform

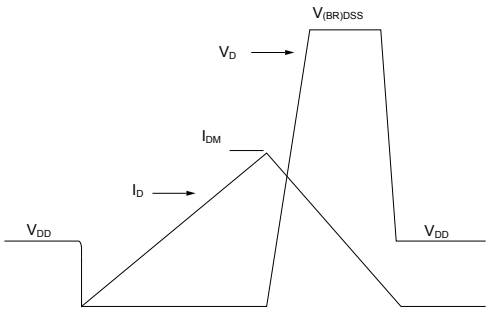

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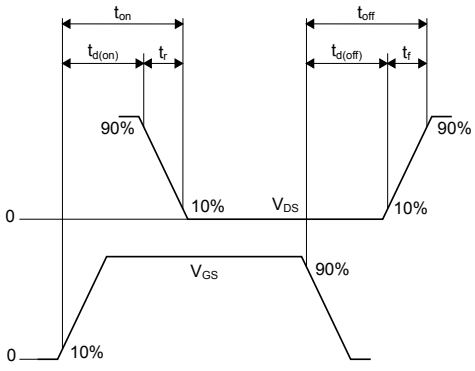
Figure 17. Switching time waveform



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4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 LFPAK 5x6 package information

Figure 18. LFPAK 5x6 package outline

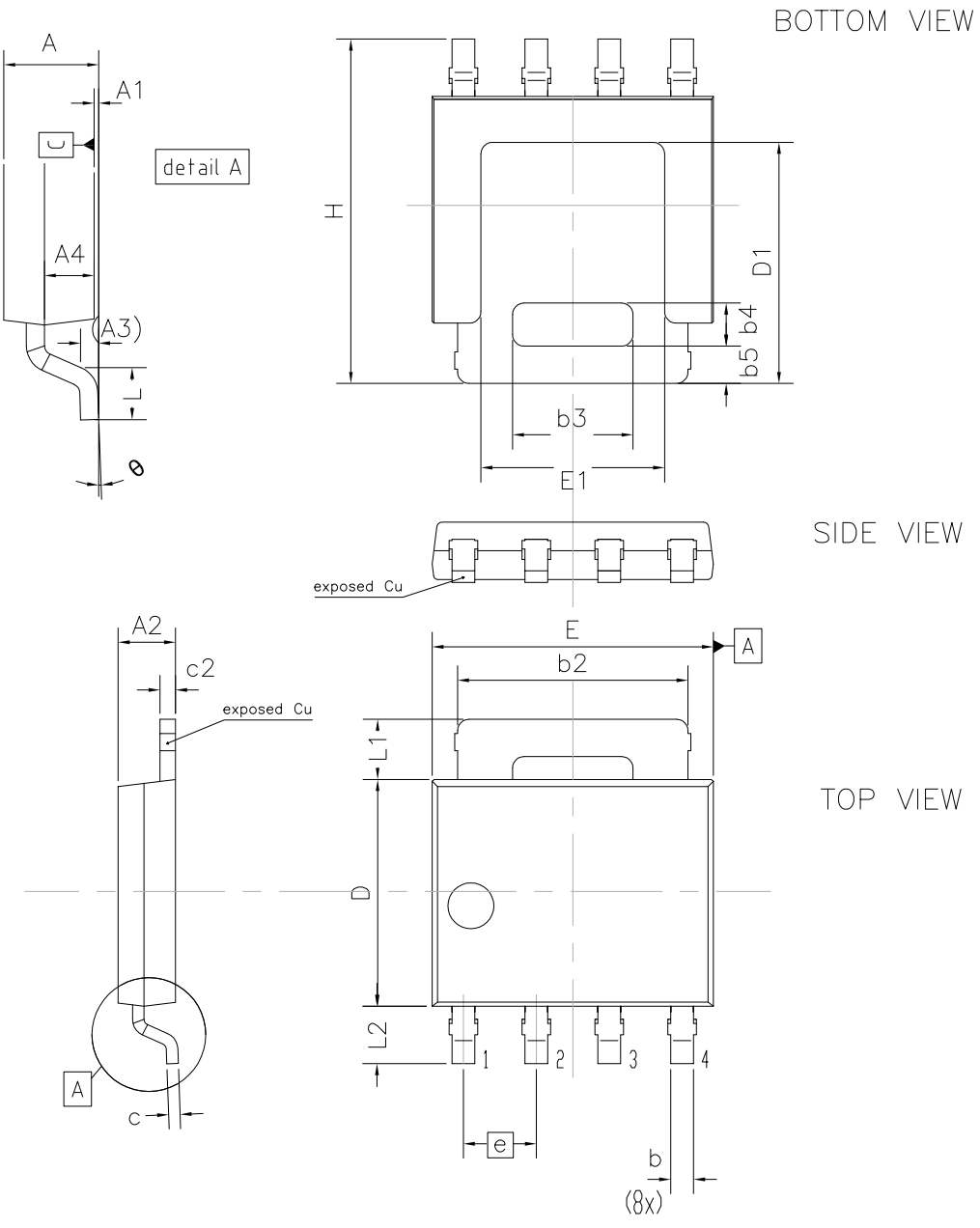

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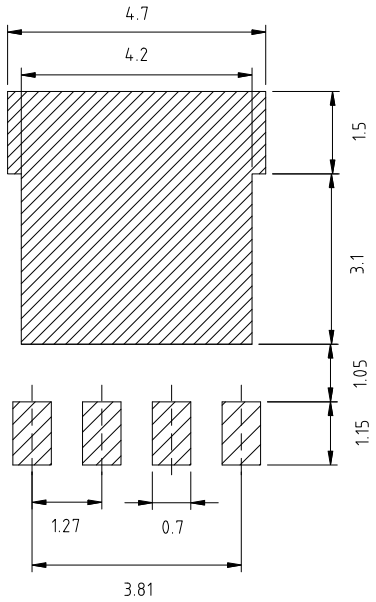
Table 7. LFPAK 5x6 package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	1.01		1.20
A1	0.00		0.15
A2	0.95		1.10
A3		0.25	
A4	0.50	0.55	0.65
b	0.35		0.50
b2	3.62		4.41
b3	2.00		2.20
b4	0.70		0.90
b5			0.70
c	0.19	0.20(1)	0.25
c2	0.24		0.30
D	3.80		4.10
D1	3.80	4.00	4.20
E	4.80		5.00
E1	3.10		3.30
e		1.27	
H	5.80		6.20
L	0.40		0.85
L1	0.80		1.30
L2	0.80		1.30
w		0.25	
y		0.10	
Θ	0°		8°

1. *Dimension without plating*

Figure 19. **LFPAK 5x6 recommended footprint (dimensions in mm)**



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Revision history

Table 8. **Document revision history**

Date	Revision	Changes
18-Mar-2019	1	First release.
27-Jul-2020	2	Updated title and features in cover page.
24-May-2021	3	Modified *Table 1. Absolute maximum ratings*, *Table 3. On/off states*, *Table 4. Dynamic*, *Table 5. Switching times*, and *Table 6. Source-drain diode*. Added *Electrical characteristics (curves)*. Minor text changes.
28-Sep-2021	4	Updated Figure 1. Safe operating area.

Contents