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NTE74HCT08
Integrated Circuit
TTL – High Speed CMOS,
Quad, 2–Input AND Gate

Description:

The NTE74HCT08 is a logic function in a 14–Lead plastic DIP type package fabricated using advanced silicon–gate CMOS technology which provides the inherent benefits of CMOS – low quiescent power and wide power supply range. This device is input and output characteristic and pinout compatible with standard NTE74LS logic families. All inputs are protected from static discharge damage by internal diodes to V_{CC} and ground.

The NTE74HCT08 is intended to interface between TTL and NMOS components and standard CMOS devices. This device is also a plug–in replacement for LS–TTL devices and can be used to reduce power consumption in existing designs.

Features:

- TTL, LS Pinout and Threshold Compatible
- Fast Switching: t_{PLH}, t_{PLH} = 12ns (typ)
- Low Power: 10μW at DC,
- High Fanout: ≥ 10 LS Loads

Absolute Maximum Ratings: (Note 1, Note 2)

Supply Voltage, V_{CC} . . . . . –0.5 to +7.0V
DC Input Voltage, V_{IN} . . . . . –1.5 to V_{CC} +1.5V
DC Output Voltage, V_{OUT} . . . . . –0.5 to V_{CC} + 0.5V
Clamp Diode Current, I_{IK}, I_{OK} . . . . . ±20mA
DC Output Current (Per Pin), I_{OUT} . . . . . ±25mA
DC V_{CC} or GND Current (Per Pin), I_{CC} . . . . . ±50mA
Power Dissipation (Note 3), P_D 600mW
Storage Temperature Range, T_{stg} . . . . . –65°C to +150°C
Lead Temperature (During Soldering, 10sec), T_L . . . . . +260°C

Note 1. Stresses exceeding the Absolute Maximum Ratings may damage the device. The device may not function or be operable above the Recommended Operating Conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the Recommended Operating Conditions may effect device reliability. The Absolute Maximum Ratings are stress ratings only.

Note 2. Unless otherwise specified, all voltages are referenced to GND.

Note 3. Power Dissipation temperature derating: 12mW/°C from +65°C to +85°C.

Recommended Operating Conditions:

Parameter	Symbol	Min	Typ	Max	Unit
Supply Voltage	V_{CC}	4.5	–	5.5	V
DC Input or Output Voltage	V_{IN}, V_{OUT}	0	–	V_{CC}	V
Operating Temperature Range	T_A	–40	–	+85	°C
Input Rise or Fall Times	t_r, t_f	–	–	500	ns

DC Electrical Characteristics: (V_{CC} = 5V ±10% unless otherwise specified)

Parameter	Symbol	Test Conditions		T_A = +25°C	T_A = –40° to +85°C		Unit
				Typ	Guaranteed Limits		
Minimum High Level Input Voltage	V_{IH}			–	2.0	2.0	V
Maximum Low Level Input Voltage	V_{IL}			–	0.8	0.8	V
Minimum High Level Output Voltage	V_{OH}	V_{IN} = V_{IH} or V_{IL}	$\|I_{OUT}\|$ = 20μA	V_{CC}	V_{CC} –0.1	V_{CC} –0.1	V
			$\|I_{OUT}\|$ = 4.0mA, V_{CC} = 4.5V	4.2	3.98	3.84	V
			$\|I_{OUT}\|$ = 4.8mA, V_{CC} = 5.5V	5.2	4.98	4.84	V
Minimum Low Level Output Voltage	V_{OL}	V_{IN} = V_{IH}	$\|I_{OUT}\|$ = 20μA	0	0.1	0.1	V
			$\|I_{OUT}\|$ = 4.0mA, V_{CC} = 4.5V	0.2	0.26	0.33	V
			$\|I_{OUT}\|$ = 4.8mA, V_{CC} = 5.5V	0.2	0.26	0.33	V
Maximum Input Current	I_{IN}	V_{IN} = V_{CC} or GND, V_{IH} or V_{IL}		–	±0.1	±1.0	μA
Maximum Quiescent Supply Current	I_{CC}	V_{IN} = V_{CC} or GND, I_{OUT} = 0μA		–	2.0	20	μA
		V_{IN} = 2.4V or 0.5V, Note 4		–	1.2	1.4	mA

Note 4. This is measured per input with all other inputs held at V_{CC} or GND.

AC Electrical Characteristics: (V_{CC} = 5V, t_r = t_f = 6ns, C_L = 15pF, T_A = +25°C unless otherwise specified)

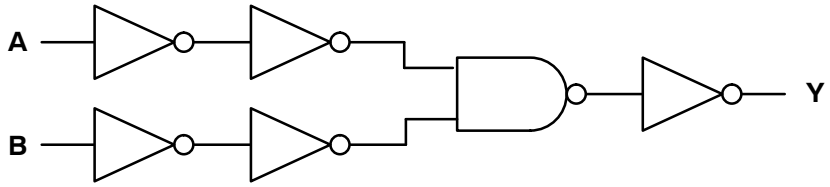
Parameter	Symbol	Test Conditions	Typ	Guaranteed Limits	Unit
Maximum Propagation Delay	t_{PLH}, t_{PHL}		9	15	ns

AC Electrical Characteristics: (V_{CC} = 5V ±10%, t_r = t_f = 6ns, C_L = 50pF unless otherwise specified)

Parameter	Symbol	Test Conditions	T_A = +25°C	T_A = –40° to +85°C		Unit
			Typ	Guaranteed Limits		
Maximum Propagation Delay	t_{PLH}, t_{PHL}		11	18	23	ns
Maximum Output Rise and Fall Time	t_{THL}, t_{TLH}		7	15	19	ns
Power Dissipation Capacitance	C_{PD}	Note 5	38	–	–	pF
Input Capacitance	C_{IN}		5	10	10	pF

Note 5. C_{PD} determines the no load dynamic power consumption, $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$, and the no load dynamic current consumption, $I_S = C_{PD} V_{CC} f + I_{CC}$.

Logic Diagram



Pin Connection Diagram