

#### Maxim > Design Support > Technical Documents > Application Notes > Power-Supply Circuits > APP 5504

Keywords: flyback, continuous conduction mode, CCM, discontinuous conduction mode, DCM, transformer, optoisolated feedback, error amplifier compensation, pi controller, biasing optocoupler, flyback converter, peak current mode controller, MAX17596, MAX17595

# APPLICATION NOTE 5504 Designing Flyback Converters Using Peak-Current-Mode Controllers

By: Srinivasa Rao Meesala Nov 27, 2012

Abstract: Flyback converter design using MAX17595/MAX17596 is outlined. Design methodology and calculations for components value selection are presented. Continuous conduction mode (CCM) and discontinuous conduction mode (DCM) are treated individually.

# Introduction

This application note describes the methodology of designing flyback converters using the MAX17595/MAX17596 peak-current-mode controllers. Flyback converters may be operated in discontinuous conduction mode (DCM) or continuous conduction mode (CCM). The component choices, stress level in power devices, and controller design vary depending on the operating mode of the converter. Formulas for calculating component values and ratings are also presented.

# **DCM Flyback**

## **Primary Inductance Selection**

In a DCM flyback converter, the energy stored in the primary inductance of the flyback transformer is delivered entirely to the output. The maximum primary-inductance value for which the converter remains in DCM at all operating conditions can be calculated as:

$$L_{\text{PRIMAX}} \leq \frac{(V_{\text{INMIN}} \times D_{\text{MAX}})^2 \times 0.4}{(V_{\text{OUT}} + V_{\text{D}}) \times I_{\text{OUT}} \times F_{\text{SW}}}$$

(Eq. 1)

Where D<sub>MAX</sub> is chosen as 0.43 for the MAX17595/MAX17596, V<sub>D</sub> is the voltage drop of the output rectifier diode on the secondary winding, and  $F_{SW}$  is the switching frequency of the power converter. Choose the primary inductance value to be less than L<sub>PRIMAX</sub>.

## **Duty Cycle Calculation**

The accurate value of the duty cycle (DNEW) for the selected primary inductance (LPRI) can be

calculated using the following equation:

$$D_{NEW} = \frac{\sqrt{2.5 \times L_{PRI} \times (V_{OUT} + V_D) \times I_{OUT} \times F_{SW}}}{V_{INMIN}}$$
(Eq. 2)

# Turns Ratio Calculation (N<sub>S</sub>/N<sub>P</sub>)

Transformer turns ratio ( $K = N_S/N_P$ ) can be calculated as:

$$K = \frac{(V_{OUT} + V_D) \times (1 - D_{NEW})}{V_{INMIN} \times D_{NEW}}$$
(Eq. 3)

#### Peak/RMS Current Calculation

Primary and secondary RMS currents and primary peak current calculations are needed to design the transformer in switched-mode power supplies. Also, primary peak current is used in setting the current limit. Use the following equations to calculate the primary and secondary peak and RMS currents.

Maximum primary peak current, 
$$I_{PRIPEAK} = \frac{V_{INMIN} \times D_{NEW}}{L_{PRI} \times F_{SW}}$$
 (Eq. 4)  
Maximum primary RMS current,  $I_{PRIRMS} = I_{PRIPEAK} \times \sqrt{\frac{D_{NEW}}{3}}$  (Eq. 5)

Maximum secondary peak current, 
$$I_{SECPEAK} = \frac{I_{PRIPEAK}}{K}$$
 (Eq. 6)

Maximum secondary RMS current, 
$$I_{SECRMS} = \sqrt{\frac{2 \times I_{OUT} \times I_{PRIPEAK}}{3 \times K}}$$
 (Eq. 7)

For the purpose of current limit setting, the peak current may be calculated as follows:

$$I_{\text{LIM}} = I_{\text{PRIPEAK}} \times 1.2 \tag{Eq. 8}$$

## **Primary Snubber Selection**

Ideally, the external MOSFET experiences a drain-source voltage stress equal to the sum of the input voltage and reflected voltage across the primary winding during the OFF period of the MOSFET. In practice, parasitic inductors and capacitors in the circuit, such as leakage inductance of the flyback transformer, cause voltage overshoot and ringing in addition to the ideally expected voltage stress. Snubber circuits are used to limit the voltage overshoots to safe levels within the voltage rating of the external MOSFET. The snubber capacitor can be calculated using the following equation:

$$C_{SNUB} = \frac{2 \times L_{LK} \times I_{PRIPEAK}^{2} \times K^{2}}{V_{OUT}^{2}}$$
(Eq. 9)

Where  $L_{LK}$  is the leakage inductance that can be obtained from the transformer specifications (usually 1% to 2% of the primary inductance).

The power that must be dissipated in the snubber resistor is calculated using the following formula:

$$P_{SNUB} = 0.833 \times L_{LK} \times I_{PRIPEAK^2} \times F_{SW}$$
(Eq. 10)

The snubber resistor is calculated based on the equation below:

$$R_{SNUB} = \frac{6.25 \times V_{OUT}^2}{P_{SNUB} \times K^2}$$
(Eq. 11)

The voltage rating of the snubber diode is:

$$V_{\text{DSNUB}} = V_{\text{INMAX}} + (2.5 \times V_{\text{OUT}}/\text{K})$$
(Eq. 12)

#### Output Capacitor Selection

X7R ceramic output capacitors are preferred in industrial applications due to their stability over temperature. The output capacitor is usually sized to support a step load of 50% of the rated output current in nonisolated applications so that the output voltage deviation is contained to 3% of the rated output voltage. The output capacitance can be calculated as follows:

$$C_{OUT} = \frac{I_{STEP} \times T_{RESPONSE}}{\Delta V_{OUT}}$$
(Eq. 13)

$$T_{\text{RESPONSE}} \cong \left(\frac{0.33}{F_{\text{C}}} + \frac{1}{F_{\text{SW}}}\right) \tag{Eq. 14}$$

The output capacitor RMS current rating can be calculated as follows:

$$I_{\text{COUTRMS}} = I_{\text{OUT}} \times \sqrt{\frac{2 \times I_{\text{PRIPEAK}}}{3 \times K \times I_{\text{OUT}}}} - 1$$
(Eq. 15)

Where I<sub>STEP</sub> is the load step, T<sub>RESPONSE</sub> is the response time of the controller,  $\Delta V_{OUT}$  is the allowable output voltage deviation, and F<sub>C</sub> is the target closed-loop crossover frequency. F<sub>C</sub> is chosen to be 1/10 of the switching frequency F<sub>SW</sub>. For the flyback converter, the output capacitor supplies the load current when the main switch is on, and therefore the output voltage ripple is a function of load current and duty cycle. Use the following equation to calculate the output capacitor ripple:

$$\Delta V_{\text{COUT}} = \frac{I_{\text{OUT}} \times [I_{\text{PRIPEAK}} - (K \times I_{\text{OUT}})]^2}{I_{\text{PRIPEAK}}^2 \times F_{\text{SW}} \times C_{\text{OUT}}}$$
(Eq. 16)

Where I<sub>OUT</sub> is load current and DNEW is the duty cycle at minimum input voltage.

## Input Capacitor Selection

The MAX17595 is optimized to implement offline AC-DC converters. In such applications, the input capacitor must be selected based on either the ripple due to the rectified line voltage, or based on holdup-time requirements. Holdup time can be defined as the time period over which the power supply should regulate its output voltage from the instant the AC power fails. The MAX17596 is useful in implementing low-voltage DC-DC applications where the switching-frequency ripple must be used to calculate the input capacitor. In both cases, the capacitor must be sized to meet RMS current requirements for reliable operation.

# Capacitor Selection Based on Switching Ripple (MAX17596)

For DC-DC applications, X7R ceramic capacitors are recommended due to their stability over the operating temperature range. The effective series resistance (ESR) and effective series inductance (ESL) of a ceramic capacitor are relatively low, so the ripple voltage is dominated by the capacitive component. For the flyback converter, the input capacitor supplies the current when the main switch is on. Use the following equation to calculate the input capacitor for a specified peak-to-peak input switching ripple (V<sub>IN\_RIP</sub>):

$$C_{IN} = \frac{D_{NEW} \times I_{PRIPEAK} [1 - (0.5 \times D_{NEW})]^2}{2 \times F_{SW} \times V_{IN} RIP}$$
(Eq. 17)

The input capacitor RMS current in low-voltage DC-DC applications can be calculated as follows:

$$I_{\text{INCRMS}} = \frac{1}{2} \times I_{\text{PRIPEAK}} \times D_{\text{NEW}} \times \sqrt{\frac{4}{3 \times D_{\text{NEW}}} - 1}$$
(Eq. 18)

# Capacitor Selection Based on Rectified Line Voltage Ripple (MAX17595)

For the flyback converter, the input capacitor supplies the input current when the diode rectifier is off. The voltage discharge on the input capacitor, due to the input average current, should be within the limits specified.

Assuming 25% ripple present on input DC capacitor, the input capacitor can be calculated as follows:

$$C_{IN} = \frac{0.045 \times P_{LOAD}}{\eta \times V_{IN,PK}^{2}}$$

(Eq. 19)

Where  $P_{LOAD}$  = rated output power  $\eta$  = typical efficiency at V<sub>AC,MIN</sub> and I<sub>LOAD</sub>  $V_{IN,PK} = \sqrt{2} \times V_{AC,MIN}$  = peak voltage at minimum input AC voltage.

# Capacitor Selection Based on Holdup Time Requirements (MAX17595)

For a given output power ( $P_{HOLDUP}$ ) that needs to be delivered during holdup time ( $T_{HOLDUP}$ ), the DC bus voltage at which the AC supply fails ( $V_{INFAIL}$ ), and the minimum DC bus voltage at which the converter can regulate the output voltages ( $V_{INMIN}$ ), the input capacitor ( $C_{IN}$ ) is estimated as:

$$C_{IN} = \frac{3 \times P_{HOLDUP} \times T_{HOLDUP}}{(V_{INFAIL}^2 - V_{INMIN}^2)}$$
(Eq. 20)

The input capacitor RMS current for AC-DC applications can be calculated as:

$$I_{\text{INCRMS}} = \frac{2.7 \times P_{\text{LOAD}}}{\eta \times V_{\text{IN,PK}}}$$
(Eq. 21)

## External MOSFET Selection

MOSFET selection criteria include maximum drain voltage, peak/RMS current in the primary, and the maximum allowable power dissipation of the package without exceeding the junction temperature limits. The voltage seen by the MOSFET drain is the sum of the input voltage, the reflected secondary voltage on the transformer primary, and the leakage inductance spike. The MOSFET's absolute maximum VDS rating must be higher than the worst-case drain voltage:

$$V_{\text{DSMAX}} = V_{\text{INMAX}} + \left[ \left( \frac{V_{\text{OUT}} + V_{\text{DIODE}}}{K} \right) \times 2.5 \right]$$
(Eq. 22)

The drain current rating of the external MOSFET is selected to be greater than the worst-case peak current limit setting.

## Secondary Diode Selection

Secondary-diode-selection criteria includes the maximum reverse voltage, average current in the secondary, reverse recovery time, junction capacitance, and the maximum allowable power dissipation of the package. The voltage stress on the diode is the sum of the output voltage and the reflected primary voltage. The maximum operating reverse-voltage rating must be higher than the worst-case reverse voltage:

$$V_{\text{SECDIODE}} = 1.25 \times (\text{K} \times \text{V}_{\text{INMAX}} + \text{V}_{\text{OUT}})$$
(Eq. 23)

The current rating of the secondary diode should be selected so that the power loss in the diode (given as the product of forward-voltage drop and the average diode current) should be low enough to ensure that the junction temperature is within limits. Select fast-recovery diodes with a recovery time less than 50ns, or Schottky diodes with low junction capacitance.

## Error Amplifier Compensation Design

For nonisolated designs, output voltage feedback and the loop compensation network are connected as shown in **Figure 1**.



Figure 1. Loop compensation arrangement for nonisolated designs.

The loop compensation values are calculated as:

$$R_{Z} = 1833 \times R_{CS} \times \sqrt{\frac{\left[1 + \left[\frac{0.1 \times F_{SW}}{F_{P}}\right]^{2}\right] \times V_{OUT} \times I_{OUT}}{2 \times L_{PRI} \times F_{SW}}}$$
(Eq. 24)

Where:

$$F_{P} = \frac{I_{OUT}}{\pi \times V_{OUT} \times C_{OUT}}$$

$$C_{Z} = \frac{1}{2 \times \pi \times R_{Z} \times F_{P}}$$

$$C_{P} = \frac{1}{\pi \times R_{Z} \times F_{SW}}$$
(Eq. 25)

 $F_{SW}$  is the switching frequency.

# CCM Flyback

# Transformer Turns Ratio Calculation ( $K = N_S/N_P$ )

The transformer turns ratio can be calculated using the following formula:

$$K = \frac{(V_{OUT} + V_D) \times (1 - D_{MAX})}{V_{INMIN} \times D_{MAX}}$$
(Eq. 26)

Where  $D_{MAX}$  is the duty cycle assumed at minimum input (0.43 for the MAX17595/MAX17596).

#### **Primary Inductance Calculation**

Calculate the primary inductance based on the ripple:

$$L_{PRI} = \frac{(V_{OUT} + V_D) \times (1 - D_{NOM})^2}{2 \times I_{OUT} \times \beta \times F_{SW} \times K^2}$$
(Eq. 27)

Where D<sub>NOM</sub>, the nominal duty cycle at nominal operating DC input voltage V<sub>INNOM</sub>, is given as:

$$D_{\text{NOM}} = \frac{(V_{\text{OUT}} + V_{\text{D}})}{[V_{\text{INNOM}} \times K + (V_{\text{OUT}} + V_{\text{D}})]}$$
(Eq. 28)

The output current, down to which the flyback converter should operate in CCM, is determined by selection of  $\beta$  in Equation 27. For example,  $\beta$  should be selected as 0.15 so that the converter operates in CCM down to 15% of the maxim output load current. The ripple in the primary current waveform is a function of the duty cycle; maximum ripple occurs at the maximum DC input voltage. Therefore, the maximum (worst-case) load current down to which the converter operates in CCM occurs at the maximum operating DC input voltage. V<sub>D</sub> is the forward drop of the selected output diode at maximum output current.

#### Peak and RMS Current Calculation

Primary and secondary RMS currents and primary peak current calculations are needed to design the transformer in switched-mode power supplies. Also, primary peak current is used in setting the current limit. Use the following equations to calculate the primary and secondary peak and RMS currents.

Maximum primary peak current:

$$I_{\text{PRIPEAK}} = \left(\frac{I_{\text{OUT}} \times K}{1 - D_{\text{MAX}}}\right) + \left(\frac{V_{\text{INMIN}} \times D_{\text{MAX}}}{2 \times L_{\text{PRI}} \times F_{\text{SW}}}\right)$$
(Eq. 29)

Maximum primary RMS current:

$$I_{\text{PRIRMS}} = \sqrt{D_{\text{MAX}}} \times \sqrt{I_{\text{PRIPEAK}}^2 + \frac{\Delta I_{\text{PRI}}^2}{3} - (I_{\text{PRIPEAK}} \times \Delta I_{\text{PRI}})}$$
(Eq. 30)

Where  $\Delta I_{PRI}$  is the ripple current in the primary current waveform, and is given by:

$$\Delta I_{PRI} = \left(\frac{V_{INMIN} \times D_{MAX}}{L_{PRI} \times F_{SW}}\right)$$
(Eq. 31)

Maximum secondary peak current:

$$I_{SECPEAK} = I_{PRIPEAK}/K$$
 (Eq. 32)

Maximum secondary RMS current:

$$I_{\text{SECRMS}} = \sqrt{1 - D_{\text{MAX}}} \times \sqrt{I_{\text{SECPEAK}}^2 + \frac{\Delta I_{\text{SEC}}^2}{3} - (I_{\text{SECPEAK}} \times \Delta I_{\text{SEC}})}$$
(Eq. 33)

Where  $\Delta I_{SEC}$  is the ripple current in the secondary current waveform, and is given by:

$$\Delta I_{SEC} = \left(\frac{V_{INMIN} \times D_{MAX}}{L_{PRI} \times F_{SW} \times K}\right)$$
(Eq. 34)

For the purpose of current-limit setting, the peak current can be calculated as follows:

 $I_{\text{LIM}} = I_{\text{PRIPEAK}} \times 1.2 \tag{Eq. 35}$ 

#### Primary RCD Snubber Selection

The design procedure for primary RCD snubber selection is identical to that outlined in the DCM Flyback section.

#### **Output Capacitor Selection**

X7R ceramic output capacitors are preferred in industrial applications due to their stability over temperature. The output capacitor is usually sized to support a step load of 50% of the rated output current in nonisolated applications so that the output-voltage deviation is contained to 3% of the rated output voltage. The output capacitance can be calculated as:

$$C_{OUT} = \frac{I_{STEP} \times T_{RESPONSE}}{\Delta V_{OUT}}$$
(Eq. 36)

$$T_{\text{RESPONSE}} \cong \left(\frac{0.33}{F_{\text{C}}} + \frac{1}{F_{\text{SW}}}\right) \tag{Eq. 37}$$

The output capacitor RMS current rating can be calculated as follows:

$$I_{COUTRMS} = I_{OUT} \times \sqrt{\frac{D_{MAX}}{1 - D_{MAX}}}$$
 (Eq. 38)

Where I<sub>STEP</sub> is the load step,  $T_{RESPONSE}$  is the response time of the controller,  $\Delta V_{OUT}$  is the allowable output voltage deviation, and  $F_C$  is the target closed-loop crossover frequency.  $F_C$  is chosen to be less than 1/5 of the worst-case (lowest) RHP zero frequency  $F_{RHP}$ . The right half-plane zero frequency is calculated as follows:

$$F_{ZRHP} = \frac{(1 - D_{MAX})^2 \times V_{OUT}}{2 \times \pi \times D_{MAX} \times L_{PRI} \times I_{OUT} \times K^2}$$
(Eq. 39)

For the CCM flyback converter, the output capacitor supplies the load current when the main switch is on, and therefore, the output-voltage ripple is a function of load current and duty cycle. Use Equation 40

to estimate the output-voltage ripple:

$$\Delta V_{\text{COUT}} = \frac{I_{\text{OUT}} \times D_{\text{MAX}}}{F_{\text{SW}} \times C_{\text{OUT}}}$$
(Eq. 40)

#### Input Capacitor Selection (MAX17596)

Use Equation 41 to calculate the input capacitor for a specified peak-to-peak input switching ripple ( $V_{IN\_RIP}$ ) in low-voltage DC-DC converters operating in CCM mode.

$$C_{IN} = \frac{K \times I_{OUT} \times D_{MAX}}{F_{SW} \times V_{IN}_{RIP}}$$
(Eq. 41)

$$I_{\text{INCRMS}} = K \times I_{\text{OUT}} \times \sqrt{\frac{D_{\text{MAX}}}{1 - D_{\text{MAX}}}}$$
(Eq. 42)

#### Error Amplifier Compensation Design

For nonisolated designs, the output voltage feedback and loop compensation network are connected as shown in Figure 1.

In the CCM flyback converter, the primary inductance and the equivalent load resistance introduces a right half-plane zero at the following frequency:

$$F_{ZRHP} = \frac{(1 - D_{MAX})^2 \times V_{OUT}}{2 \times \pi \times D_{MAX} \times L_{PRI} \times I_{OUT} \times K^2}$$
(Eq. 43)

The loop compensation values are calculated as:

$$R_{Z} = 924 \times \frac{1 + D_{MAX}}{1 - D_{MAX}} \times R_{CS} \times I_{OUT} \times K \times \sqrt{1 + \left[\frac{F_{RHP}}{5 \times F_{P}}\right]^{2}}$$
(Eq. 44)

Where FP, the pole due to output capacitor and load, is given by:

$$F_{P} = \frac{(1+D_{MAX}) \times I_{OUT}}{2 \times \pi \times C_{OUT} \times V_{OUT}}$$
(Eq. 45)

The above selection of  $R_Z$  sets the loop-gain crossover frequency ( $F_C$ , where the loop gain equals 1) equal to 1/5 the right-half plane zero frequency.

 $F_C \leq F_{ZRHP}/5$ 

With the control loop zero placed at the load pole frequency:

(Eq. 46)

$$C_{Z} = \frac{1}{2\pi \times R_{Z} \times F_{P}}$$

With the high-frequency pole placed at half the switching frequency:

$$C_{P} = \frac{1}{\pi \times R_{Z} \times F_{SW}}$$
(Eq. 47)

# Isolated Flyback with Optocoupler Feedback

Optocoupler feedback is used in isolated flyback converter designs for precise control of isolated output voltage. This section describes the different configurations of a controller and outlines a general procedure to calculate compensating network component values. Flyback converter designs, operating in both DCM and CCM, are covered.

The overall scheme of optocoupler feedback is shown in Figure 2.



Figure 2. Optocoupler feedback for isolated flyback designs.

Use  $R_{FB} = 470\Omega$  (typical), for an optocoupler transistor current of 1mA. Select  $R_1 = 49.9k\Omega$  and  $R_2 = 22k\Omega$  (typical values), to use the full range of available COMP voltage. U3 is a low-voltage adjustable shunt regulator with a 1.24V reference voltage. Calculate  $R_{LED}$  using Equation 48, based on output voltage  $V_{OUT}$ .

$$R_{\text{LED}} = 400 \times \text{CTR} \times (V_{\text{OUT}} - 2.7)\Omega$$
 (Eq. 48)

The bandwidth of typical optocouplers limits the achievable closed loop bandwidth of opto-isolated converters. And in CCM flyback designs, the presence of right-half-plane (RHP) zero limits the practical bandwidth of the closed-loop system. Considering these limitations, the closed-loop crossover frequency may be chosen, at the nominal input voltage as follows:

$$f_{\rm C} = 5 \text{kHz}$$
, for DCM designs (Eq. 49)

Or 
$$f_{\rm C} = f_{\rm ZRHP}/10$$
, for CCM designs, limited to  $f_{\rm C} = 5$ kHz (Eq. 50)

Closed-loop compensation values are designed based on the open-loop gain at the desired crossover frequency,  $f_{\rm C}$ . The open-loop gains in DCM and CCM, at  $f_{\rm C}$ , are calculated using the following expressions.

Or 
$$f_{\rm C} = f_{\rm ZRHP}/10$$
, for CCM designs, limited to  $f_{\rm C} = 5$ kHz (Eq. 50)

$$G_{PLANT} = \frac{f_P}{f_C} \times \sqrt{\frac{L_{PRI} \times f_{SW} \times V_{OUT}}{8 \times I_{OUT}}} \times \frac{V_{IN}}{(V_{IN} \times R_{CS} + 50 \times 10^3 \times L_{PRI})}, \text{ for DCM designs (Eq. 51)}$$

And

$$G_{PLANT} = \frac{f_P}{f_C} \times \frac{V_{IN}^2 \times V_{OUT}}{2 \times I_{OUT} \times (2 \times V_{OUT} + K \times V_{IN}) \times (V_{IN} \times R_{CS} + 50 \times 10^3 \times L_{PRI})}, \text{ for } (Eq. 52)$$

CCM designs

Where  $K = N_S/N_P$  is the transformer turns ratio  $f_P = I_{OUT}/(\pi \times V_{OUT} \times C_{OUT})$ , for DCM designs

And

$$f_{P} = \frac{(2 \times V_{OUT} + K \times V_{IN}) \times I_{OUT}}{2 \times (V_{OUT} + K \times V_{IN}) \times \pi \times V_{OUT} \times C_{OUT}}, \text{ for CCM designs}$$

Three controller configurations are suggested, based on open-loop gain and the value of R<sub>LED</sub>. For typical designs, the current transfer ratio (CTR) of the optocoupler designs can be assumed to be unity. It is known that the comparator and gate driver delays associated with the input voltage variations affects the optocoupler CTR. Depending on the optocopler selected, variations in CTR causes wide variations in bandwidth of the closed-loop system across the input-voltage operating range. It is recommended to select an optocoupler with less CTR variations across the operating range.

$$\begin{array}{l} \begin{array}{l} \text{Configuration} \\ 1: \end{array} & \text{When} \left( G_{\text{PLANT}} \times \text{CTR} \times \frac{R_{\text{FB}}}{R_{\text{LED}}} \times \frac{R_1}{R_2} \right) \leq \ 0.8 \end{array} \end{array}$$

$$\begin{array}{l} \text{(Eq. 53)} \\ \text{R}_{\text{F}} = \left( \frac{R_{\text{LED}} \times R_2}{G_{\text{PLANT}} \times \text{CTR} \times R_{\text{FB}} \times R_1} - 1 \right) \times R_{\text{U}} \quad \Omega \\ \\ \text{C}_{\text{F}} = \frac{1}{2\pi \times (R_{\text{U}} + R_{\text{F}}) \times f_{\text{P}}} \text{ Farad} \\ \\ \text{C}_{\text{CF1}} = \frac{1}{\pi \times f_{\text{SW}} \times R_{\text{F}}} \text{ Farad} \end{array}$$



The schematic for this controller configuration is depicted in Figure 3.

Figure 3. Controller configuration 1.



The schematic for this controller configuration is depicted in Figure 4.



Figure 4. Controller configuration 2.

Configuration 3: When 0.8 <  $\left(G_{PLANT} \times CTR \times \frac{R_{FB}}{R_{LED}} \times \frac{R_1}{R_2}\right)$  < 1.2 (Eq. 55)  $C_{CF2} = \frac{1}{\pi \times R_1 \times f_{SW}}$  Farad  $C_{CF1} = \frac{1}{2\pi \times R_U \times f_P}$  Farad

The schematic for this controller configuration is depicted in Figure 5.



Figure 5. Controller configuration 3.

# **Bias Winding Supply Configuration**

The MAX17595 is implemented with a 20V V<sub>IN</sub> UVLO wake-up level with 13V hysteresis to optimize the size of bias capacitor. A simple RC circuit is used to start up the MAX17595. To sustain the operation of the circuit, the input supply to the IC is bootstrapped through diode D2 as shown in **Figure 6** (refer to the MAX17595–7 data sheet to design the startup network).



Figure 6. IN supply configuration for an offline isolated design.

# Turns Ratio Calculation (N<sub>B</sub>/N<sub>P</sub>)

The transformer turns ratio ( $K_B = N_B/N_P$ ) can be calculated as follows:

$$K_{b} = K \times \frac{V_{BIAS} + V_{D2}}{V_{OUT} + V_{D1}}$$
(Eq. 56)

# Bias Capacitor (CSTART) Calculation

In isolated applications where a bias winding configuration is used to power up MAX17595/MAX17596,  $C_{\text{START}}$  can be calculated as follows:

$$C_{\text{START}} = 0.75 \times (C_{\text{DRV}} + 0.1 \times I_{\text{IN}} \times T_{\text{SS}} + 0.04 \times T_{\text{SS}} \times Q_{\text{G}} \times F_{\text{SW}})$$
(Eq. 57)

## Feedback Potential Divider Selection (RU, RB)

For all the applications that use a startup network to bias IN pin during the power-up sequence, calculate the feedback potential divider using the following formulas.

$$R_{B} = \frac{10 \times (30 \times C_{START} - 20 \times C_{DRV} - I_{IN} \times T_{SS})}{V_{OUT} \times C_{OUT} \times (I_{IN} + Q_{G} \times F_{SW})} \Omega$$
(Eq. 58)

$$\mathbf{R}_{\mathbf{U}} = \left(\frac{\mathbf{V}_{\mathbf{OUT}}}{\mathbf{V}_{\mathsf{REF}}} - 1\right) \times \mathbf{R}_{\mathsf{B}} \,\,\Omega \tag{Eq. 59}$$

Where  $V_{REF}$  is the reference set by the secondary side controller (e.g.,  $V_{REF} = 1.24V$  for TLV431)

 $C_{START}$  is the startup capacitor,  $C_{DRV}$  is the cumulative capacitor used at the DRV pin, I<sub>IN</sub> is the MAX17595 quiescent current, T<sub>SS</sub> is the soft-start time, V<sub>OUT</sub> is the output voltage, C<sub>OUT</sub> is the output capacitor used, and Q<sub>G</sub> is the gate charge of the primary n-channel MOSFET.

The bias winding configuration is not needed in low-voltage DC-DC applications where the input voltage can be directly used for IC supply, as shown in **Figure 7**. Using the input supply directly for the IC eliminates the external RC startup network and bias winding circuit. The MAX17596 is optimized for such low-voltage DC-DC applications with UVLO  $V_{IN}$  wake-up level of 4.1V (typ) with 200mV hysteresis. In such applications where bias winding is not used, the feedback potential divider may be chosen as follows:

Choose  $R_B = 10k\Omega$  (typ)

$$R_{U} = \left(\frac{V_{OUT}}{V_{REF}} - 1\right) \times R_{B} \Omega$$

(Eq. 60)



Figure 7. The IN supply configuration for low-voltage isolated DC-DC designs.

# **Typical Operating Circuit**



More detailed image (PDF, 304kB) Figure 8. The MAX17595 typical application circuit.

# Design Calculations for the MAX17595-Based Isolated DCM Flyback Converter

# **Technical Specifications**

Input voltage range: 85VAC to 265VAC Output voltage: 15V

Rated output current: 1.5A Switching frequency: 120kHz Operating mode: Discontinuous Conduction Mode (DCM)

1. Primary inductance selection

In offline applications, the DC bus voltage varies from 120VDC to 375VDC. But the actual minimum input operating voltage depends on the 100Hz ripple present on the DC bus capacitor. In this application, the ripple is assumed to be 30V and hence the minimum DC input to the converter is 90V.

$$L_{\text{PRIMAX}} \leq \frac{(V_{\text{INMIN}} \times D_{\text{MAX}})^2 \times 0.4}{(V_{\text{OUT}} + V_{\text{D}}) \times I_{\text{OUT}} \times F_{\text{SW}}} = 210 \mu \text{H}$$

Where  $V_{\text{INMIN}}$  = 90V,  $D_{\text{MAX}}$  = 0.43,  $V_{\text{D}}$  = 0.8V

Select primary inductance  $L_{PRI} = 190 \mu H$  to account for 10% tolerance on primary inductance.

2. Maximum duty cycle calculation with selected LPRI

$$\mathsf{D}_{\mathsf{NEW}} = \frac{\sqrt{2.5 \times \mathsf{L}_{\mathsf{PRI}} \times (\mathsf{V}_{\mathsf{OUT}} + \mathsf{V}_{\mathsf{D}}) \times \mathsf{I}_{\mathsf{OUT}} \times \mathsf{F}_{\mathsf{SW}}}}{\mathsf{V}_{\mathsf{INMIN}}} = 0.4$$

3. Turns ratio calculation (K = N<sub>S</sub>/N<sub>P</sub>)

$$K = \frac{V_{OUT} + V_D \times (1 - D_{NEW})}{V_{INMIN} \times D_{NEW}} = 0.263$$

4. Peak/RMS current calculation

$$I_{PRIPEAK} = \frac{V_{INMIN} \times D_{NEW}}{L_{PRI} \times F_{SW}} = 1.58A$$

$$I_{PRIRMS} = I_{PRIPEAK} \times \sqrt{\frac{D_{NEW}}{3}} = 0.58A$$

$$I_{\text{SECPEAK}} = \frac{I_{\text{PRIPEAK}}}{K} = 6A$$
$$I_{\text{SECRMS}} = \sqrt{\frac{2 \times I_{\text{OUT}} \times I_{\text{PRIPEAK}}}{3 \times K}} = 2.45 \text{ A}$$

5. Primary snubber selection

$$C_{10} = \frac{2 \times L_{LK} \times I_{PRIPEAK}^2 \times K^2}{V_{OUT}^2} = 2.9 \text{nF}$$

Where leakage inductance  $L_{LK} = 1.9 \mu H (1\% \text{ of } L_{PRI})$ 

Considering the derating of the snubber capacitor, select  $C_{10} = 3.3$ nF.

$$P_{R18} = 0.833 \times L_{LK} \times I_{PRIPEAK^2} \times F_{SW} = 0.47W$$

$$R_{18} = \frac{6.25 \times V_{OUT}^2}{P_{SNUB} \times K^2} = 43.26 k\Omega$$

$$V_{D3} = V_{INMAX} + \left(2.5 \times \frac{V_{OUT}}{K}\right) = 518V$$

6. Output capacitor selection

F<sub>C</sub> = 5kHz, typical bandwidth at nominal voltage for isolated applications

 $I_{STEP} = 0.25 \times I_{OUT} = 0.375A$  (25% of  $I_{LOAD}$ , typical for isolated applications)

 $\Delta V_{OUT} = 450 \text{mV}$  (3% of  $V_{OUT}$ , typical)

$$T_{\text{RESPONSE}} \cong \left(\frac{0.33}{F_{\text{C}}} + \frac{1}{F_{\text{SW}}}\right) = 74.3 \mu \text{s}$$

$$C_{\text{OUT}} = \frac{I_{\text{STEP}} \times T_{\text{RESPONSE}}}{\Delta V_{\text{OUT}}} = 62 \mu \text{F}$$

$$I_{\text{COUTRMS}} = I_{\text{OUT}} \times \sqrt{\frac{2 \times I_{\text{PRIPEAK}}}{3 \times \text{K} \times I_{\text{OUT}}}} - 1 = 1.96 \text{A}$$

Actual output capacitance used in the application is:  $C_{13,14,15,16} = 30\mu F$  (with  $22\mu F/25V \times 4$  capacitors after derating)

**Note**: Capacitor values change with temperature and applied voltage. Refer to capacitor data sheets to select capacitors that guarantee the required output capacitance across the operating range. For design calculations, use the worst-case derated value of capacitance, based on temperature range and applied voltage.

$$\Delta V_{\text{COUT}} = \frac{I_{\text{OUT}} \times [I_{\text{PRIPEAK}} - (K \times I_{\text{OUT}})]^2}{I_{\text{PRIPEAK}}^2 \times F_{\text{SW}} \times C_{\text{OUT}}} = 236 \text{mV}$$

7. Input capacitor selection based on 100Hz ripple on DC bus voltage

 $\eta = 0.85$  (typical efficiency)  $P_{LOAD} = 15 \times 1.5 = 22.5W$ 

$$C_5 = \frac{0.045 \times P_{LOAD}}{\eta \times V_{IN,PK}^2} = 83 \mu F$$

$$I_{\text{INCRMS}} = \frac{2.7 \times P_{\text{LOAD}}}{\eta \times V_{\text{IN,PK}}} = 0.6A$$

8. External MOSFET selection

$$V_{N1} = V_{INMAX} + \left[ \left( \frac{V_{OUT} + V_{DIODE}}{K} \right) \times 2.5 \right] = 530V$$

9. Secondary diode selection

$$V_{D4} = 1.25 \times (K \times V_{INMAX} + V_{OUT}) = 140V$$

#### 10. Bias winding supply configuration

For offline applications, bias supply configuration as shown in Figure 6 is used to power up the MAX17595.

Use  $V_{BIAS} = 12V$ ,  $V_{D2} = 0.8V$ ,  $V_{D1} = 0.8V$ , K = 0.24,  $C_{DRV} = 1\mu$ F,  $I_{IN} = 2m$ A,  $Q_G = 35$ nC (STB11NM80), R1 = 49.9k $\Omega$ , R2 = 22k $\Omega$  for the following calculations.

Select soft-start time  $T_{SS}$  = 12ms (refer to the MAX17595/MAX17596/MAX17597 data sheet for programming soft-start time).

#### 11. Output-voltage soft-start time calculation

In isolated designs, the output-voltage soft-start time depends on the values of  $T_{SS}$ , R1, and R2 and can be calculated as follows:

$$T_{SSactual} = \frac{T_{SS}}{1 + \frac{R_1}{R_2}} = 3.67 \text{ms}$$

**Note**: The above equation provides an approximate output-voltage soft-start time. Due to the presence of the optocircuit, the actual soft-start may be different from the programmed soft-start time. It is recommended to adjust the soft-start capacitor to get the required soft-start time.

12. Bias turns ratio selection (K<sub>B</sub> = N<sub>B</sub>/N<sub>P</sub>)

$$K_b = K \times \frac{V_{BIAS} + V_{D2}}{V_{OUT} + V_{D1}} = 0.21$$

13. Startup capacitor selection

 $C_9 = 0.75 \times (C_{DVR} + 0.1 \times I_{IN} \times T_{SS} + 0.04 \times T_{SS} \times Q_G \times F_{SW}) = 4\mu F$ 

**Note**: Usually the bias voltage is in the range of 12V to 20V, so it is suggested to consider the derating of the startup capacitor. Improper selection of the  $C_{START}$ ,  $R_L$ , and  $R_U$  may result in an unnecessary power up sequence if IN supply falls below the UVLO lower threshold during circuit operation.

14. Feedback potential divider selection

$$\mathsf{R}_{29} = \frac{10 \times (30 \times \mathsf{C}_{\mathsf{START}} - 20 \times \mathsf{C}_{\mathsf{DRV}} - \mathsf{I}_{\mathsf{IN}} \times \mathsf{T}_{\mathsf{SS}})}{\mathsf{V}_{\mathsf{OUT}} \times \mathsf{C}_{\mathsf{OUT}} \times (\mathsf{I}_{\mathsf{IN}} + \mathsf{Q}_{\mathsf{G}} \times \mathsf{F}_{\mathsf{SW}})} = 272\Omega$$

Select  $R_{29} = 221\Omega$ 

$$R_{28} = \left(\frac{V_{OUT}}{1.24} - 1\right) \times R_{29} = 2.5 k\Omega$$

15. Isolated flyback with opto-isolated feedback compensation design

Choose V<sub>IN</sub> = 325VDC, R1 = 49.9k $\Omega$ , R2 = 22k $\Omega$ , R<sub>FB</sub> = 470 $\Omega$ , CTR = 1 (all typical values)

$$R_{CS} = 0.2\Omega$$

 $R_{26} = 400 \times CTR \times (V_{OUT} - 2.7)\Omega = 4.9k\Omega$ 

Choose  $f_C = 5kHz$  (typical, at nominal input voltage of 325VDC)

$$f_{P} = \frac{I_{OUT}}{\pi \times V_{OUT} \times C_{OUT}} = 1060 \text{Hz}$$

$$G_{PLANT} = \frac{f_P}{f_C} \times \sqrt{\frac{L_{PRI} \times f_{SW} \times V_{OUT}}{8 \times I_{OUT}}} \times \frac{V_{IN}}{(V_{IN} \times R_{CS} + 50 \times 10^3 \times L_{PRI})} = 4.94$$
$$G_{PLANT} \times CTR \times \frac{R_{FB}}{R_{LED}} \times \frac{R_1}{R_2} = 1.1$$

Since the loop gain is less than **1.2**, the third configuration shown in the isolated compensation design should be used for this application.

$$C_{17} = \frac{1}{2\pi \times R_U \times f_P} = 60nF$$

Select  $C_{17} = 68nF$ 

$$C_4 = \frac{1}{\pi \times R_1 \times f_{SW}} = 53 pF$$

Select  $C_4 = 56pF$ 

DesignationQtyDescriptionC11 $0.1\mu$ F 20% 275VAC X2 plastic film capacitor (17mr ECQ-U2A104MLC4156pF 5% 50V C0G ceramic capacitor (0603) MuratC51 $100\mu$ F 20% 450V aluminium electrolytic capacitor ( Panasonic ECO-S2GP101CAC6, C212 $0.47\mu$ F 10% 25V X7R ceramic capacitors (0603) MuratC71 $0.1\mu$ F 10% 16V X7R ceramic capacitor (0603) Murat	a GRM1885C1H560J (25mm diameter) Iurata
C1         1         ECQ-U2A104ML           C4         1         56pF 5% 50V C0G ceramic capacitor (0603) Murat           C5         1         100μF 20% 450V aluminium electrolytic capacitor ( Panasonic ECO-S2GP101CA           C6, C21         2         0.47μF 10% 25V X7R ceramic capacitors (0603) M GRM188R71E474K           C7         1         0.1μF 10% 16V X7R ceramic capacitor (0603) Murat	a GRM1885C1H560J (25mm diameter) Iurata
C51100μF 20% 450V aluminium electrolytic capacitor ( Panasonic ECO-S2GP101CAC6, C2120.47μF 10% 25V X7R ceramic capacitors (0603) M GRM188R71E474KC710.1μF 10% 16V X7R ceramic capacitor (0603) Mur GRM188R71C104K	(25mm diameter) Iurata
C5         1         Panasonic ECO-S2GP101CA           C6, C21         2         0.47µF 10% 25V X7R ceramic capacitors (0603) M GRM188R71E474K           C7         1         0.1µF 10% 16V X7R ceramic capacitor (0603) Mur GRM188R71C104K	Iurata
C6, C21         Z         GRM188R71E474K           C7         1         0.1µF 10% 16V X7R ceramic capacitor (0603) Mur GRM188R71C104K	
GRM188R71C104K	ata
C8 1 1µF 10% 25V X7R ceramic capacitor (0603) Murat	a GRM188R71E105K
C9 1 4.7µF 10% 50V X7R ceramic capacitor (1206) Mur GRM31CR71H475K	ata
C <sub>10</sub> 1 3300pF 10% 250V X7R ceramic capacitor (0805) M GRM21AR72E332K	Murata
C11 1 1000pF 10% 50V X7R ceramic capacitor (0603) M GRM188R71H102K	urata
C13, C14, C15, C16 4 22µF 10% 25V X7R ceramic capacitors (1210) Mu GRM32ER71E226K	rata
C17 1 68nF 10% 50V X7R ceramic capacitor (0603) TDK	C1608X7R1H683K
D1 1 600V 1.5A bridge rectifier (DF-S) Diodes Inc. DF15	506S
D2 1 100V 300mA fast switching diode (SOD-123) Diode	es Inc. 1N4148W-7-F
D3 1 800V 1A ultra-fast rectifier (SMA) Diodes Inc. US1	K-TP
D4 1 200V 6A ultra-fast recovery rectifier (PowerDI 5) D 13	iodes Inc. PDU620-
L1 1 6.8mH 0.8A line filter (13mm x 10mm) Panasonic®	ELF15N008A
N1 1 800V 11A N-channel MOSFET (D2PAK) ST Micro	STB11NM80T4
R1 1 10Ω 2A NTC thermistor (5mm) EPCOS B57153S07	100M000
R2, R3, R4 3 549kΩ 1% resistors (1206)	
R5 1 19.8kΩ 1% resistor (0603)	

R6	1	4.99kΩ 1% resistor (0603)
R9	1	82.5kΩ 1% resistor (0603)
R12	1	49.9kΩ 1% resistor (0603)
R13	1	22kΩ 1% resistor (0603)
R14, R15, R16	3	$402k\Omega$ 1% resistors (1206)
R18	2	100k $\Omega$ 5% resistors (1206) Panasonic ERJ-P08J104V
R19	1	10Ω 1% resistor (0603)
R20	1	100Ω 1% resistor (0603)
R21	1	0.2Ω 1% resistor (1206) Panasonic ERJ-8BSFR20V
R22	1	470Ω 1% resistor (0603)
R26	1	4.99kΩ 1% resistor (0603)
R28	1	2.49kΩ 1% resistor (0603)
R29	1	221Ω 1% resistor (0603)
T1	1	180µH, 0.8A, 1:0.24:0.2 transformer (EFD25) Coilcraft® MA5475-AL
U1	1	Peak-current-mode controller for flyback regulator (16-TQFN 3mm x 3mm x 0.8mm) Maxim MAX17595ATE+
U2	1	Phototransistor (6-DIP) Avago™ 4N35-300E
U3	1	Shunt regulator 1.24V 0.5% (SOT-23-3) Diodes Inc. TLV431BFTA

NOTE: The design methodology for isolated fly back converter using MAX17596 is same as the MAX17595.

Avago is a trademark of Avago Technologies, Inc.

Coilcraft is a registered trademark of Coilcraft, Incorporated.

Panasonic is a registered trademark and registered service mark of Panasonic Corporation.

Related Parts					
MAX17595	Peak-Current-Mode Controllers for Flyback and Boost Regulators	Free Samples			
MAX17596	Peak-Current-Mode Controllers for Flyback and Boost Regulators	Free Samples			

#### More Information

For Technical Support: http://www.maximintegrated.com/support For Samples: http://www.maximintegrated.com/samples Other Questions and Comments: http://www.maximintegrated.com/contact

Application Note 5504: http://www.maximintegrated.com/an5504 APPLICATION NOTE 5504, AN5504, AN 5504, APP5504, Appnote5504, Appnote 5504 © 2013 Maxim Integrated Products, Inc. Additional Legal Notices: http://www.maximintegrated.com/legal