MICRONAS

Application Note

HAL® 24xy, HAR® 24xy

Programming Guide

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Contents

1. General Information

Release Note: **Revision bars indicate significant changes to the previous version.**

This document is intended as guidance for programming the HAL/HAR 24xy sensors using own programming hardware and software. The programming interface as well as all programming procedures for reading and writing data to the sensor's memory are described in detail. In combination with their respective data sheets and the application note "HAL/HAR 24xy User Manual" it represents the complete customer documentation of the HAL/HAR 24xy, high-precision programmable linear Hall-effect sensors with arbitrary output characteristics.

1.1. Certification

TDK-Micronas GmbH fulfills the requirements of the international automotive standard IATF 16949 and is certified according to ISO 9001. This ISO standard is a worldwide accepted quality standard.

1.2. Support

We advise you to register on https://service.micronas.com in order to obtain access to the workgroups for our various product families. Here you are able to get support by opening a support ticket in the customer support system.

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2. Programming Interface

2.1. Physical Layer

The implemented memory access is based on the Biphase-M encoding scheme. Biphase-M uses a constant bit time over the entire telegram. A logical *0* is coded as no level change within the bit time. A logical *1* is coded as a level change in the middle of the bit time. After each bit, a level change occurs regardless of the coded logical value.

An example of the Biphase-M data coding/encoding scheme is given in Fig. 2–1.

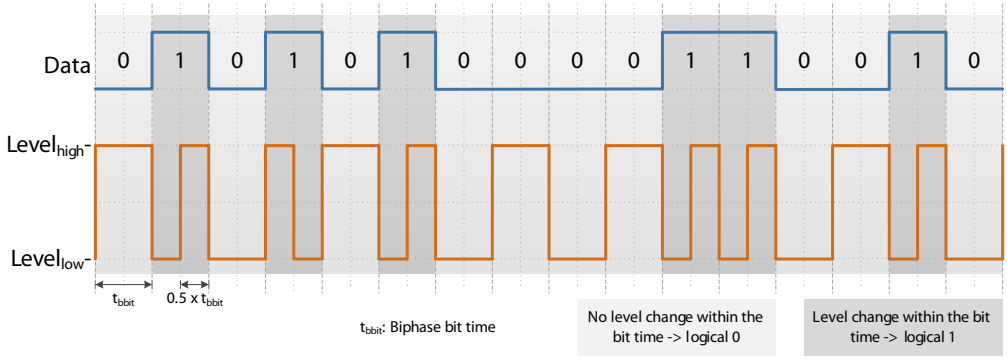

Fig. 2–1: Example of Biphase-M data coding/encoding scheme

The Biphase protocol implemented in the HAL/HAR 24xy can be used with one of two possible physical layers. These differ only in the way the input direction to the sensor is realized. The response always occurs at the OUT Pin

2.2. Data Link and Transport Layer

The sensor can be programmed via supply voltage modulation or via output voltage modulation. The default mode is the programming via the output voltage modulation. The sensor transmits either a data telegram, or sends an acknowledge by a modulation of the output voltage.

The frame structure of communication via VSUP Pin is described in Section 2.2.1 and the frame structure of communication via OUT Pin is described in Section 2.2.2.

2.2.1. Frame Structure of Communication via VSUP Pin

This section shows the frame structure of the read, write, and set base address commands via VSUP Pin. In order to assure a successful communication the host has to ensure that VSUP lies within the specified limits for V_{H_SUPL} and V_{H_SUPH}.

Note: All used abbreviations in the following figures can be found in Table 2–2.

Read Frame

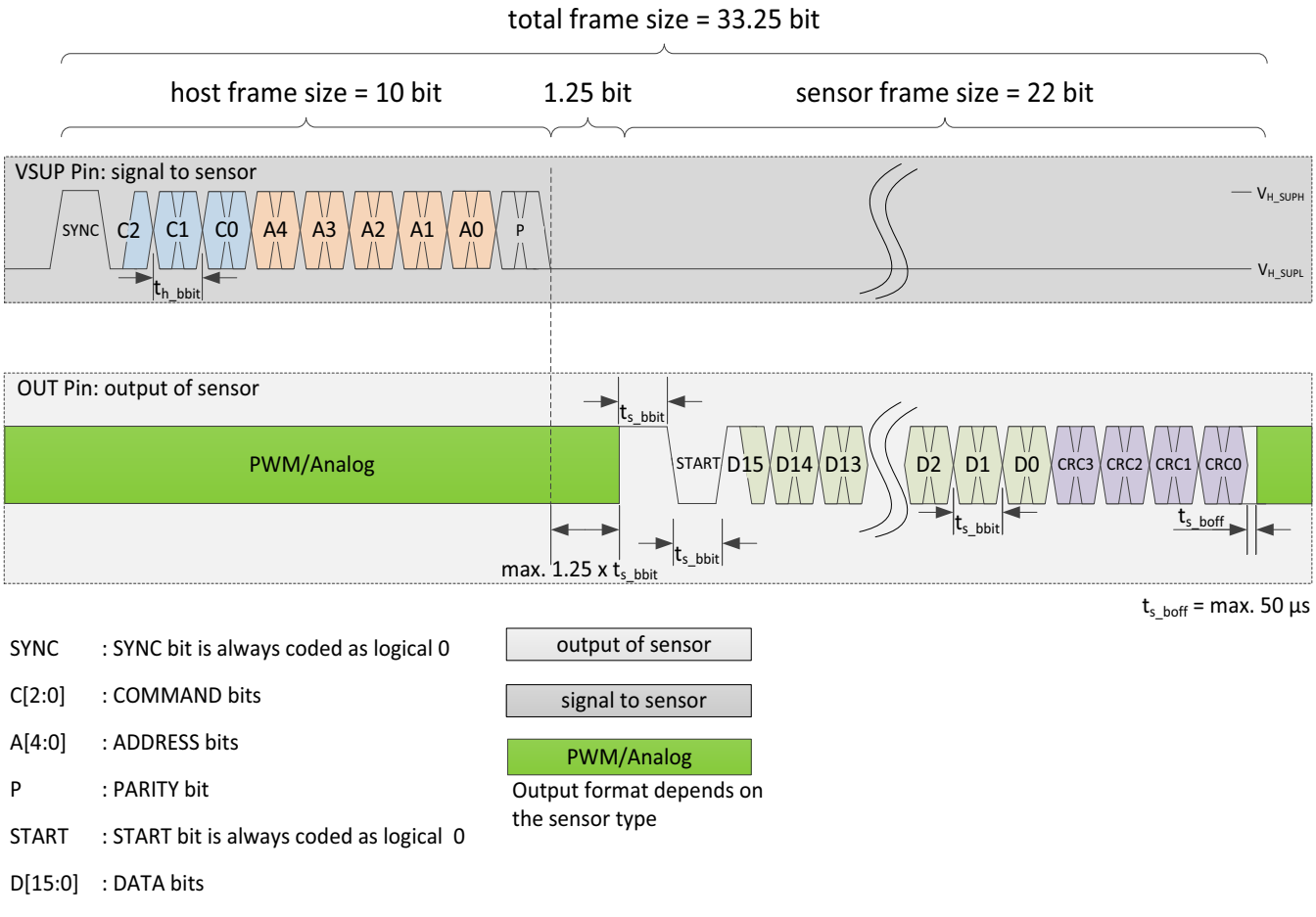

Fig. 2–2: Read frame structure of communication via VSUP Pin

The parity bit will always end with the V_{H_SUPL} level. After max. 1.25 x t_{s_bbit} the sensor starts with the transmission of the data.

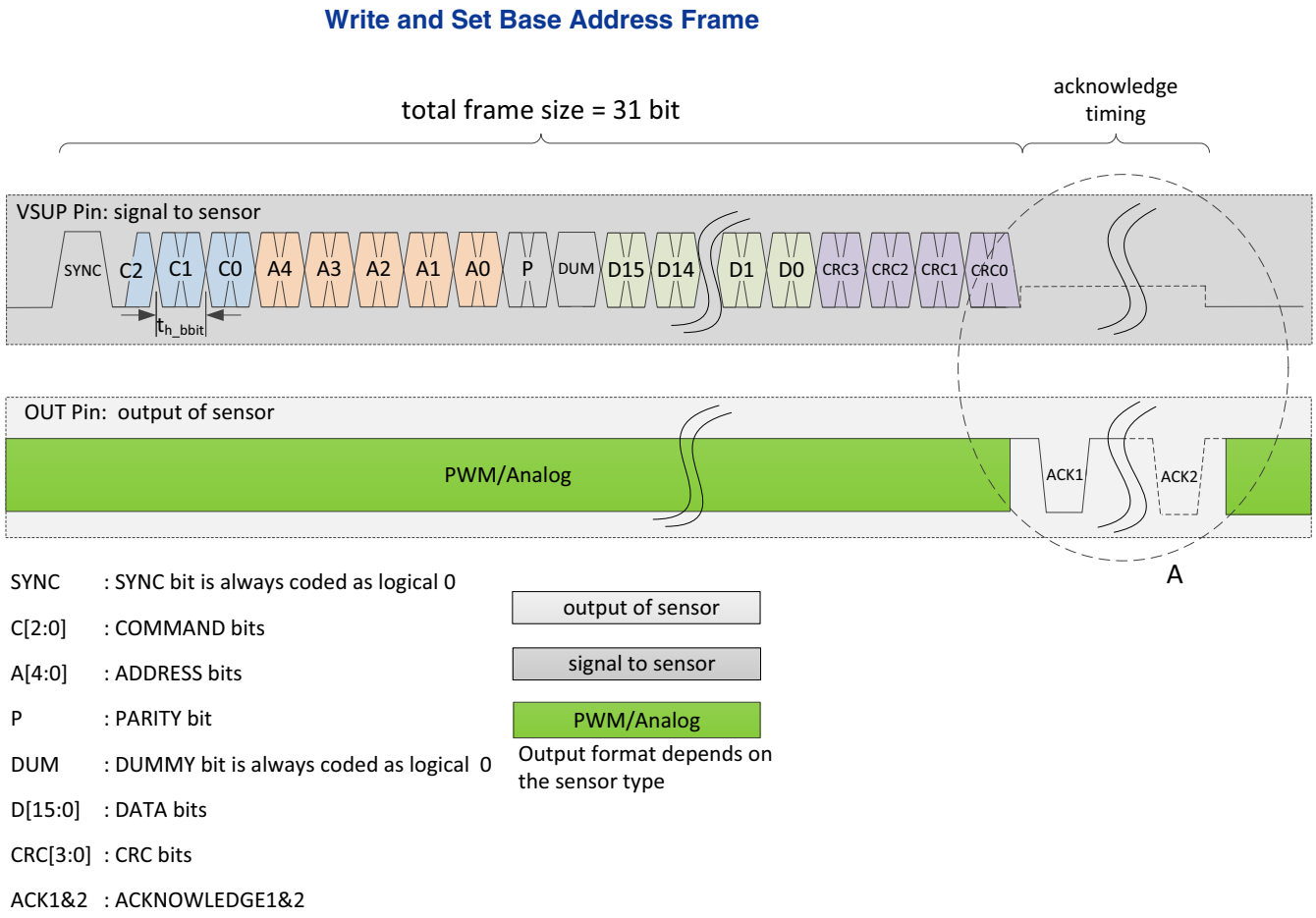

Fig. 2–3: Write and set base address frame structure of communication via VSUP Pin

The write and set base address commands use the same frame structure. The set base address command is used to switch between the four different banks of the sensor. The difference between the commands is explained in Section 3.2 and Section 3.4.

The transmission of the second acknowledge (ACK2) depends on a successful programming of the sensor.

Setting a base address or writing NVRAM registers (see Table 5–1) does not trigger a programming. Therefore only the first acknowledge (ACK1) is transmitted by the sensor, when the command and the CRC have been correctly received. Whether the first acknowledge (ACK1) is transmitted after t_{s_bbit} or 1.25 x t_{s_bbit} depends on the termination of the CRC0 bit (case A and case B).

Fig. 2–4 shows the response of the sensor (Detail A in Fig. 2–3) without programming of the sensor.

Detail A (acknowledge and voltage level) without programming

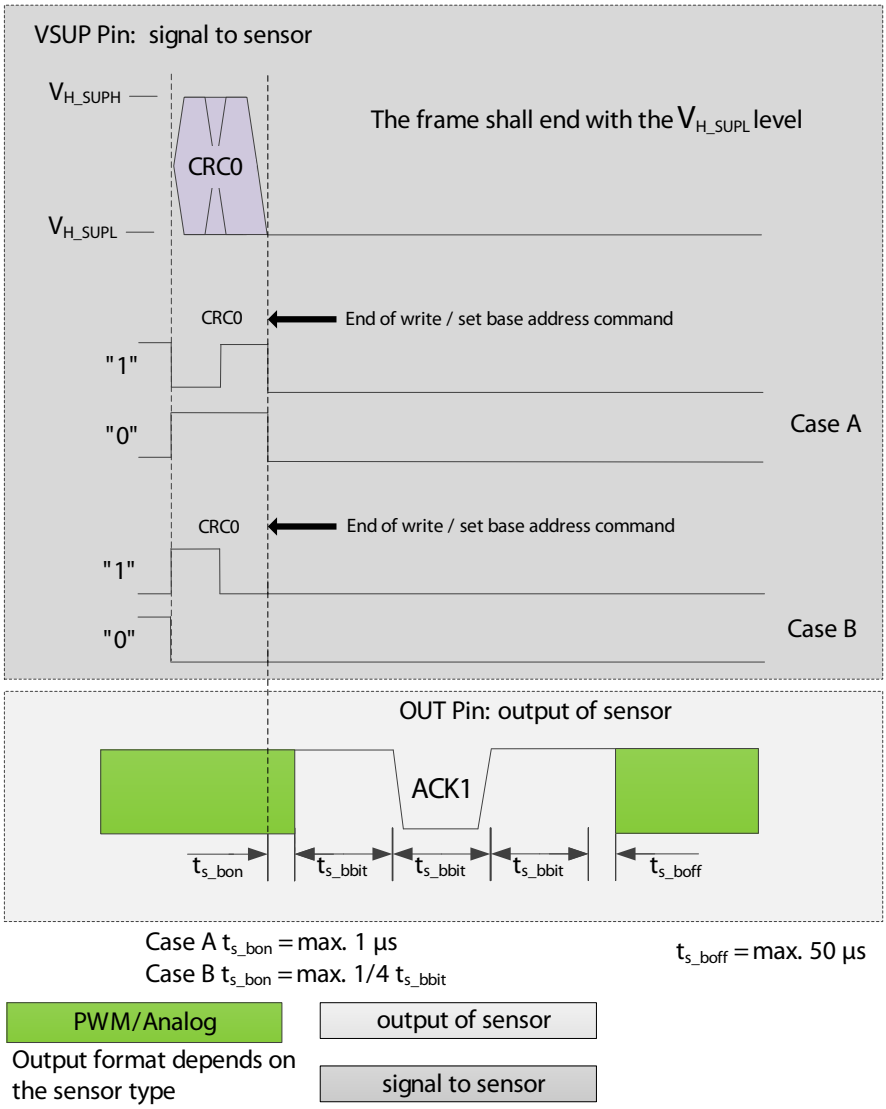

Fig. 2–4: Response from sensor without programming

Writing EEPROM registers and setting the PROG-ERASE bit in the PROG_DIAGNOSIS register (see Table 5–2) triggers the erase and program sequence of the sensor. When the command and the CRC were correctly received, and the programming was successful, two acknowledges are transmitted. Whether the first acknowledge (ACK1) is transmitted after t_{s_bbit} or 1.25 x t_{s_bbit} depends on the termination of the CRC0 bit (case A and case B).

If ACK1 is not detected within t_{s_bon} + 3 t_{s_bbit} after the completion of the data frame transmission, the transmission has to be assumed unsuccessful and a retransmission is required.

Fig. 2–5 shows the response of the sensor (Detail A in Fig. 2–3) with successful programming of the sensor.

Detail A (acknowledge and voltage level) with successful programming

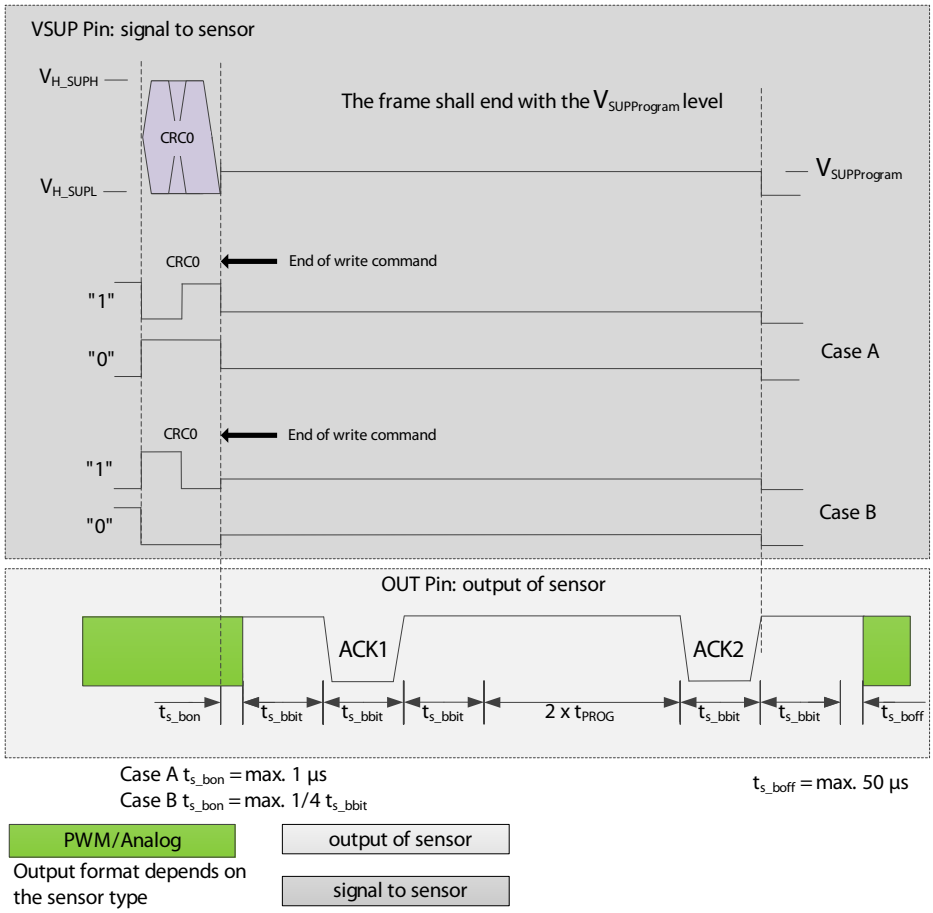

Fig. 2–5: Response from sensor after successful programming

Note: To ensure that the host does not misinterpret the PWM duty cycle of the HAL/HAR 2455 as an acknowledge, it is mandatory to set CLAMP-HIGH to 0% during programming. Additionally, the Diagnosis Latch bit (see Table 5–4) shall be set during end of line testing. Without this precaution programming errors will not be indicated by the second acknowledge.

To enable debugging of the production line it is recommended to read back the PROG_DIAGNOSIS register and the DIAGNOSIS register (see Table 5–1) in case of a missing second acknowledge.

2.2.2. Frame Structure of Communication via OUT Pin

This section shows the frame structure of the read, write, and set base address commands via OUT Pin.

Read Frame

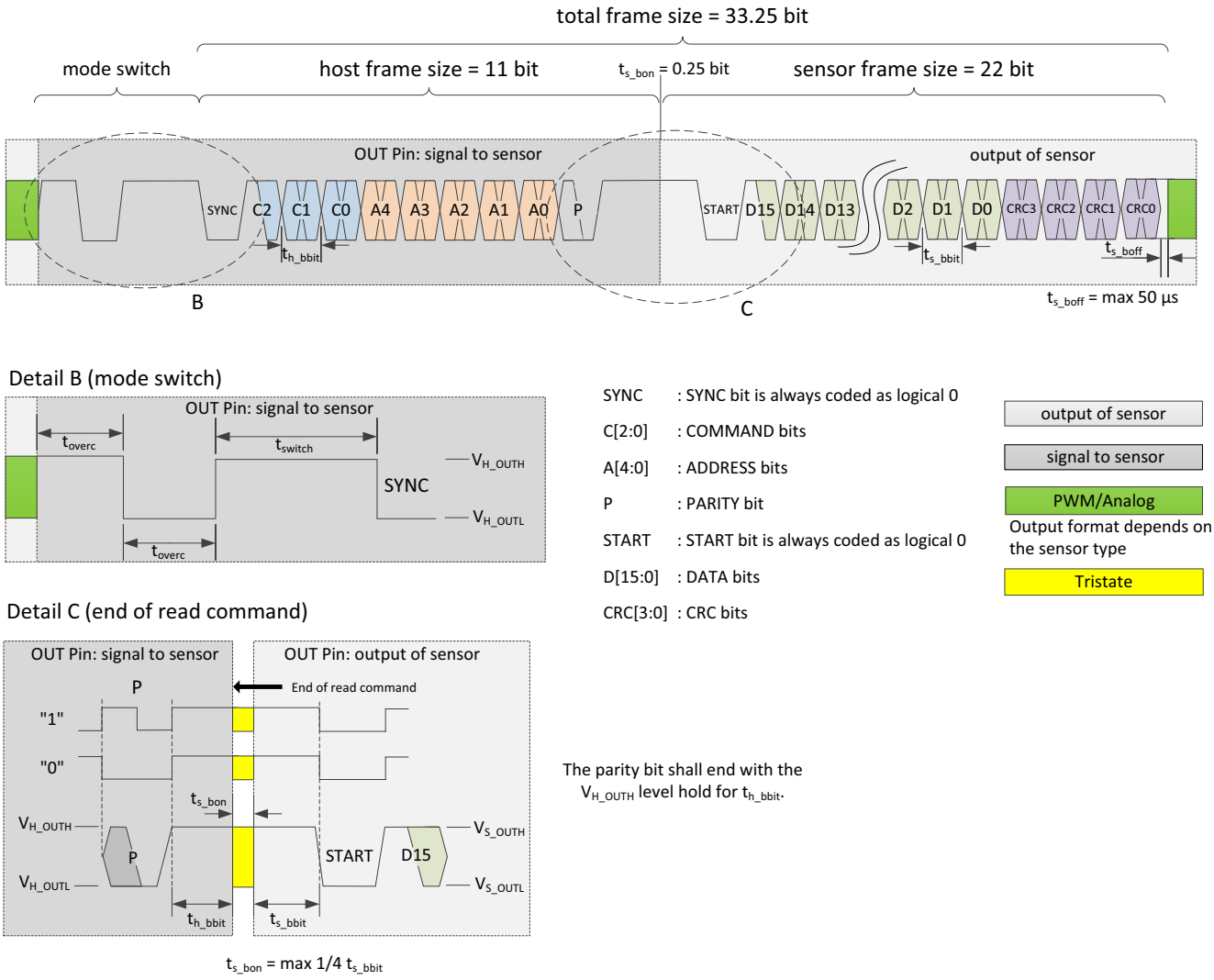

Fig. 2–6: Read frame structure of communication via OUT Pin

Detail B (mode switch):

By driving the voltage at the sensor OUT Pin to V_{SUP} for a duration of t_{overc} (over current pulse duration) followed by driving the voltage at the sensor OUT Pin to GND for t_{overc} with I_{out_oc} (output over current) it is ensured that the sensor will switch within t_{switch} after the actual over current event from application mode into programming mode.

The sensor detects an applied overcurrent within 128 µs either for a positive or a negative current. Depending on the application mode output signal, the minimum overcurrent pulse length necessary for ensuring the detection of an overcurrent event may vary. Table 2–1 indicates the minimum overcurrent pulse lengths t_{overc} for the available PWM output frequencies of the HAL/HAR 2455.

Table 2–1: Min. required overcurrent pulse length (t_{overc}) for HAL/HAR 2455

PWM Frequency (Hz)	t_{overc} (ms)
2000	0.83
1000	0.83
500	1.2
250	2.7

After a successful changeover into the programming mode the sensor switches back into the application mode, if no valid Biphase protocol is detected within $t_{timeout}$, or after a valid Biphase telegram is finished.

Detail C (end of read command)

The parity bit shall always end with the V_{H_OUTL} level. It is mandatory for the sensor that the parity bit is completed with a rising edge to V_{H_OUTH}. The V_{H_OUTH} level shall be hold for 1 bit time t_{h_bbit} before switching the host tristate. After this bit time the sensor needs time (t_{s_bon}) to enable the sensor Biphase driver. The sensor drives the output to V_{S_OUTH} for 1 bit time (t_{s_bbit}) before the protocol starts with a zero.

Write and Set Base Address Frame

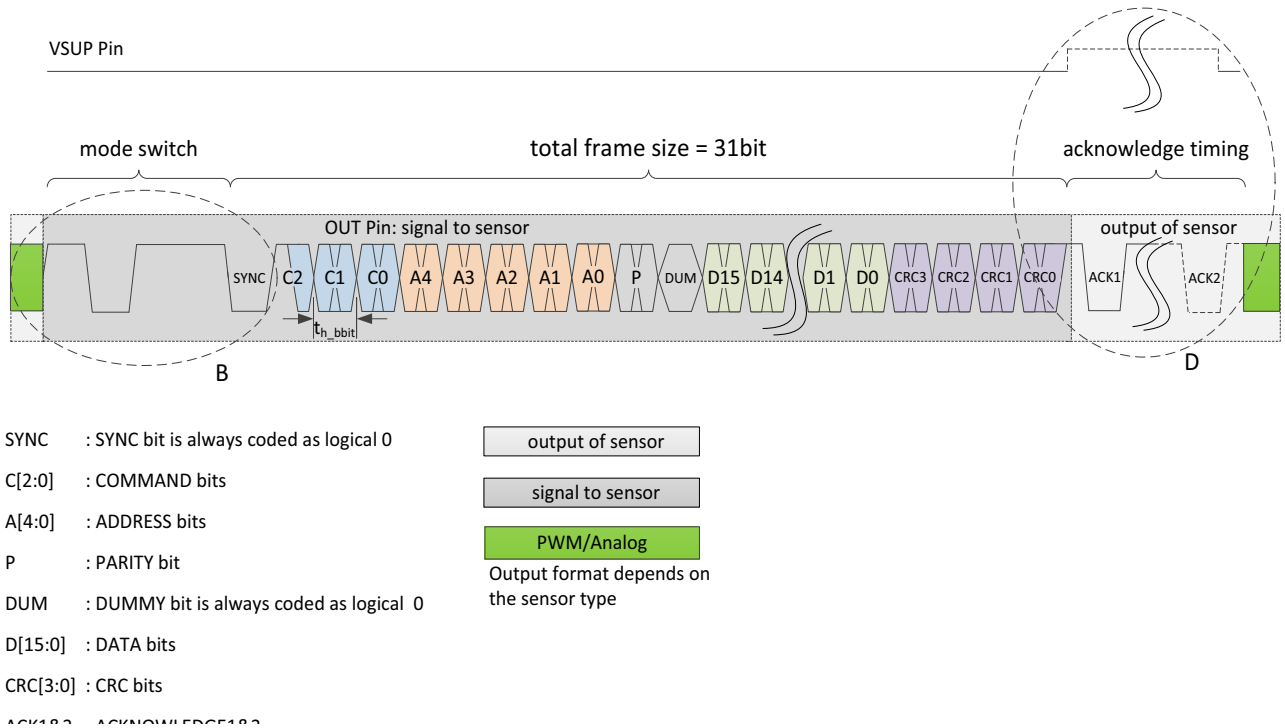

Fig. 2–7: Write and set base address structure of communication via OUT Pin

Detail B is shown in Fig. 2–6.

The write and set base address commands use the same frame structure. The set base address command is used to switch between the four different banks of the sensor.

The transmission of the second acknowledge (ACK2) depends on a successful programming of the sensor.

Setting the base address, or writing a NVRAM register (see Table 5–1) does not trigger a programming. Therefore, only the first acknowledge (ACK1) is transmitted by the sensor when the command and the CRC were correctly received. Whether the first acknowledge (ACK1) is transmitted after t_{s_bbit} or 1.25 x t_{s_bbit} depends on the termination of the CRC0 bit (case A and case B).

Fig. 2–8 shows the response of the sensor (Detail D in Fig. 2–7) without programming of the sensor.

Detail D (acknowledge and voltage level) without programming

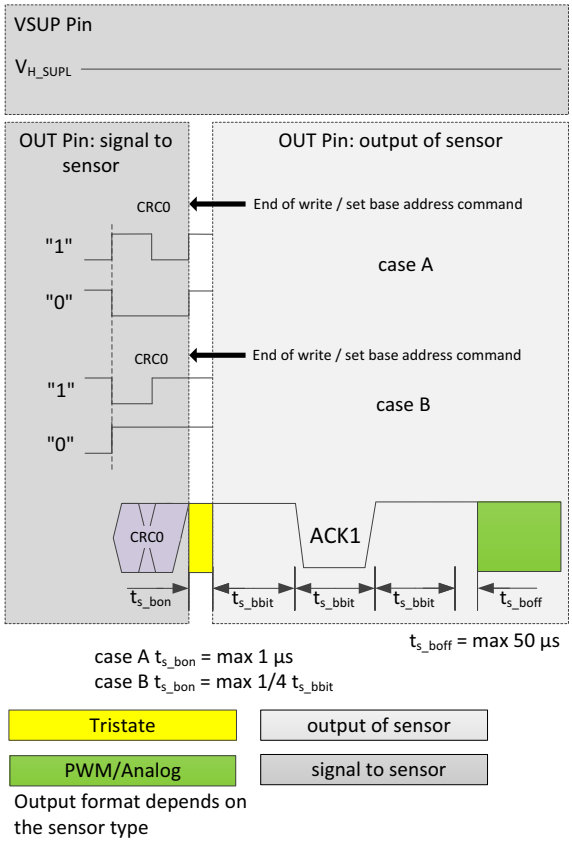

Fig. 2–8: Response from sensor without programming

Writing EEPROM registers and setting the PROG-ERASE bit in the PROG_DIAGNOSIS register (see Table 5–2) triggers the erase and program sequence of the sensor. When the command and the CRC were correctly received, and the programming was successful, two acknowledges are transmitted. Whether the first acknowledge (ACK1) is transmitted after t_{s_bbit} or 1.25 x t_{s_bbit} depends on the termination of the CRC0 bit (case A and case B).

If ACK1 is not detected within t_{s_bon} + 3 t_{s_bbit} after the completion of the data frame transmission, the transmission has to be assumed unsuccessful and a retransmission is required.

Fig. 2–9 shows the transmission of the sensor (Detail D in Fig. 2–7) with successful programming of the sensor.

Detail D (acknowledge and voltage level) with successful programming

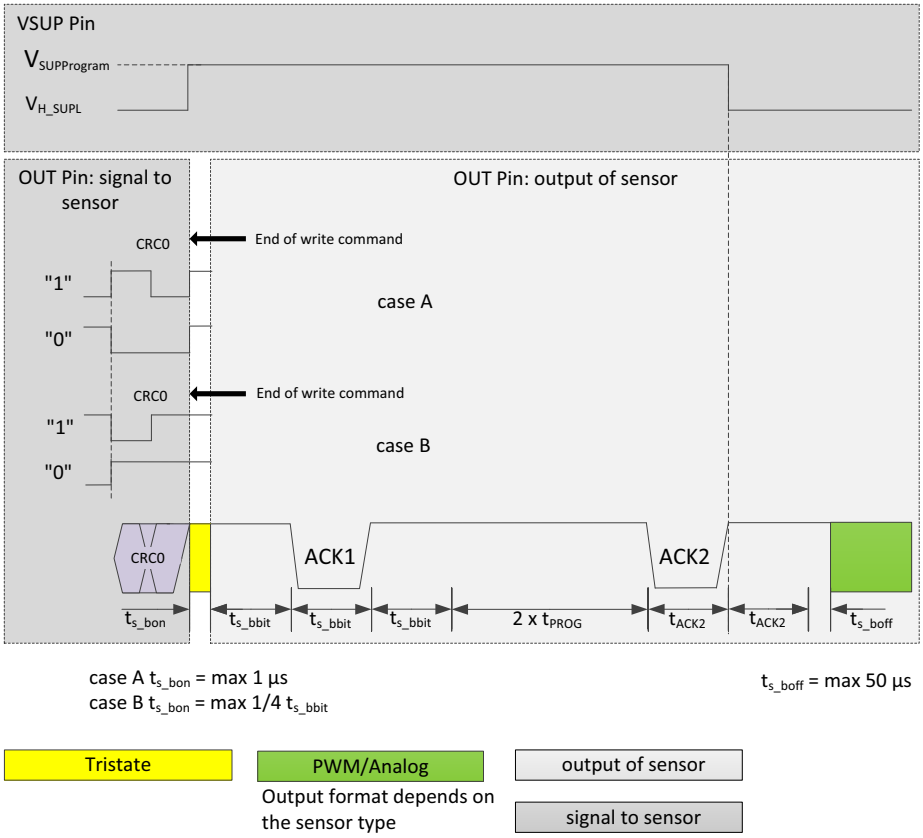

Fig. 2–9: Response from sensor after successful programming

Note: To ensure that the host does not misinterpret the PWM duty cycle of the HAL/HAR 2455 as an acknowledge, it is mandatory to set CLAMP-HIGH to 0% during programming. Additionally, the Diagnosis Latch bit (see Table 5–4) shall be set during end of line testing. Without this precaution programming errors will not be indicated by the second acknowledge.

To enable debugging of the production line it is recommended to read back the PROG_DIAGNOSIS register and the DIAGNOSIS register (see Table 5–1) in case of a missing second acknowledge.

The minimum time between consecutive frames, independently from the communication pin, is described in Fig. 2–10.

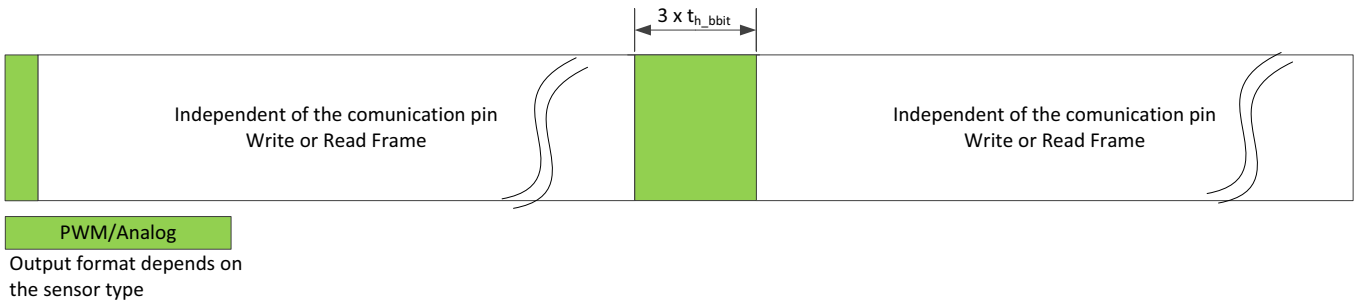

Fig. 2–10: Time between consecutive frames

2.3. Telegram Parameters

Table 2–2: Biphase telegram parameters

Symbol	Parameter	Pin No.	Limit Values			Unit	Comment
			Min.	Typ.	Max.		
$V_{SUPProgram}$	Supply voltage during EEPROM & NVRAM programming	1	5.7	6	6.5	V	
t_{h_bbit}	Host Biphase bit time	1/3	950	1000	1050	µs	
SR_H	Slew rate	1/3	0.23	–	–	V/µs	
Programming via VSUP Pin (Detail A)							
V_{H_SUPL}	Host supply voltage for low level during programming via sensor VSUP Pin	1	5	–	6	V	
V_{H_SUPH}	Host supply voltage for high level during programming via sensor VSUP Pin	1	8	–	9	V	
Biphase frame characteristic via OUT Pin							
V_{H_OUTL}	Host OUT Pin voltage for low level during programming	3	–	–	0.5	V	
V_{H_OUTH}	Host OUT Pin voltage for high level during programming	3	4.5	–	–	V	
Programming via OUT Pin (Detail C)							
t_{overc}	Overcurrent pulse duration	3	0.128	2	–	ms	
t_{switch}	Time to switch sensor from application mode into programming mode	3	2	4	–	ms	
I_{out_oc}	Overcurrent threshold	3	20	–	–	mA	
$t_{timeout}$	Time after sensor switches back to application mode if an invalid/ no host frame is detected	3	230	256	282	ms	
t_{s_bbit}	Sensor Biphase bit time	3	820	1024	1225	µs	
t_{s_bon}	Time till the sensor switches the biphase transceiver on	3	–	–	0.25	t_{s_bbit}	
t_{s_boff}	Time till the sensor switches the biphase transceiver off	3	–	–	50	µs	
t_{s_rise}	Sensor rise time of the Biphase protocol	3	–	0.4	–	µs	I_{OUT} = 5 mA C_L = 1 nF
t_{s_fall}	Sensor fall time of the Biphase protocol	3	–	0.5	–	µs	I_{OUT} = 5 mA C_L = 1 nF
Timing tolerances given are cumulative, i.e. each timing parameter does not vary independently from the other.							

Table 2–2: Biphase telegram parameters, continued

Symbol	Parameter	Pin No.	Limit Values			Unit	Comment
			Min.	Typ.	Max.		
V_{S_OUTL}	Sensor OUT Pin voltage for low level during programming	3	–	–	1	V	I_{OUT} = 5 mA C_L = 1 nF
V_{S_OUTH}	Sensor OUT Pin voltage for high level during programming	3	4	–	–	V	I_{OUT} = 5 mA C_L = 1 nF
Programming (Detail B and Detail D)							
t_{PROG}	Programming time	3	1.57	1.75	1.93	ms	
Timing tolerances given are cumulative, i.e. each timing parameter does not vary independently from the other.							

3. Available Sensor Commands

The sensor supports three commands which provide read and write access to the whole memory (EEPROM, NVRAM and RAM registers).

Each write data frame and read data frame contains 5 address bits only. The set base address command expands the address range to 8 bits.

In case of an unknown command, the sensor does neither transmit an acknowledge nor a body. (Each message consists of two parts: the message header, which contains information about the message body so that the recipient can interpret the message correctly, and the message body, which finally contains the payload.)

Table 3–1: Available sensor commands

Command	COMMAND [2:0]	frame type	ADDRESS[4:0]	DATA[15:0] (RD/WD)
read	1	read	offset address (0 to 31)	data read from address = ADDRESS
set base address	3	write	do not care	base address 0, 1, 2, 3
write	6	write	offset address (0 to 31)	data which is written to address = ADDRESS

3.1. Acknowledge Check

The logic used to detect the occurrence of ACK1 and ACK2 is described in Fig. 3–1.

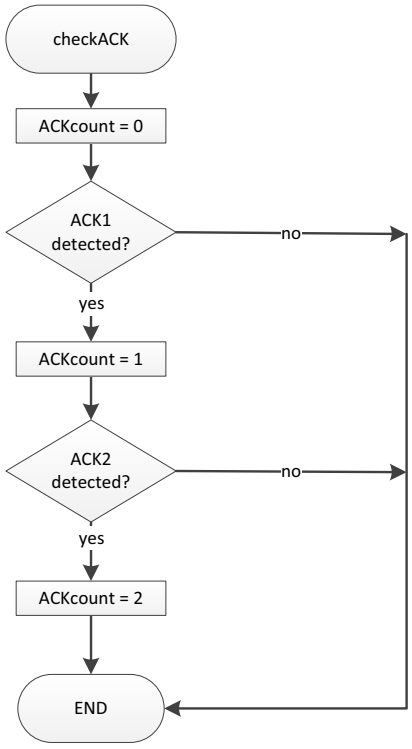

Fig. 3–1: Flowchart checkACK

3.2. Set Base Address

The set base address telegram uses the write data frame and functions as preparation for a following write and/or read command. The bits ADDRESS[4:0] and bits DATA[15:2] are 0. The bits DATA[1:0] contain the base address. The sensor transmits ACK1 if the set base address command was received correctly and the CRC matches.

An exemplary flowchart for the set base address command is given in Fig. 3–2.

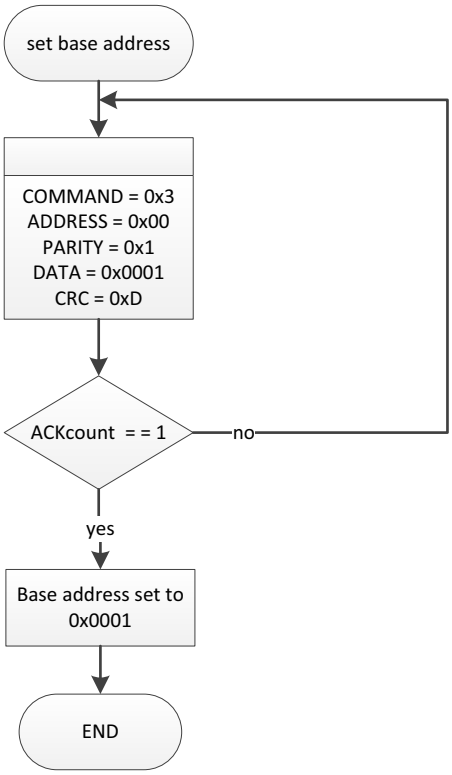

Fig. 3–2: Flowchart - set base address to 0x0001

3.3. Read

The read telegram uses the read data frame. The sensor transmits the data of the effective address after the header has been successfully received, the parity has been checked, and the effective address is permitted. Otherwise, the sensor does not respond.

The effective address is calculated based on the base address plus the offset address. The offset address is defined by the bits ADDRESS[4:0] of the header.

An exemplary flowchart for the read command is given in Fig. 3–3.

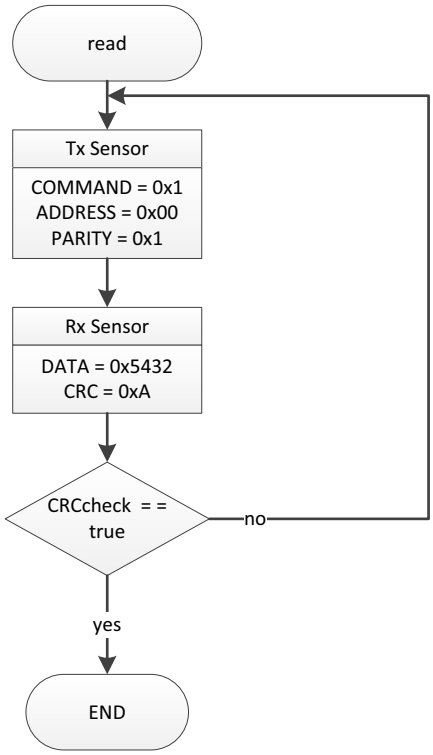

Fig. 3–3: Flowchart - read from offset address 0x0

3.4. Write (EEPROM Address)

The write EEPROM telegram uses the write data frame. The sensor saves the received address to the calculated effective address and transmits an acknowledge (ACK1) after the header and the body have been successfully received and the effective address is permitted. The sensor transmits an additional acknowledge (ACK2) after DATA is successfully programmed. Otherwise, the command is discarded and the sensor transmits no acknowledge at all.

A write telegram is also discarded:

– during EEPROM programming.

– during the NVRAM programming sequence.

An exemplary flowchart for the write command is given in Fig. 3–4.

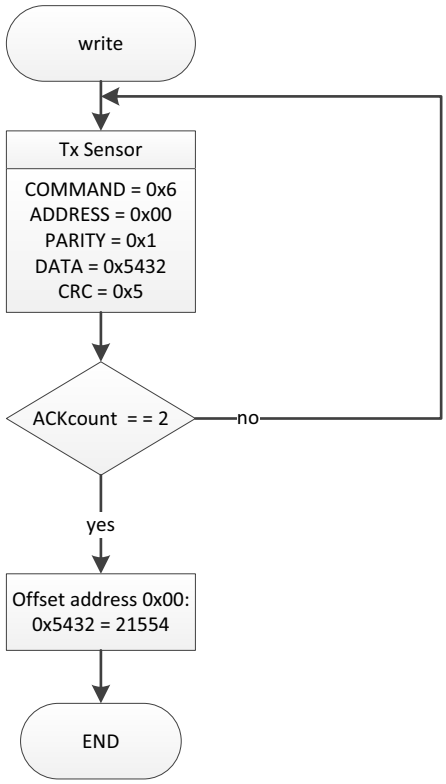

Fig. 3–4: Flowchart - write 0x5432 to offset address 0x0

Write EEPROM after Power On

After switching on the supply voltage and after a failed programming it is mandatory to reset the diagnostic registers (PROG_DIAGNOSIS and DIAGNOSIS, see Table 5–1). This is done by setting the base address to 3 and writing 0 into address 11 and 12.

Note: To ensure that the host does not misinterpret the PWM duty cycle of the HAL/HAR 2455 as an acknowledge, it is mandatory to set CLAMP-HIGH to 0% during programming. Additionally, the Diagnosis Latch bit (see Table 5–4) shall be set during end of line testing. Without this precaution programming errors will not be indicated by the second acknowledge.

To enable debugging, it is recommended to read back the diagnostic registers (PROG_DIAGNOSIS and DIAGNOSIS, see Table 5–1) in case of a missing second acknowledge.

3.5. Write (NVRAM Address)

The write NVRAM telegram uses the write data frame. This chapter describes the sequence used to program the NVRAM registers of the device.

A flowchart of the write NVRAM sequence is given in Fig. 3–5.

A detailed flowchart of the write NVRAM sequence, showing the programming of the Customer Setup register, is given in Fig. 3–6.

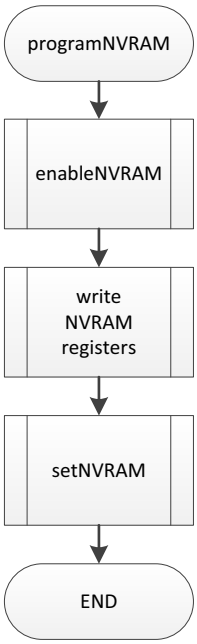

Fig. 3–5: Flowchart - write NVRAM sequence

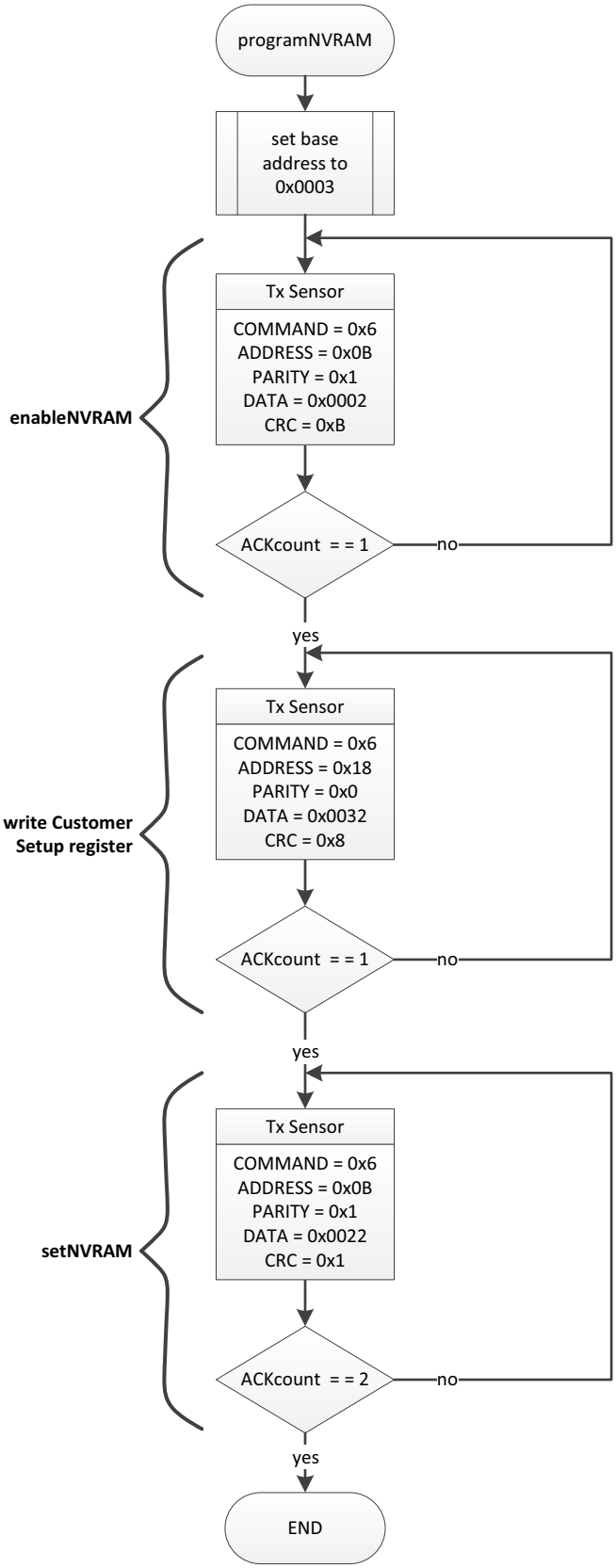

Fig. 3–6: Flowchart - write NVRAM sequence, example Customer Setup register

3.5.1. enableNVRAM

The first action when programming the NVRAM is to enable the write access to the RAM layer by disabling the hardware outputs (PROG_DIAGNOSIS[0]: NVRAM Layer = 0) and latching the current NVRAM bits (PROG_DIAGNOSIS[1]: LATCH = 1) (see Table 5–2).

The sections of the NVRAM are now ready for writing new values to the RAM layer.

An exemplary flowchart to enable the NVRAM is given in Fig. 3–7.

3.5.2. setNVRAM

After writing the new NVRAM register value the NVRAM content has to be stored permanently by starting the automatic erase and program of the NVRAM (PROG_DIAGNOSIS[5]: PROG-ERASE = 1) and latching the new NVRAM bits (PROG_DIAGNOSIS[1]: LATCH = 1) (see Table 5–2).

An exemplary flowchart to set the NVRAM is given in Fig. 3–7.

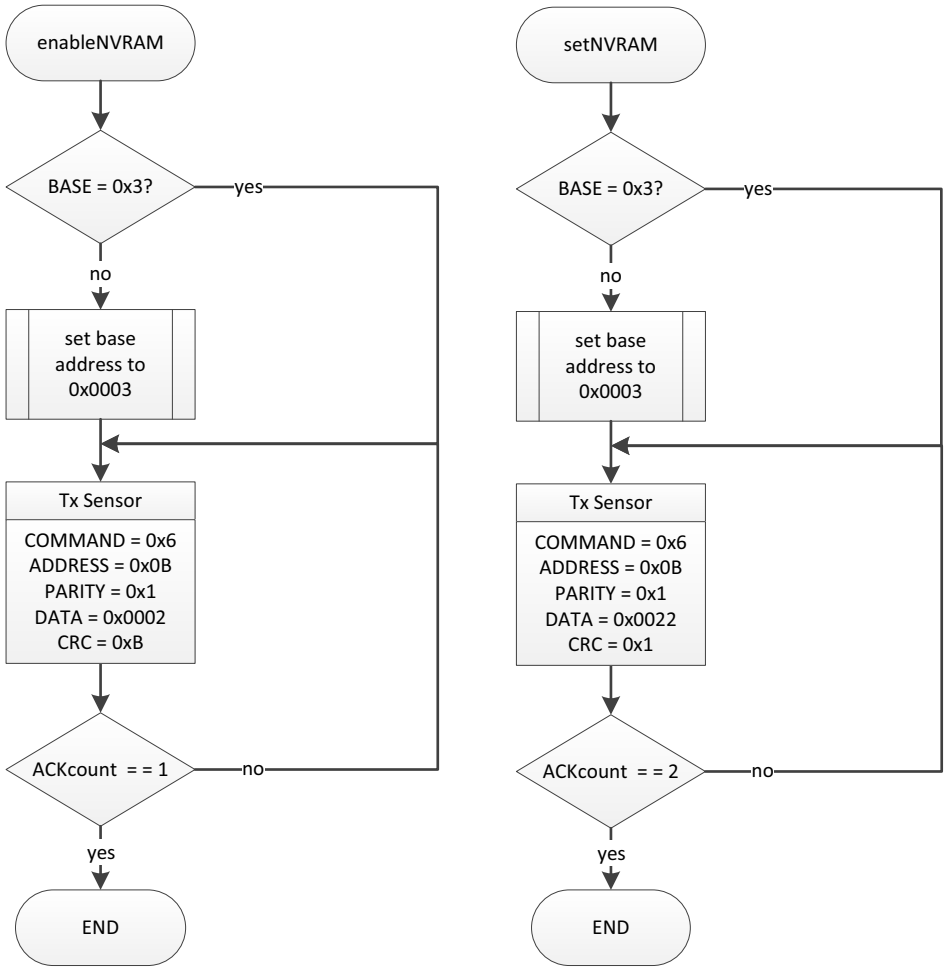

Fig. 3–7: Flowchart - enableNVRAM and setNVRAM

3.6. Parity Calculation

For the command and address bits an odd parity check is used:

– In case of an even number of ones, the parity bit has to be 1.

– In case of an odd number of ones, the parity bit has to be 0.

A flowchart for the PARITY determination is given in Fig. 3–8.

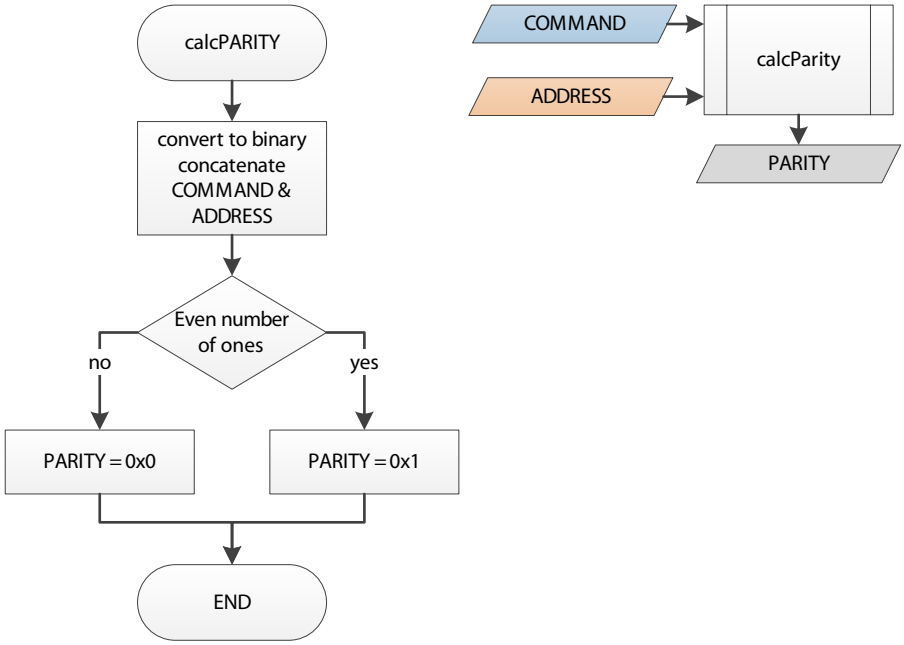

Fig. 3–8: Flowchart - calcPARITY

3.7. CRC Calculation

The DATA bits are always followed by 4 CRC bits. For all commands except read, the CRC is calculated of all protocol bits, including COMMAND, ADDRESS, PARITY, dummy bit, and DATA bits.

For the read command, the CRC is calculated from DATA bits only.

The polynomial for the CRC calculation is always $\mathbf{X^4 + X + 1}$. (With a seed value of 0.)

In case of a correct command detection (PARITY, CRC, and ADDRESS, if applicable), the senor responds with an acknowledge (ACK1).

An example of the CRC calculation is shown in Table 3–2.

Table 3–2: CRC calculation

```
const unsigned char CRC_POLY = 0x13; // x^4 + x + 1
int crc (int data, int size)
{
     int i;
     unsigned char crc = 0x00;
     for (i=0; i<size; i++)
     {
          if ((crc<<3 & 0x1) != (data >> (size - 1 - i) & 1))
          {
               crc = crc<<1;
               crc ^= CRC_POLY;
               crc &= 0xF;
          }
          else
               crc <<= 1;
     }
     return crc = crc&0xF;
}
```

3.8. Protocol Error Handling

The sensor detects the following protocol and command errors and transmits in these cases neither a body nor an acknowledge:

– invalid PARITY / invalid CRC

– unknown command

– command execution failed

4. Locking the Sensor

For reliability in service, it is mandatory to set the LOCK bit after final adjustment and programming.

The successful setting of the LOCK bit shall be checked, e.g. by reading back the LOCK bit after programming, but before a power-on reset.

To verify that the programming of the sensor was successful it is mandatory to check the acknowledges of the sensor or to read/check the status of the PROG_DIAGNOSIS register (see Table 5–2) after each store sequence.

Electro-static discharges (ESD) may disturb the supply voltage during programming. Please take precautions against ESD.

Note: It is not possible to write or to read a register after locking. The locked sensor will not respond.

5. Memory Table

The following table gives an overview of the internal memory of the HAL/HAR 24xy, consisting of programmable EEPROM and NVRAM registers and readable RAM registers.

Note: The EEPROM and NVRAM registers can be safely programmed up to 100 times.

Table 5–1: HAL/HAR 24xy Memory Table

Bank	Address	Name	Type	Explanation	Memory Type
0	0	CUST_ID1	Read/Write	Customer ID 1 (free programmable value) Range: 0x0000... 0xFFFF	EEPROM
0	1	CUST_ID2	Read/Write	Customer ID 2 (free programmable value) Range: 0x0000... 0xFFFF	EEPROM
0	2	TCCO0	Read/Write	Offset temperature compensation: offset Range: 0x8000... 0x7FFF (two's complement)	EEPROM
0	3	TCCO1	Read/Write	Offset temperature compensation: linear factor Range: 0x8000... 0x7FFF (two's complement)	EEPROM
0	4	TCCG0	Read/Write	Sensitivity temperature compensation: offset Range: 0x8000... 0x7FFF (two's complement)	EEPROM
0	5	TCCG1	Read/Write	Sensitivity temperature compensation: linear factor Range: 0x8000... 0x7FFF (two's complement)	EEPROM
0	6	TCCG2	Read/Write	Sensitivity temperature compensation: quadratic factor Range: 0x8000... 0x7FFF (two's complement)	EEPROM
0	7	–	Read	Reserved and locked to 0	EEPROM
0	8	–	Read	Reserved and locked to 16384	EEPROM
0	9	SCALE_GAIN	Read/Write	Sensitivity scaling before setpoint linearization block Range: 0x8000... 0x7FFF (two's complement)	EEPROM
0	10	SCALE_OFFSET	Read/Write	Offset scaling before setpoint linearization block Range: 0x8000... 0x7FFF (two's complement)	EEPROM
0	11	OUT_GAIN	Read/Write	Sensitivity scaling of digital output Range: 0x8000... 0x7FFF (two's complement)	EEPROM
0	12	OUT_OFFSET	Read/Write	Offset scaling of digital output Range: 0x8000... 0x7FFF (two's complement)	EEPROM
0	13	OUT_CMPHI	Read/Write	Clamp-High of digital output Range: 0x8000... 0x7FFF (two's complement)	EEPROM
0	14	OUT_CMPLO	Read/Write	Clamp-Low of digital output Range: 0x8000... 0x7FFF (two's complement)	EEPROM
0	15	LP_FILTER	Read/Write	Low Pass Filter Setting (only for HAL 2421) 0: Filter off (default) 1...32767: Filter on	EEPROM
0	18	MIC_ID1	Read	Micronas Identification number 1 Range: 0x8000... 0x7FFF (two's complement)	EEPROM

Table 5–1: HAL/HAR 24xy Memory Table, continued

Bank	Address	Name	Type	Explanation	Memory Type
0	19	MIC_ID2	Read	Micronas Identification number 2 Range: 0x8000... 0x7FFF (two's complement)	EEPROM
1	0	TEMP_ADJ	Read	Adjusted Temperature Value Range: 0x8000... 0x7FFF (two's complement)	RAM
1	5	MIC_COMP	Read	Micronas temperature compensated magnetic-field value Range: 0x8000... 000 (two's complement)	RAM
1	6	CUST_COMP	Read	Customer compensated magnetic-field value Range: 0x8000... 0x7FFF (two's complement)	RAM
1	8	SETPT_OUT	Read	Magnetic-field value after setpoint linearization block Range: 0x8000... 0x7FFF (two's complement)	RAM
1	9	DIG_OUT	Read	Digital output value after output gain and offset scaling Range: 0x8000... 0x7FFF (two's complement)	RAM
2	0	SP0	Read/Write	Setpoint for non-linear characteristic (only available for 24x5) Range: 0x8000... 0x7FFF (two's complement)	EEPROM
2	1	SP1	Read/Write	Setpoint for non-linear characteristic (only available for 24x5) Range: 0x8000... 0x7FFF (two's complement)	EEPROM
2	2	SP2	Read/Write	Setpoint for non-linear characteristic (only available for 24x5) Range: 0x8000... 0x7FFF (two's complement)	EEPROM
2	3	SP3	Read/Write	Setpoint for non-linear characteristic (only available for 24x5) Range: 0x8000... 0x7FFF (two's complement)	EEPROM
2	4	SP4	Read/Write	Setpoint for non-linear characteristic (only available for 24x5) Range: 0x8000... 0x7FFF (two's complement)	EEPROM
2	5	SP5	Read/Write	Setpoint for non-linear characteristic (only available for 24x5) Range: 0x8000... 0x7FFF (two's complement)	EEPROM
2	6	SP6	Read/Write	Setpoint for non-linear characteristic (only available for 24x5) Range: 0x8000... 0x7FFF (two's complement)	EEPROM
2	7	SP7	Read/Write	Setpoint for non-linear characteristic (only available for 24x5) Range: 0x8000... 0x7FFF (two's complement)	EEPROM
2	8	SP8	Read/Write	Setpoint for non-linear characteristic (only available for 24x5) Range: 0x8000... 0x7FFF (two's complement)	EEPROM
2	9	SP9	Read/Write	Setpoint for non-linear characteristic (only available for 24x5) Range: 0x8000... 0x7FFF (two's complement)	EEPROM
2	10	SP10	Read/Write	Setpoint for non-linear characteristic (only available for 24x5) Range: 0x8000... 0x7FFF (two's complement)	EEPROM
2	11	SP11	Read/Write	Setpoint for non-linear characteristic (only available for 24x5) Range: 0x8000... 0x7FFF (two's complement)	EEPROM
2	12	SP12	Read/Write	Setpoint for non-linear characteristic (only available for 24x5) Range: 0x8000... 0x7FFF (two's complement)	EEPROM
2	13	SP13	Read/Write	Setpoint for non-linear characteristic (only available for 24x5) Range: 0x8000... 0x7FFF (two's complement)	EEPROM
2	14	SP14	Read/Write	Setpoint for non-linear characteristic (only available for 24x5) Range: 0x8000... 0x7FFF (two's complement)	EEPROM

Table 5–1: HAL/HAR 24xy Memory Table, continued

Bank	Address	Name	Type	Explanation	Memory Type
2	15	SP15	Read/Write	Setpoint for non-linear characteristic (only available for 24x5) Range: 0x8000... 0x7FFF (two's complement)	EEPROM
3	0	TEMP	Read	Raw Temperature value Range: 0x8000... 0x7FFF (two's complement)	RAM
3	1	CFX	Read	Uncompensated magnetic-field value Range: 0x8000... 0x7FFF (two's complement)	RAM
3	7	DAC_IN	Read	Input value for D/A converter / output for digital versions Range: 0x0000... 0x7FFF	RAM
3	11	PROG_DIAGNOSIS	Read/Write	NVRAM programming (see Table 5–2) Range: 0x8000... 0x7FFF	NVRAM
3	12	DIAGNOSIS	Read/Write	Diagnosis register (fault-modes) (see Table 5–3) Range: 0x8000... 0x7FFF	NVRAM
3	24	CUST_SETUP	Read/Write	Customer Setup register (see Table 5–4) Range: 0x8000... 0x7FFF (two's complement)	NVRAM

Table 5–2: PROG_DIAGNOSIS register

Bit	Name	Type	Description
15:11	–	–	Reserved (do not care)
10	Charge Pump Error	Read/Write	This bit is set to 1 in case that the internal programming voltage was too low.
9	Voltage Error during Program/ Erase	Read/Write	This bit is set to 1 in case that the internal supply voltage was too low during program or erase.
8	NVRAM Error	Read/Write	This bit is set to 1 in case that the programming of the NVRAM failed.
7:6	–	–	Reserved (must be set to 0)
5	PROG-ERASE	Write	Erase and program of NVRAM 0: idle 1: start erase and program
4:2	–	–	Reserved (must be set to 0)
1	LATCH	Read/Write	Latch hardware outputs[1)] 0: latching of customer setup bits disabled 1: latching of customer setup bits enabled The affected bits in the customer setup register are labeled with latched.
0	NVRAM Layer	Read/Write	NVRAM layer 0: enable RAM layer 1: disable RAM layer

Table 5–3: DIAGNOSIS register

Bit	Name	Type	Description
15:6	–	–	Reserved (do not care)
5	DSP Self Test	Read/Write	This bit is set to 1 in case of the self test of the DSP fails. (Continuously running) Write 0: clear selftest error-flag
4	EEPROM Self Test	Read/Write	This bit is set to 1 in case of the EEPROM self test fails. (Performed during power-up and after every write to the EEPROM) Write 0: clear selftest error-flag
3	ROM Check	Read/Write	This bit is set to 1 in case of ROM parity check fails. (continuously running) Write 0: clear parity error-flag
2	Adder Overflow	Read/Write	This bit is set to 1 in case of an overflow occurs during calculation Write 0: clear selftest error-flag
1:0	–	–	Reserved (do not care)

Table 5–4: CUST_SETUP register

Bit	Name	Type	Description
15	Interpolator	Read/Write	Analog output interpolator (only available for HAL 2421) 0: Disabled (default) 1: Enabled
14:12	Barrel Shifter	Read/Write	Magnetic range: 000: ±400 mT 001: ±200 mT 010: ±100 mT (default) 011: ±50 mT 100: ±25 mT 101: ±12,5 mT 110: ±6,25 mT
11:10	PWM Frequency	Read/Write	Selection of PWM frequency (for HAL/HAR 2455) 00: 1 kHz, 500 Hz in failure mode (default) 01: 500 Hz, 250 Hz in failure mode 10: 250 Hz, 125 Hz in failure mode 11: 2 kHz (11-bit resolution), 1 kHz in failure mode
9:8	Output Short Detection	Read/Write	Overcurrent detection on output pin (latched)[1)] 00: Disabled 01: OUT = V_{SUP} in error case (default for HAL/HAR 2420, 2425, 2455) 10: OUT = GND in error case 11: OUT = Tristate in error case (default for HAL 2421) Tristate as long as Lock bit not set, or communication via OUT is enabled
7	Error Band	Read/Write	Error Band definition for locked devices (for HAL/ HAR 242x) 0: High Error Band (OUT = V_{SUP}, default) 1: Low Error Band (OUT = GND) High as long as lock bit not set Polarity of the PWM signal (for HAL/ HAR 2455) 0: PWM period starts with high pulse (default) 1: PWM period starts with low pulse

Table 5–4: CUST_SETUP register, continued

Bit	Name	Type	Description
6	Burn-In Mode	Read/ Write	Triangular output voltage (latched)[1)] 0: Disabled (default) 1: Enabled
5	Functionality Mode	Read/Write	Supply voltage supervision 0: Extended: undervoltage (POR) 3.8V, overvoltage 9V 1: Normal: undervoltage (POR) 4.2V, overvoltage 6V (default)
4	Communication Mode (POUT)	Read/Write	Communication via output pin (latched)[1)] 0: Disabled 1: Enabled (default)
3	Overvoltage Detection	Read/Write	Internal overvoltage detection (latched)[1)] 0: Enabled (default) 1: Disabled
2	Diagnosis Latch	Read/Write	Latching of diagnosis bits (latched)[1)] 0: No latching (default) 1: Latched till next Power-On Reset (POR)
1	Diagnosis	Read/Write	Error visibility on output according to selected Error Band (Bit 7) 0: Diagnosis errors force output to Error Band. 1: Diagnosis errors do not force output to Error Band (default).
0	Lock	Read/Write	Lock of Customer Setup register (latched)[1)] 0: not locked (default) 1: locked

[1)] Latched means that the bit is not immediately activated after programming. The next power-on reset of the sensor activates the bit. This allows e.g. reading of the registers after programming the customer lock bit.

6. Application Note History

1. HAL/HAR 24xy Programming Guide, Dec. 8, 2016; APN000115_001EN. First release of the application note.
2. HAL/HAR 24xy Programming Guide, July 1, 2019; APN000115_002EN. Second release of the application note.

Major Changes:

– Section 1 “General Information” updated
– Section 2.2 ”Data Link and Transport Layer” updated
– Section 2.3 ”Telegram parameters” updated
– Section 3 “Available Sensor Commands” updated
– Section 5 “Memory Table” updated

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