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MOSFET - Power, N-Channel, SUPERFET[®] III, FAST

650 V, 250 mΩ, 13 A

NTD250N65S3H

Description

SUPERFET III MOSFET is ON Semiconductor's brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provides superior switching performance, and withstand extreme dv/dt rate.

Consequently, SUPERFET III FAST MOSFET series helps minimize various power systems and improve system efficiency.

Features

- 700 V @ $T_J = 150^\circ\text{C}$
- Typ. $R_{DS(on)} = 201\text{ m}\Omega$
- Ultra Low Gate Charge (Typ. $Q_g = 24\text{ nC}$)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)} = 229\text{ pF}$)
- 100% Avalanche Tested
- These Devices are Pb-Free and are RoHS Compliant

Applications

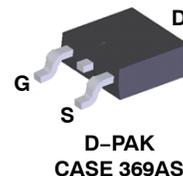
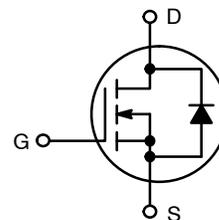
- Computing / Display Power Supplies
- Telecom / Server Power Supplies
- Industrial Power Supplies
- Lighting / Charger / Adapter



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V_{DSS}	$R_{DS(on)}\text{ MAX}$	$I_D\text{ MAX}$
650 V	250 mΩ @ 10 V	13 A



MARKING DIAGRAM



T250N65S3H = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
ZZ = Lot Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

NTD250N65S3H

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, Unless otherwise specified)

Symbol	Parameter	Value	Unit
V _{DSS}	Drain to Source Voltage	650	V
V _{GSS}	Gate to Source Voltage	DC	±30
		AC (f > 1 Hz)	±30
I _D	Drain Current	Continuous (T _C = 25°C)	13
		Continuous (T _C = 100°C)	8
I _{DM}	Drain Current	Pulsed (Note 1)	36
E _{AS}	Single Pulsed Avalanche Energy (Note 2)	108	mJ
I _{AS}	Avalanche Current (Note 2)	2.9	A
E _{AR}	Repetitive Avalanche Energy (Note 1)	1.06	mJ
dv/dt	MOSFET dv/dt	120	V/ns
	Peak Diode Recovery dv/dt (Note 3)	20	
P _D	Power Dissipation	(T _C = 25°C)	106
		Derate Above 25°C	0.85
T _J , T _{STG}	Operating and Storage Temperature Range	-55 to +150	°C
T _L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 s	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. I_{AS} = 2.9 A, R_G = 25 Ω, starting T_J = 25°C.
3. I_{SD} ≤ 6.5 A, di/dt ≤ 200 A/μs, V_{DD} ≤ 400 V, starting T_J = 25°C.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
R _{θJC}	Thermal Resistance, Junction to Case, Max.	1.18	°C/W
R _{θJA}	Thermal Resistance, Junction to Ambient, Max. (Note 4)	40	

4. Device on 1 in² pad 2 oz copper pad on 1.5 x 1.5 in. board of FR-4 material.

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Reel Size	Tape Width	Shipping†
NTD250N65S3H	T250N65S3H	D-PAK	330 mm	16 mm	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV _{DSS}	Drain to Source Breakdown Voltage	V _{GS} = 0 V, I _D = 1 mA, T _J = 25°C	650			V
		V _{GS} = 0 V, I _D = 1 mA, T _J = 150°C	700			V
ΔBV _{DSS} /ΔT _J	Breakdown Voltage Temperature Coefficient	I _D = 10 mA, Referenced to 25°C		0.63		V/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 650 V, V _{GS} = 0 V			3	μA
		V _{DS} = 520 V, T _C = 125°C		0.7		
I _{GSS}	Gate to Body Leakage Current	V _{GS} = ±30 V, V _{DS} = 0 V			±100	nA

ON CHARACTERISTICS

V _{GS(th)}	Gate Threshold Voltage	V _{GS} = V _{DS} , I _D = 1.1 mA	2.4		4.0	V
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 6.5 A		201	250	mΩ
g _{FS}	Forward Transconductance	V _{DS} = 20 V, I _D = 6.5 A		14		S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V _{DS} = 400 V, V _{GS} = 0 V, f = 250 kHz		1261		pF
C _{oss}	Output Capacitance			19		pF
C _{oss(eff.)}	Effective Output Capacitance	V _{DS} = 0 V to 400 V, V _{GS} = 0 V		229		pF
C _{oss(er.)}	Energy Related Output Capacitance	V _{DS} = 0 V to 400 V, V _{GS} = 0 V		33		pF
Q _{g(tot)}	Total Gate Charge at 10 V	V _{DS} = 400 V, I _D = 6.5 A, V _{GS} = 10 V (Note 5)		24		nC
Q _{gs}	Gate to Source Gate Charge			5.9		nC
Q _{gd}	Gate to Drain "Miller" Charge			6.8		nC
ESR	Equivalent Series Resistance	f = 1 MHz		0.9		Ω

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	V _{DD} = 400 V, I _D = 6.5 A, V _{GS} = 10 V, R _g = 12 Ω (Note 5)		18		ns
t _r	Turn-On Rise Time			8.2		ns
t _{d(off)}	Turn-Off Delay Time			54		ns
t _f	Turn-Off Fall Time			4.2		ns

SOURCE-DRAIN DIODE CHARACTERISTICS

I _S	Maximum Continuous Source to Drain Diode Forward Current			13		A
I _{SM}	Maximum Pulsed Source to Drain Diode Forward Current			36		A
V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 6.5 A			1.2	V
t _{rr}	Reverse Recovery Time	V _{DD} = 400 V, I _{SD} = 6.5 A, dI _F /dt = 100 A/μs		233		ns
Q _{rr}	Reverse Recovery Charge			2.5		μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Essentially independent of operating temperature typical characteristics.

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TYPICAL CHARACTERISTICS

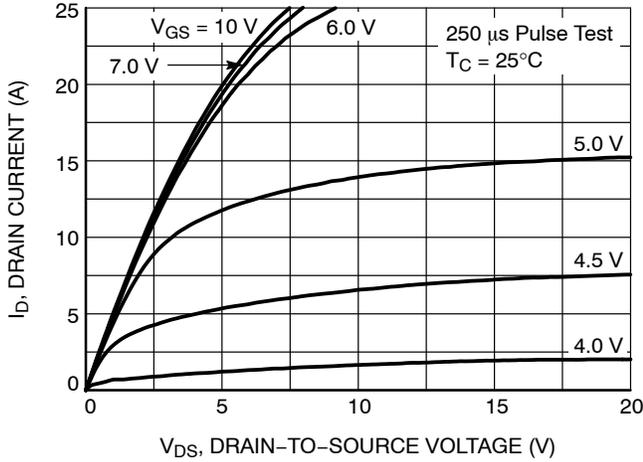


Figure 1. On-Region Characteristics

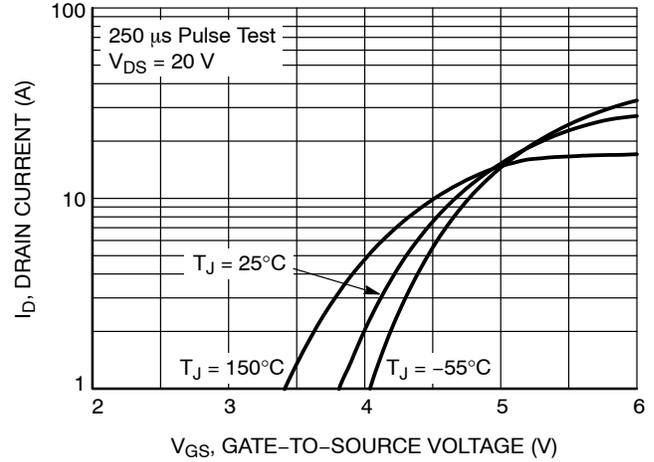


Figure 2. Transfer Characteristics

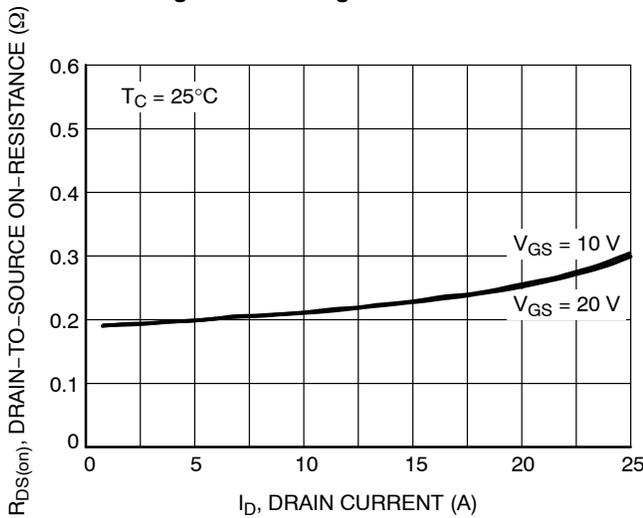


Figure 3. On Resistance Variation vs. Drain Current and Gate Voltage

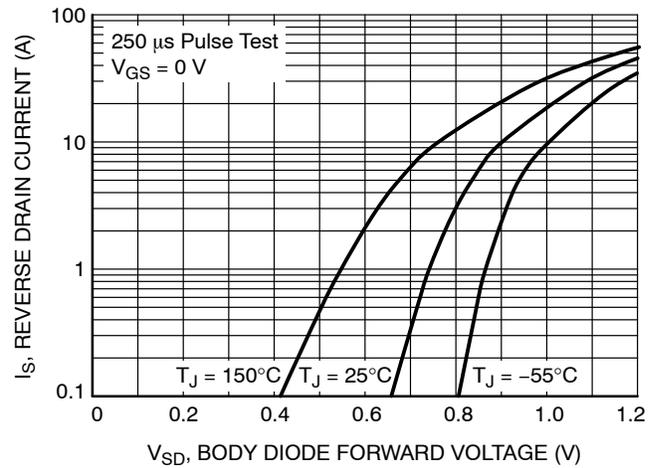


Figure 4. Diode Forward Voltage Variation vs. Source Current and Temperature

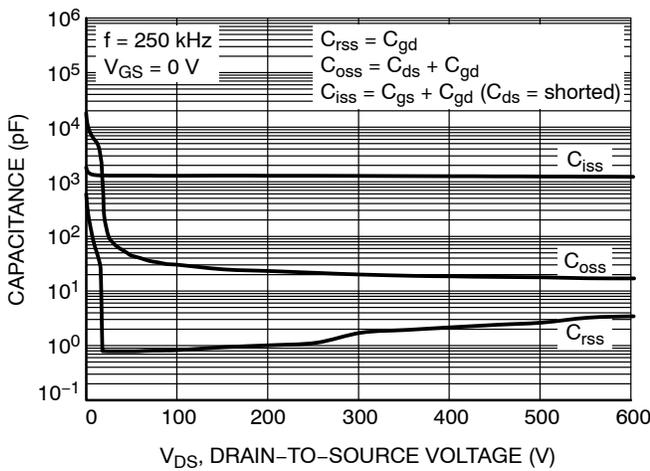


Figure 5. Capacitance Characteristics

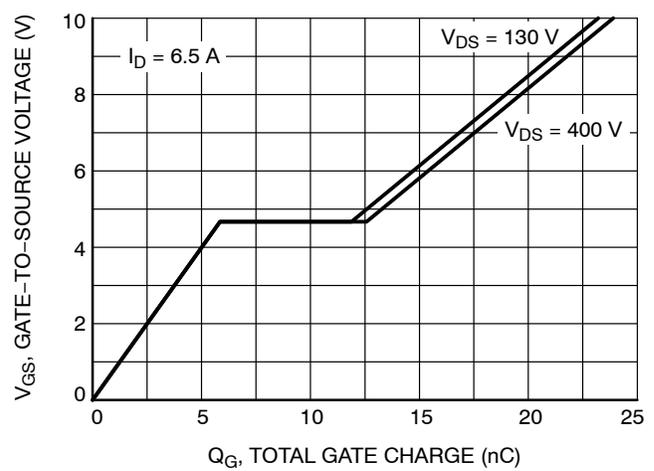


Figure 6. Gate Charge Characteristics

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TYPICAL CHARACTERISTICS

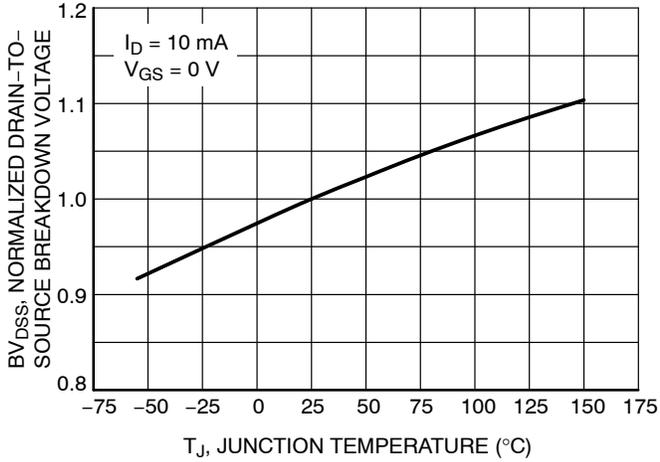


Figure 7. Breakdown Voltage Variation vs. Temperature

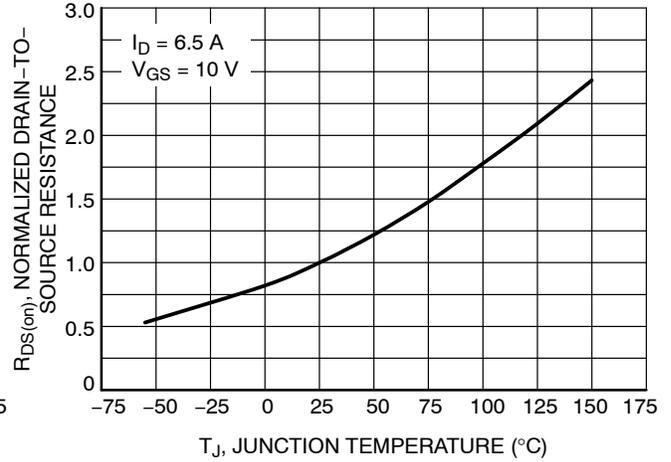


Figure 8. On-Resistance Variation vs. Temperature

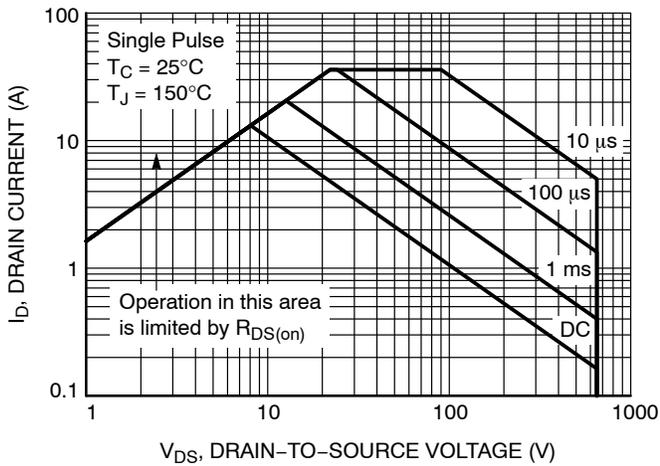


Figure 9. Maximum Safe Operating Area

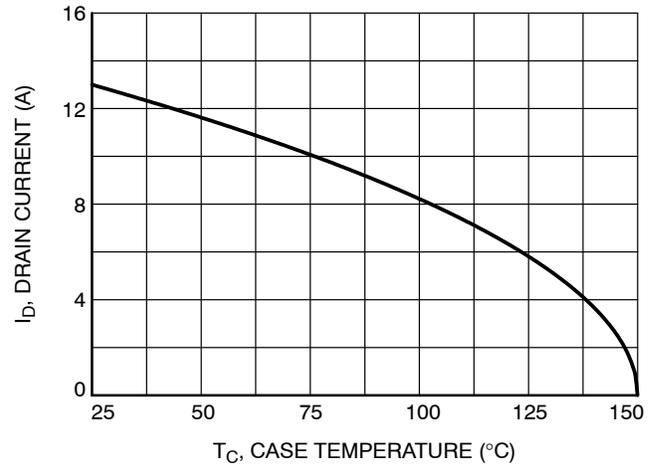


Figure 10. Maximum Drain Current vs. Case Temperature

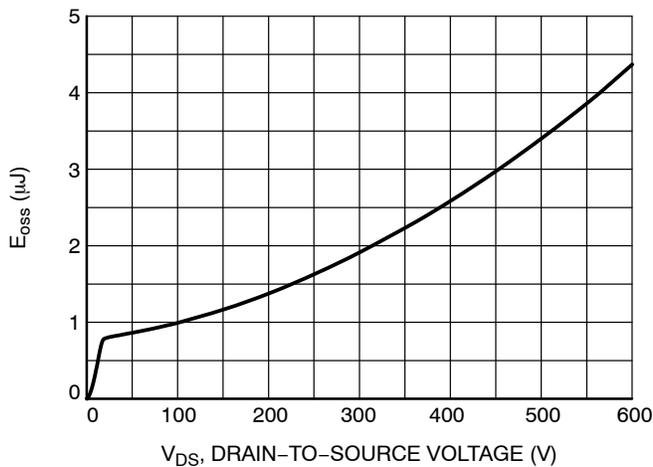


Figure 11. E_{oss} vs. Drain-to-Source Voltage

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TYPICAL CHARACTERISTICS

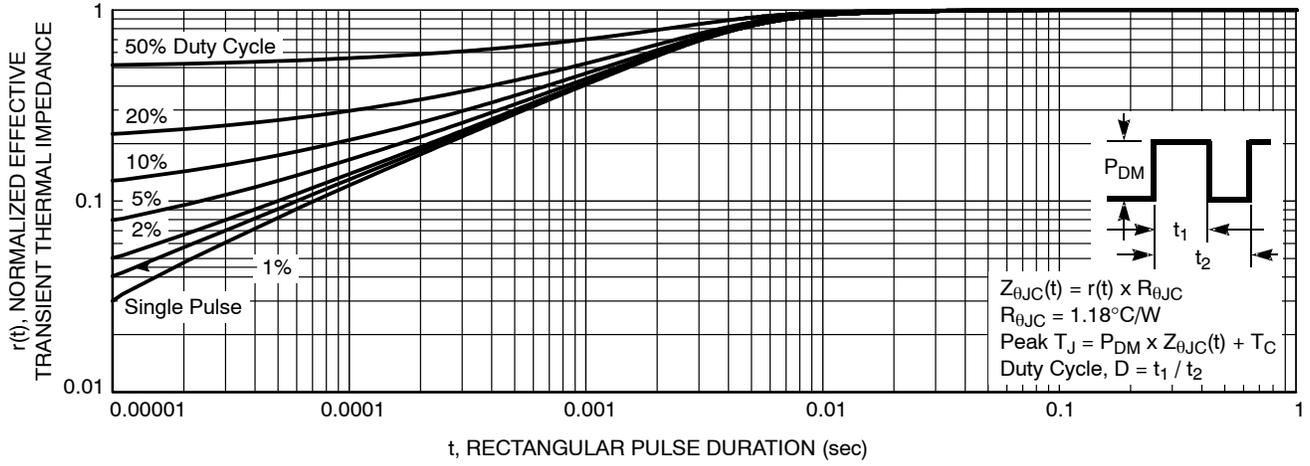


Figure 12. Transient Thermal Response Curve

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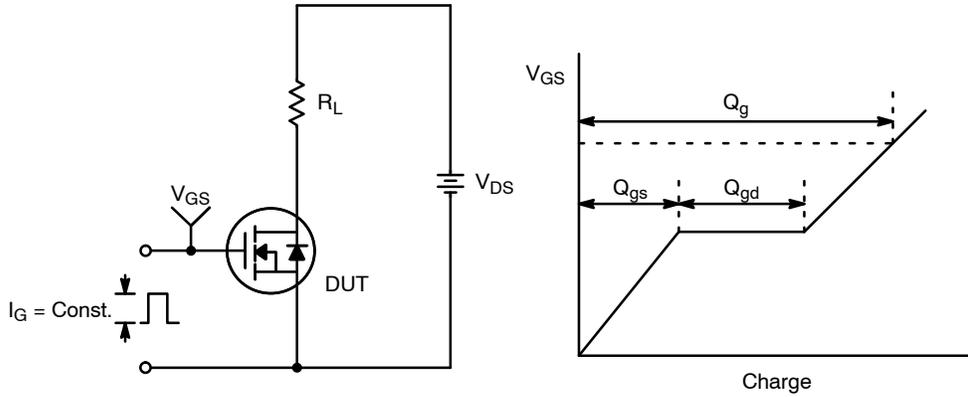


Figure 13. Gate Charge Test Circuit & Waveform

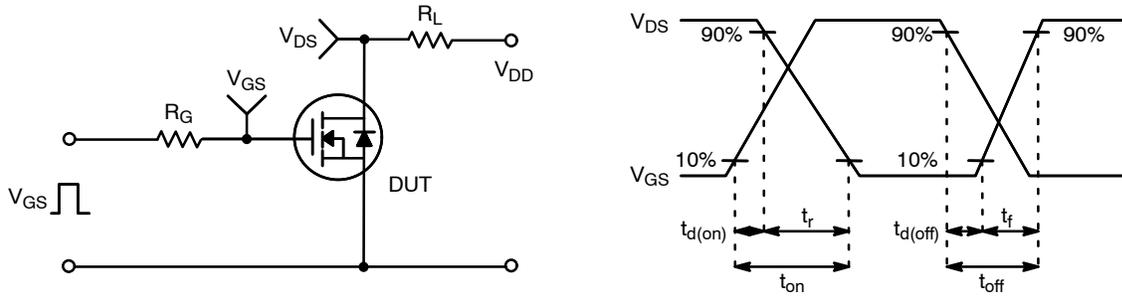


Figure 14. Resistive Switching Test Circuit & Waveforms

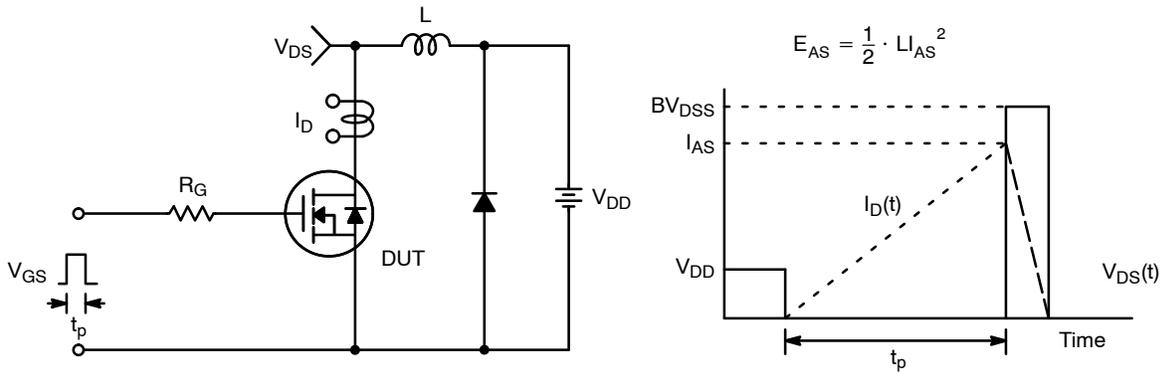


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

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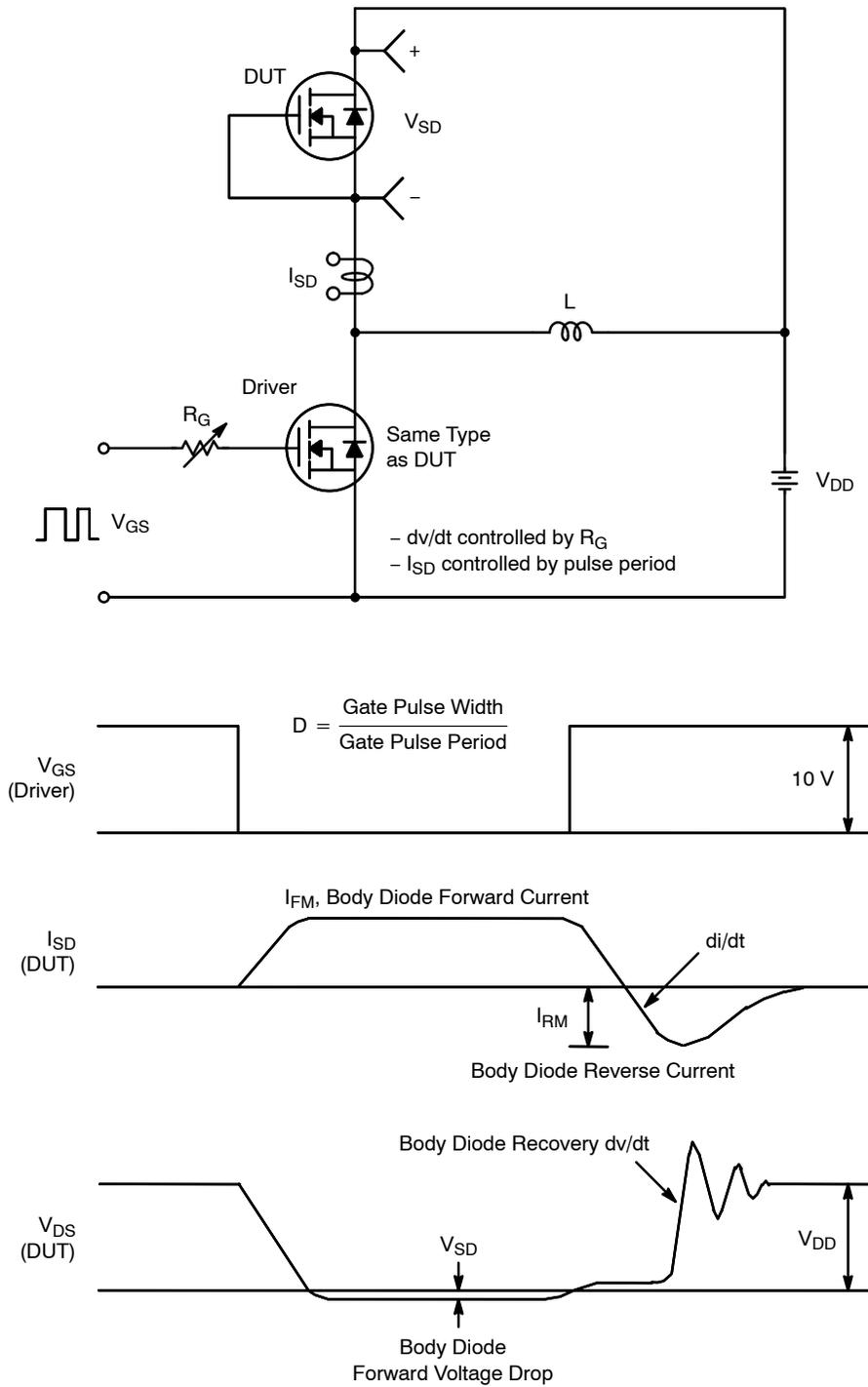
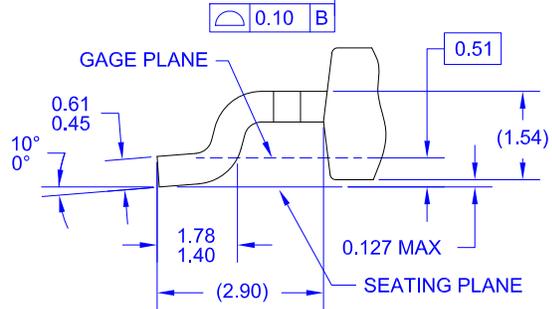
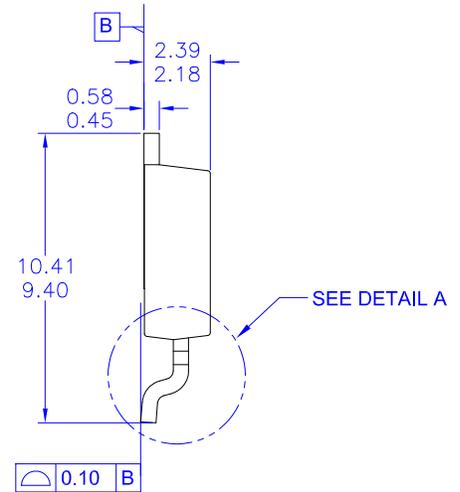
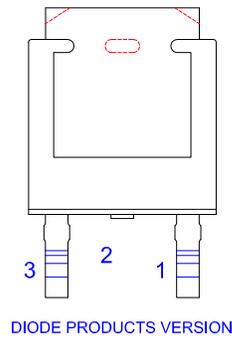
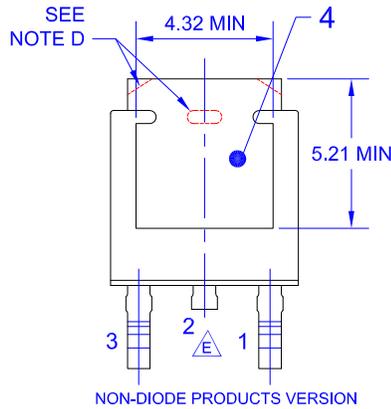
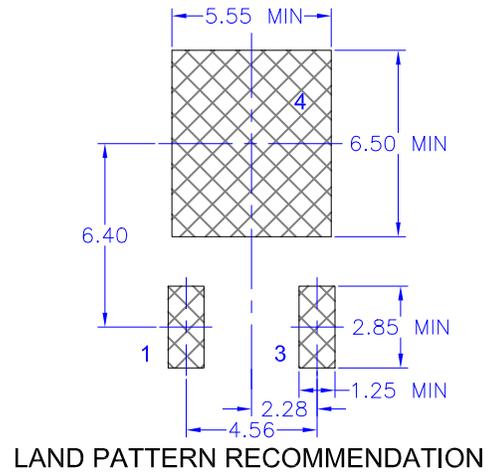
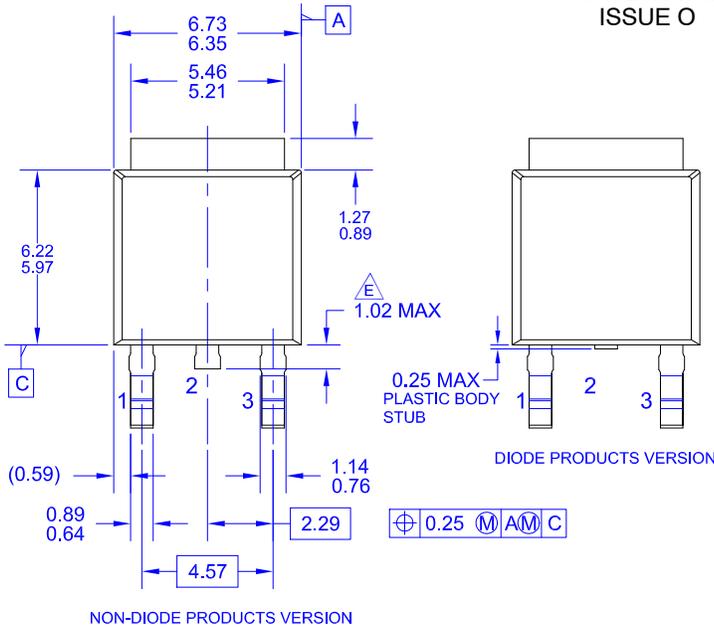


Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

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PACKAGE DIMENSIONS

DPAK3 (TO-252 3 LD) CASE 369AS ISSUE O



DETAIL A
(ROTATED -90°)
SCALE: 12X

NOTES: UNLESS OTHERWISE SPECIFIED

A) THIS PACKAGE CONFORMS TO JEDEC, TO-252, ISSUE C, VARIATION AA.

B) ALL DIMENSIONS ARE IN MILLIMETERS.

C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.

D) SUPPLIER DEPENDENT MOLD LOCKING HOLES OR CHAMFERED CORNERS OR EDGE PROTRUSION.

E) TRIMMED CENTER LEAD IS PRESENT ONLY FOR DIODE PRODUCTS

F) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR EXTRUSIONS.

G) LAND PATTERN RECOMMENDATION IS BASED ON IPC7351A STD TO228P991X239-3N.

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