

Product Summary

BV _{DSS}	BV _{DSS@} T _{J Max}	R _{DS(ON)} Max	I _D Max T _A = +25°C
115V	120V	65mΩ @ V _{GS} = 10V	4.3A
		70mΩ @ V _{GS} = 4.5V	4.5A

Description

This new generation MOSFET is designed to minimize the on-state resistance (R_{DS(ON)}) and yet maintain superior switching performance, making it ideal for high-efficiency power management applications.

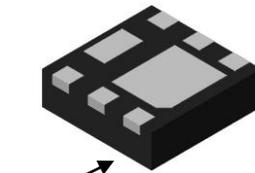
Applications

- DC-DC Primary Switch
- Load Switch

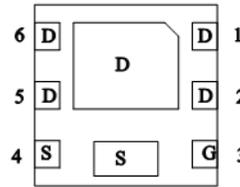
U-DFN2020-6 (Type F)



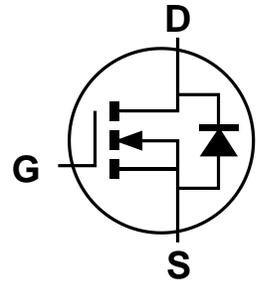
Top View



Bottom View



Pin Out
Bottom View



Equivalent Circuit

Features and Benefits

- 0.6mm Profile – Ideal for Low Profile Applications
- PCB Footprint of 4mm²
- Low On-Resistance
- 100% Unclamped Inductive Switching (UIS) Test in Production – Ensures More Reliable and Robust End Application
- Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)**
- Halogen and Antimony Free. “Green” Device (Note 3)**

Mechanical Data

- Case: U-DFN2020-6
- Case Material: Molded Plastic, “Green” Molding Compound. UL Flammability Classification Rating 94V-0
- Moisture Sensitivity: Level 1 per J-STD-020
- Terminals: Finish – NiPdAu over Copper Leadframe. Solderable per MIL-STD-202, Method 208 @4
- Weight: 0.0065 grams (Approximate)

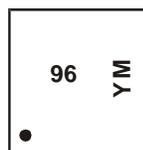
Ordering Information (Note 4)

Part Number	Case	Quantity Per Reel
DMT12H065LFDF-7	U-DFN2020-6 (Type F)	3,000
DMT12H065LFDF-13	U-DFN2020-6 (Type F)	10,000

- Notes:
- No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
 - See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 - Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
 - For packaging details, go to our website at <https://www.diodes.com/design/support/packaging/diodes-packaging/>.

Marking Information

U-DFN2020-6 (Type F)



96 = Product Type Marking Code
 YM = Date Code Marking
 Y = Year (ex: G = 2019)
 M = Month (ex: 9 = September)

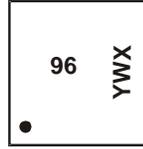
Date Code Key

Year	2019	2020	2021	2022	2023	2024	2025	2026	2027
Code	G	H	I	J	K	L	M	N	O

Month	Jan	Feb	Mar	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Code	1	2	3	4	5	6	7	8	9	O	N	D

Marking Information (continued)

U-DFN2020-6 (Type F)



96 = Product Type Marking Code
 YWX = Date Code Marking
 Y = Year (ex: 9 = 2019)
 W = Week (ex: a = week 27; z represents week 52 and 53)
 X = Internal Code (ex: U = Monday)

Date Code Key

Year	2019	2020	2021	2022	2023	2024	2025	2026	2027
Code	9	0	1	2	3	4	5	6	7

Week	1-26	27-52	53
Code	A-Z	a-z	z

Internal Code	Sun	Mon	Tue	Wed	Thu	Fri	Sat
Code	T	U	V	W	X	Y	Z

Maximum Ratings (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Drain-Source Voltage	V_{DSS}	115	V
Gate-Source Voltage	V_{GSS}	± 12	V
Continuous Drain Current, $V_{GS} = 10\text{V}$ (Note 6)	I_D	$T_A = +25^\circ\text{C}$	4.3
		$T_A = +70^\circ\text{C}$	3.4
Pulsed Drain Current (10 μs Pulse, Duty Cycle = 1%)	I_{DM}	25	A
Maximum Body Diode Continuous Current (Note 6)	I_S	6	A
Pulsed Body Diode Continuous Current (10 μs Pulse, Duty Cycle = 1%)	I_{SM}	25	A
Avalanche Current, $L = 0.3\text{mH}$	I_{AS}	4	A
Avalanche Energy, $L = 0.3\text{mH}$	E_{AS}	2.4	mJ

Thermal Characteristics (@ $T_A = +25^\circ\text{C}$, unless otherwise specified.)

Characteristic	Symbol	Value	Unit
Total Power Dissipation (Note 5)	P_D	$T_A = +25^\circ\text{C}$	1.0
		$T_A = +70^\circ\text{C}$	0.6
Thermal Resistance, Junction to Ambient (Note 5)	$R_{\theta JA}$	124	$^\circ\text{C}/\text{W}$
Total Power Dissipation (Note 6)	P_D	$T_A = +25^\circ\text{C}$	1.8
		$T_A = +70^\circ\text{C}$	1.2
Thermal Resistance, Junction to Ambient (Note 6)	$R_{\theta JA}$	69	$^\circ\text{C}/\text{W}$
Thermal Resistance, Junction to Case (Note 6)	$R_{\theta JC}$	13	
Operating and Storage Temperature Range	T_J, T_{STG}	-55 to +150	$^\circ\text{C}$

Notes: 5. Device mounted on FR-4 substrate PC board, 2oz copper, with minimum recommended pad layout.
 6. Device mounted on FR-4 substrate PC board, 2oz copper, with 1inch square copper plate.

Electrical Characteristics (@T_A = +25°C, unless otherwise specified.)

Characteristic	Symbol	Min	Typ	Max	Unit	Test Condition
OFF CHARACTERISTICS (Note 7)						
Drain-Source Breakdown Voltage	BV _{DSS}	115	—	—	V	V _{GS} = 0V, I _D = 10mA
Zero Gate Voltage Drain Current	I _{DSS}	—	—	1	μA	V _{DS} = 92V, V _{GS} = 0V
Gate-Source Leakage	I _{GSS}	—	—	±100	nA	V _{GS} = ±9.6V, V _{DS} = 0V
ON CHARACTERISTICS (Note 7)						
Gate Threshold Voltage	V _{GS(TH)}	0.6	—	2.2	V	V _{DS} = V _{GS} , I _D = 250μA
Static Drain-Source On-Resistance	R _{DS(ON)}	—	43	65	mΩ	V _{GS} = 10V, I _D = 3A
		—	54	70		V _{GS} = 4.5V, I _D = 3A
		—	58	150		V _{GS} = 3.8V, I _D = 1.0A
		—	75	350		V _{GS} = 3V, I _D = 0.5A
		—	—	—		V _{GS} = 0V, I _S = 2.4A
Diode Forward Voltage	V _{SD}	—	0.8	1.3	V	V _{GS} = 0V, I _S = 2.4A
DYNAMIC CHARACTERISTICS (Note 8)						
Input Capacitance	C _{ISS}	—	252	—	pF	V _{DS} = 50V, V _{GS} = 0V, f = 1MHz
Output Capacitance	C _{OSS}	—	80	—	pF	
Reverse Transfer Capacitance	C _{RSS}	—	3	—	pF	
Gate Resistance	R _g	—	6.9	—	Ω	V _{DS} = 0V, V _{GS} = 0V, f = 1MHz
Total Gate Charge	Q _g	—	5.5	—	nC	V _{DS} = 50V, I _D = 4.5A, V _{GS} = 10V
Gate-Source Charge	Q _{gs}	—	0.4	—	nC	
Gate-Drain Charge	Q _{gd}	—	1.7	—	nC	
Turn-On Delay Time	t _{D(ON)}	—	2.1	—	ns	V _{DS} = 50V, R _L = 11Ω V _{GS} = 10V, R _{GEN} = 3Ω
Turn-On Rise Time	t _R	—	2	—	ns	
Turn-Off Delay Time	t _{D(OFF)}	—	10	—	ns	
Turn-Off Fall Time	t _F	—	3.6	—	ns	
Reverse Recovery Time	t _{RR}	—	101	—	ns	
Reverse Recovery Charge	Q _{RR}	—	212	—	nC	I _F = 4.5A, di/dt = 300A/μs

Notes: 7. Short duration pulse test used to minimize self-heating effect.
8. Guaranteed by design. Not subject to product testing.

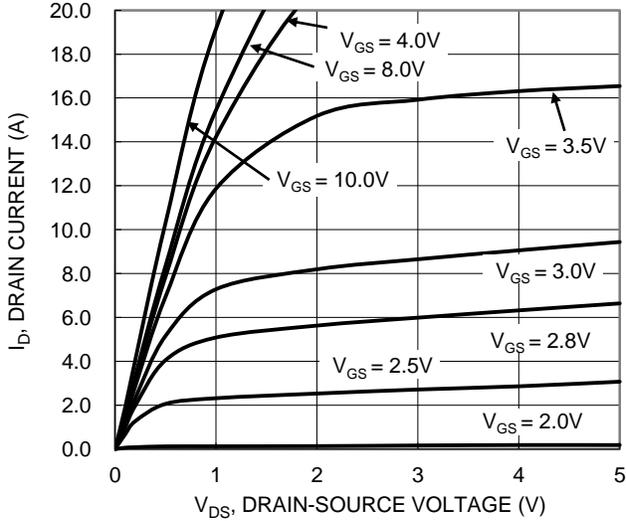


Figure 1. Typical Output Characteristic

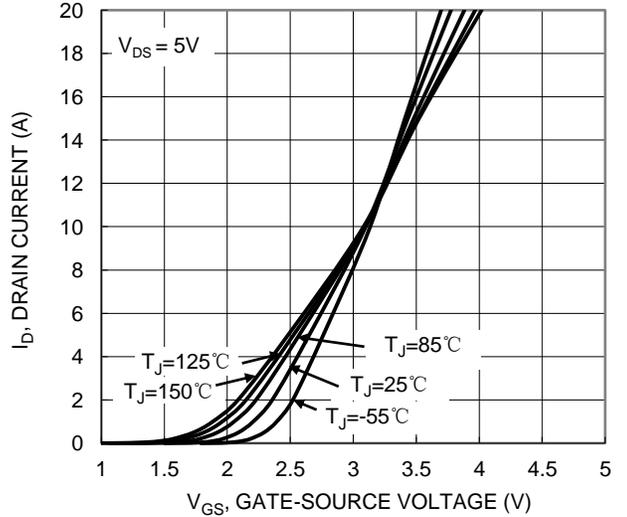


Figure 2. Typical Transfer Characteristic

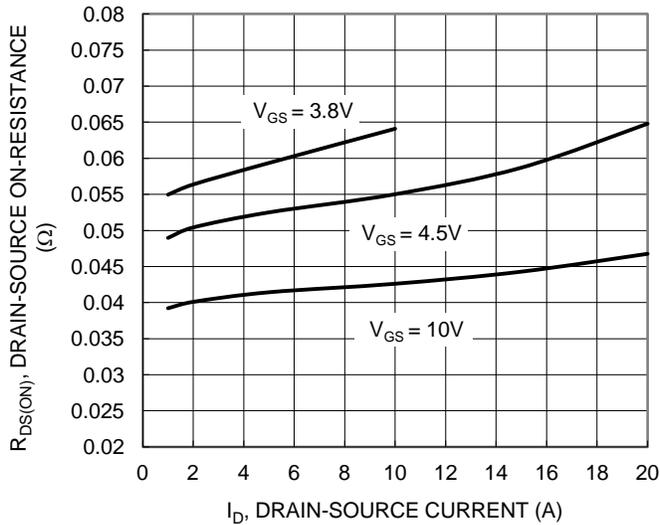


Figure 3. Typical On-Resistance vs. Drain Current and Gate Voltage

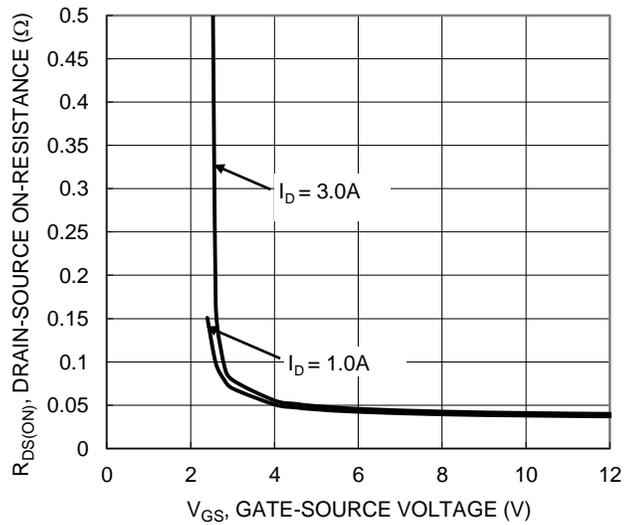


Figure 4. Typical Transfer Characteristic

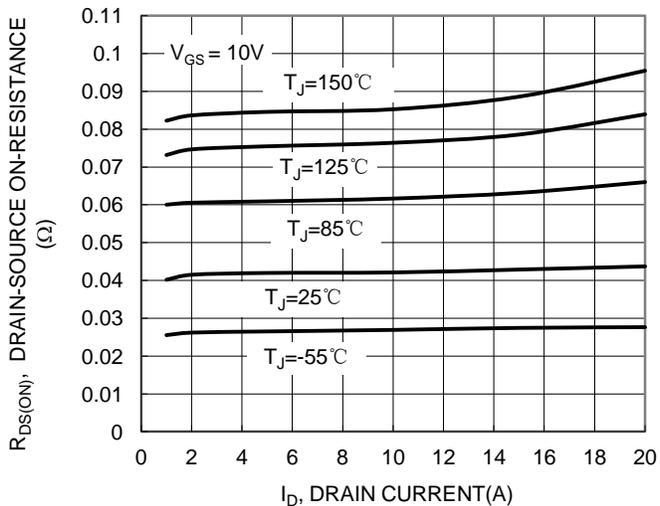


Figure 5. Typical On-Resistance vs. Drain Current and Junction Temperature

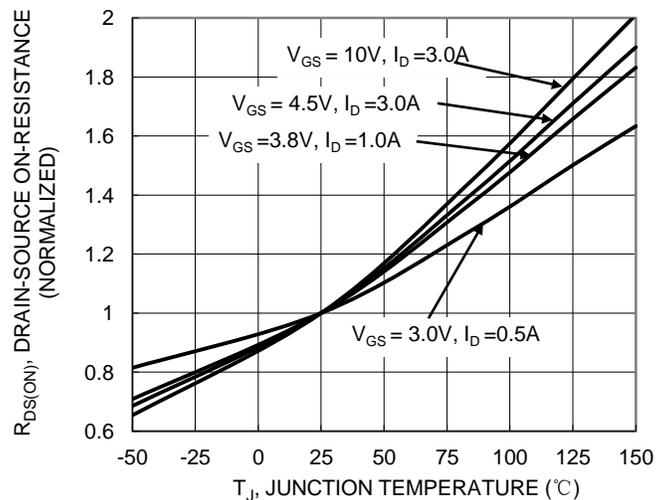


Figure 6. On-Resistance Variation with Junction Temperature

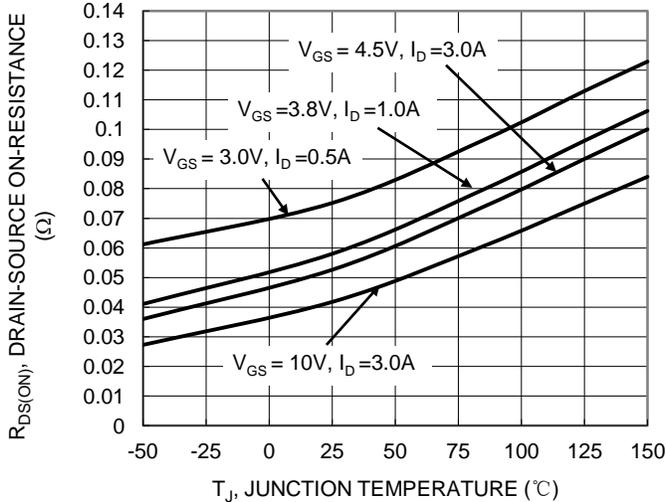


Figure 7. On-Resistance Variation with Junction Temperature

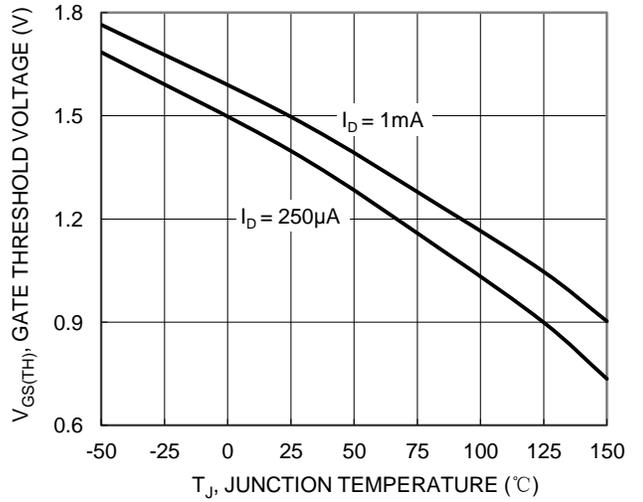


Figure 8. Gate Threshold Variation vs. Junction Temperature

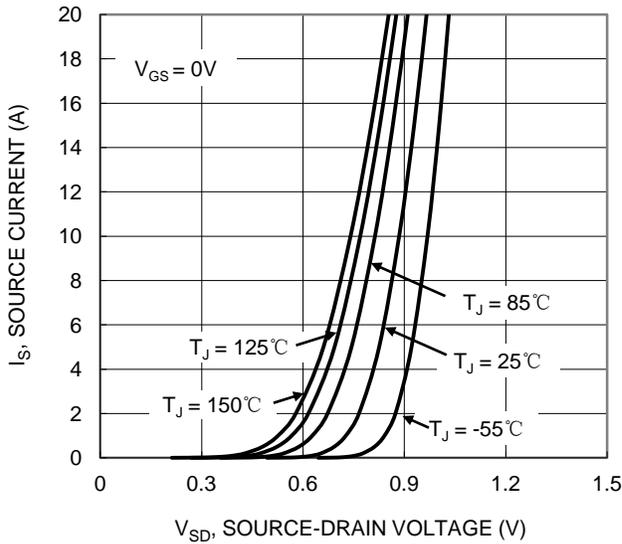


Figure 9. Diode Forward Voltage vs. Current

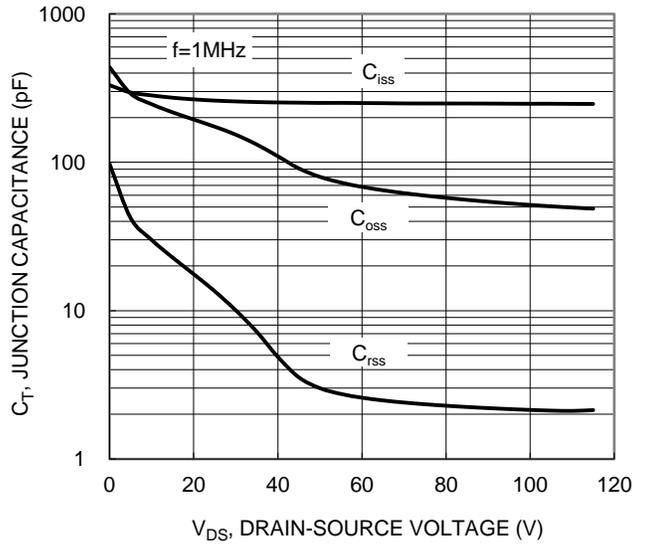


Figure 10. Typical Junction Capacitance

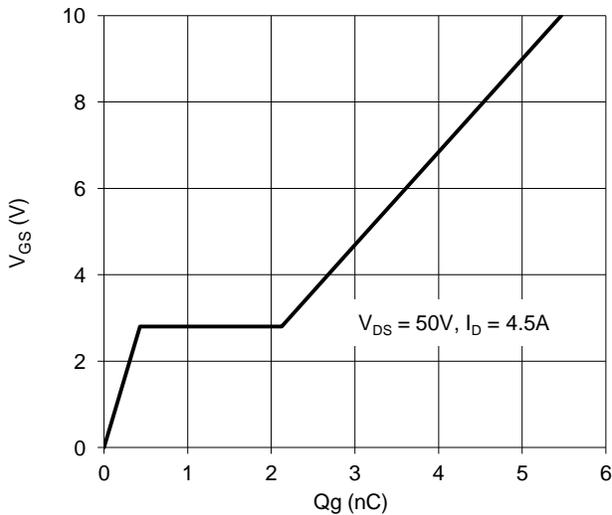


Figure 11. Gate Charge

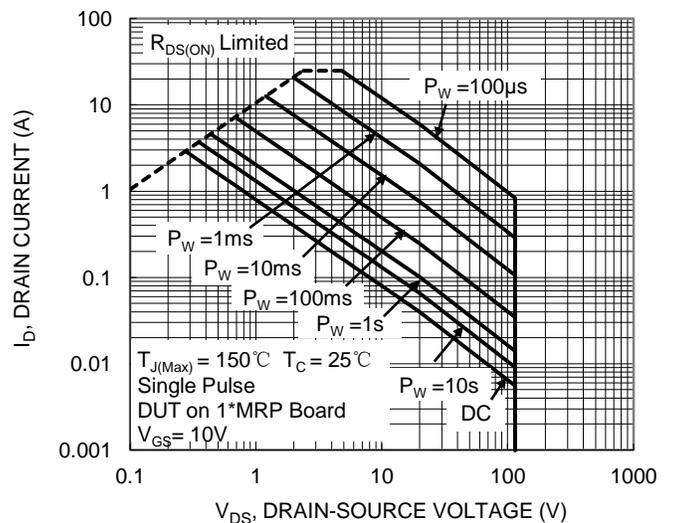


Figure 12. SOA, Safe Operation Area

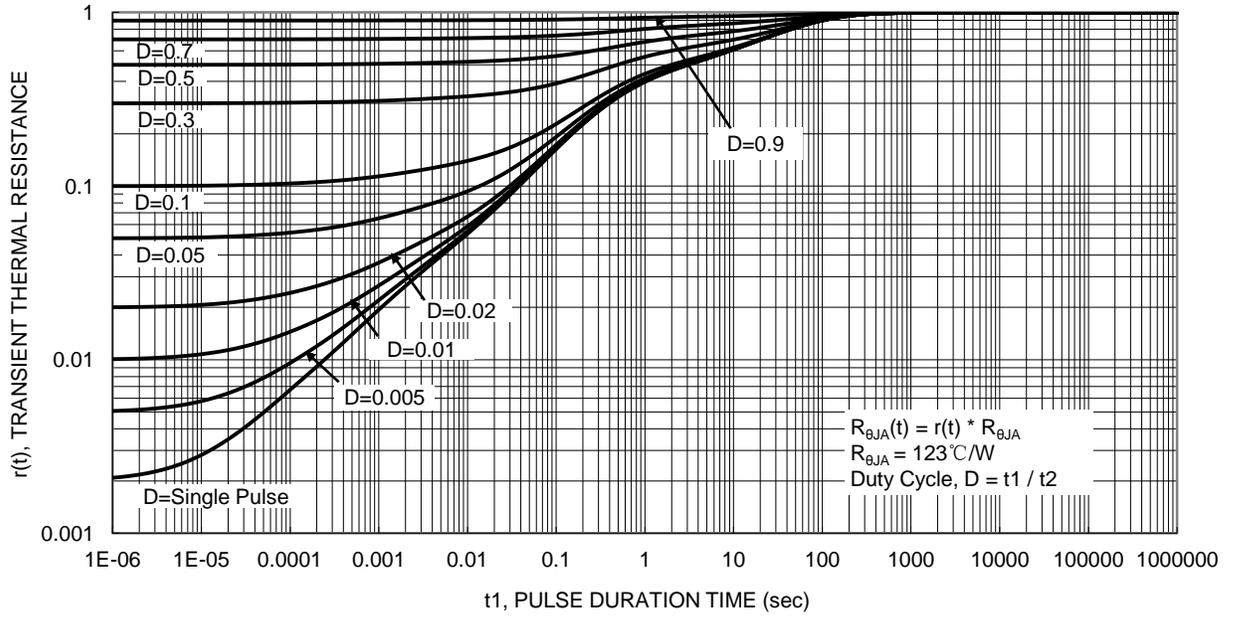
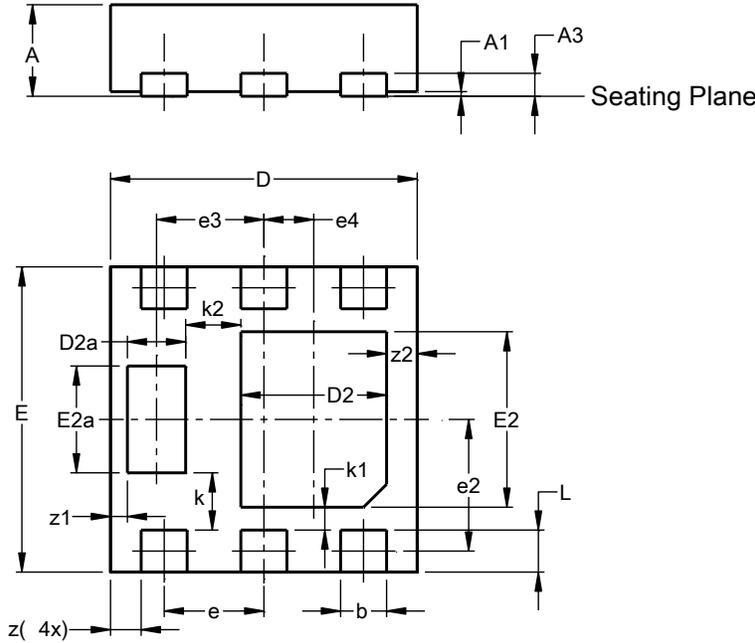


Figure 13. Transient Thermal Resistance

Package Outline Dimensions

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

U-DFN2020-6 (Type F)

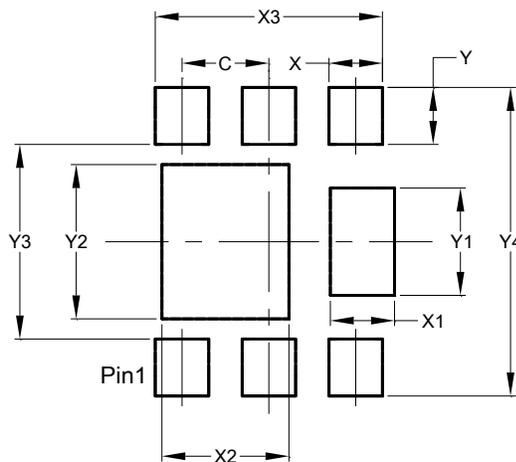


U-DFN2020-6 (Type F)			
Dim	Min	Max	Typ
A	0.57	0.63	0.60
A1	0.00	0.05	0.03
A3	-	-	0.15
b	0.25	0.35	0.30
D	1.95	2.05	2.00
D2	0.85	1.05	0.95
D2a	0.33	0.43	0.38
E	1.95	2.05	2.00
E2	1.05	1.25	1.15
E2a	0.65	0.75	0.70
e	0.65 BSC		
e2	0.863 BSC		
e3	0.70 BSC		
e4	0.325 BSC		
k	0.37 BSC		
k1	0.15 BSC		
k2	0.36 BSC		
L	0.225	0.325	0.275
z	0.20 BSC		
z1	0.110 BSC		
z2	0.20 BSC		
All Dimensions in mm			

Suggested Pad Layout

Please see <http://www.diodes.com/package-outlines.html> for the latest version.

U-DFN2020-6 (Type F)



Dimensions	Value (in mm)
C	0.650
X	0.400
X1	0.480
X2	0.950
X3	1.700
Y	0.425
Y1	0.800
Y2	1.150
Y3	1.450
Y4	2.300

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