Product Change Notice (PCN)

Subject: Product Improvement – Design Change for the Listed Intersil HIP4086* Products
Publication Date: 1/13/2017
Effective Date: 4/13/2017

Revision Description:
Initial Release

Description of Change:
This notice is to advise our customers of a minor, single level, design revision for the products listed below. The mask modification to the high side bias circuit reduces product susceptibility to shoot-through in certain circuit configurations. Products incorporating the improved design are completely compatible in any existing designs using the previous version of the product. Product data sheet updates reflecting the performance characteristics of the improved design are shown below in Appendix A.

Products impacted by the change are:

HIP4086AABZ	HIP4086AB	HIP4086ABZ	HIP4086ABZT
HIP4086AABZT	HIP4086ABT	HIP4086ABZATS2490	HIP4086APZ

Reason for Change:
The change in the product design is being implemented to eliminate the potential for shoot-through when dv/dt on the xHS node is high.

Impact on fit, form, function, quality & reliability:
The change will have no other impact on the form, fit, function, quality, reliability and environmental compliance of the devices.

Product Identification:
There will be no change in the external marking of the packaged parts. Product affected by this change is identifiable via Intersil's internal traceability system.

Qualification status: Completed, functional validation performed
Sample availability: 1/13/2017
Device material declaration: Available upon request

Questions or requests pertaining to this change notice, including additional data or samples, must be sent to Intersil within 30 days of the publication date.

For additional information regarding this notice, please contact your regional change coordinator (below)			
Americas: PCN-US@INTERSIL.COM	Europe: PCN-EU@INTERSIL.COM	Japan: PCN-JP@INTERSIL.COM	Asia Pac: PCN-APAC@INTERSIL.COM

Appendix A

From (page 5) :

DC Electrical Specifications $V_{DD} = V_{xHB} = 12V$, $V_{SS} = V_{xHS} = 0V$, $R_{DEL} = 20k$, $R_{UV} = \infty$, Gate Capacitance (C_{GATE}) = 1000pF, unless otherwise specified. **Boldface limits apply across the operating junction temperature range, -40°C to +150°C.**

PARAMETER	TEST CONDITIONS	T_J = +25°C MIN (Note 9)	TYP	MAX (Note 9)	T_J = -40°C TO +150°C MIN (Note 9)	MAX (Note 9)	UNITS
SUPPLY CURRENTS							
V_{DD} Quiescent Current	$\overline{xHI}$ = 5V, xLI = 5V (HIP4086)	2.7	3.4	4.2	**2.1**	**4.3**	mA
	$\overline{xHI}$ = 5V, xLI = 5V (HIP4086A)	2.3	2.4	2.6	**2.1**	**2.7**	mA
V_{DD} Operating Current	f = 20kHz, 50% Duty Cycle (HIP4086)	6.3	8.25	10.5	**5**	**11**	mA
	f = 20kHz, 50% Duty Cycle (HIP4086A)	3.1	3.6	4.1	**2.8**	**4.4**	mA
xHB On Quiescent Current	$\overline{xHI}$ = 0V (HIP4086)	-	40	80	**-**	**100**	µA
	$\overline{xHI}$ = 0V (HIP4086A)		80	100		**200**	µA
xHB Off Quiescent Current	$\overline{xHI}$ = V_{DD} (HIP4086)	0.6	0.8	1.3	**0.5**	**1.4**	mA
	$\overline{xHI}$ = V_{DD} (HIP4086A)	0.8	0.9	1	**0.7**	**1.2**	mA
xHB Operating Current	f = 20kHz, 50% Duty Cycle (HIP4086)	0.7	0.9	1.3	**-**	**2.0**	mA
	f = 20kHz, 50% Duty Cycle (HIP4086A)	0.8	0.9	1	**-**	**1.2**	mA
xHB, xHS Leakage Current	V_{XHS} = 80V, V_{XHB} = 93V	7	24	45	**-**	**50**	µA
Charge Pump, HIP4086 only, (Note 8)							
Q_{PUMP} Output Voltage	No Load	11.5	12.5	14	**10.5**	**14.5**	V
Q_{PUMP} Output Current	V_{XHS} = 12V, V_{XHB} = 22V	50	100	130	**-**	**140**	µA
UNDERVOLTAGE PROTECTION							
V_{DD} Rising Undervoltage Threshold	R_{UV} open	6.2	7.1	8.0	**6.1**	**8.1**	V
V_{DD} Falling Undervoltage Threshold	R_{UV} open	5.75	6.6	7.5	**5.6**	**7.6**	V
Minimum Undervoltage Threshold	R_{UV} = V_{DD}	5	6.2	6.8	**4.9**	**6.9**	V

To (page 5) :

DC Electrical Specifications $V_{DD} = V_{xHB} = 12V$, $V_{SS} = V_{xHS} = 0V$, $R_{DEL} = 20k$, $R_{UV} = \infty$, Gate Capacitance (C_{GATE}) = 1000pF, unless otherwise specified. **Boldface limits apply across the operating junction temperature range, -40°C to +150°C.**

PARAMETER	TEST CONDITIONS	T_J = +25°C MIN (Note 9)	TYP	MAX (Note 9)	T_J = -40°C TO +150°C MIN (Note 9)	MAX (Note 9)	UNIT
SUPPLY CURRENTS							
V_{DD} Quiescent Current	$\overline{xHI}$ = 5V, xLI = 5V (HIP4086)	2.7	3.4	5.1	**1.96**	**5.3**	mA
	$\overline{xHI}$ = 5V, xLI = 5V (HIP4086A)	2.3	2.8	3.1	**1.8**	**3.3**	mA
V_{DD} Operating Current	f = 20kHz, 50% Duty Cycle (HIP4086)	5.4	8.25	13	**4**	**13.5**	mA
	f = 20kHz, 50% Duty Cycle (HIP4086A)	3.1	4.0	4.6	**2.7**	**5.1**	mA
xHB On Quiescent Current	$\overline{xHI}$ = 0V (HIP4086)	-	40	110	-	**140**	µA
	$\overline{xHI}$ = 0V (HIP4086A)	-	90	115	-	**225**	µA
xHB Off Quiescent Current	$\overline{xHI}$ = V_{DD} (HIP4086)	0.6	0.8	1.3	**0.5**	**1.4**	mA
	$\overline{xHI}$ = V_{DD} (HIP4086A)	0.8	1.0	1.2	**0.7**	**1.25**	mA
xHB Operating Current	f = 20kHz, 50% Duty Cycle (HIP4086)	0.7	0.9	1.3	-	**2.0**	mA
	f = 20kHz, 50% Duty Cycle (HIP4086A)	0.8	0.9	1.1	-	**1.25**	mA
xHB, xHS Leakage Current	V_{XHS} = 80V, V_{XHB} = 93V	7	30	45	-	**50**	µA
Charge Pump, HIP4086 Only, (Note 8)							
Q_{PUMP} Output Voltage	No Load	11	12.5	14.6	**10**	**14.75**	V
Q_{PUMP} Output Current	V_{XHS} = 12V, V_{XHB} = 22V	40	100	160	-	**185**	µA
UNDERVOLTAGE PROTECTION							
V_{DD} Rising Undervoltage Threshold	R_{UV} open	6.2	7.1	8.0	**6.1**	**8.1**	V
V_{DD} Falling Undervoltage Threshold	R_{UV} open	5.75	6.6	7.5	**5.6**	**7.6**	V
Minimum Undervoltage Threshold	R_{UV} = V_{DD}	5	6.2	6.8	**4.8**	**6.9**	V

From (page 6) :

DC Electrical Specifications $V_{DD} = V_{xHB} = 12V$, $V_{SS} = V_{xHS} = 0V$, $R_{DEL} = 20k$, $R_{UV} = \infty$, Gate Capacitance (C_{GATE}) = 1000pF, unless otherwise specified. **Boldface limits apply across the operating junction temperature range, -40°C to +150°C. (Continued)**

PARAMETER	TEST CONDITIONS	$T_J = +25°C$ MIN (Note 9)	TYP	MAX (Note 9)	$T_J = -40°C$ TO +150°C MIN (Note 9)	MAX (Note 9)	UNITS
INPUT PINS: ALI, BLI, CLI, $\overline{AHI}$, $\overline{BHI}$, $\overline{CHI}$, AND DIS							
Low Level Input Voltage		-	-	1.0	-	**0.8**	V
High Level Input Voltage		2.5	-	-	**2.7**	-	V
Input Voltage Hysteresis		-	35	-	-	-	mV
Low Level Input Current	$V_{IN} = 0V$	-60	-100	-135	**-55**	**-140**	µA
High Level Input Current	$V_{IN} = 5V$	-1	-	+1	**-10**	**+10**	µA
GATE DRIVER OUTPUT PINS: ALO, BLO, CLO, AHO, BHO, AND CHO							
Low Level Output Voltage ($V_{OUT} - V_{SS}$)	$I_{SINKING} = 30mA$	-	100	-	-	**200**	mV
Peak Turn-On Current	$V_{OUT} = 0V$	0.3	0.5	0.7	-	**1.0**	A

To (page 6) :

DC Electrical Specifications $V_{DD} = V_{xHB} = 12V$, $V_{SS} = V_{xHS} = 0V$, $R_{DEL} = 20k$, $R_{UV} = \infty$, Gate Capacitance (C_{GATE}) = 1000pF, unless otherwise specified. **Boldface limits apply across the operating junction temperature range, -40°C to +150°C. (Continued)**

PARAMETER	TEST CONDITIONS	$T_J = +25°C$ MIN (Note 9)	TYP	MAX (Note 9)	$T_J = -40°C$ TO +150°C MIN (Note 9)	MAX (Note 9)	UNIT
INPUT PINS: ALI, BLI, CLI, $\overline{AHI}$, $\overline{BHI}$, $\overline{CHI}$, AND DIS							
Low Level Input Voltage		-	-	1.0	-	**0.8**	V
High Level Input Voltage		2.5	-	-	**2.7**	-	V
Input Voltage Hysteresis		-	35	-	-	-	mV
Low Level Input Current	$V_{IN} = 0V$	-60	-100	-155	**-55**	**-165**	µA
High Level Input Current	$V_{IN} = 5V$	-1	-	+1	**-10**	**+10**	µA
GATE DRIVER OUTPUT PINS: ALO, BLO, CLO, AHO, BHO, AND CHO							
Low Level Output Voltage ($V_{OUT} - V_{SS}$)	$I_{SINKING} = 30mA$	-	100	-	-	**210**	mV
Peak Turn-On Current	$V_{OUT} = 0V$	0.3	0.5	0.7	-	**1.0**	A

From (page 6) :

AC Electrical Specifications

$V_{DD} = V_{xHB} = 12V$, $V_{SS} = V_{xHS} = 0V$, $C_{GATE} = 1000pF$, $R_{DEL} = 10k$, unless otherwise specified. **Boldface limits apply over the operating junction temperature range, -40°C to +150°C.**

PARAMETER	TEST CONDITIONS	$T_J = +25°C$			$T_J = -40°C$ TO +150°C		UNITS
		MIN (Note 9)	TYP	MAX (Note 9)	MIN (Note 9)	MAX (Note 9)	
TURN-ON DELAY AND PROPAGATION DELAY							
Dead Time (Figure 3)	$R_{DEL} = 100k\Omega$	3.8	4.5	6	**3**	**7**	µs
	$R_{DEL} = 10k\Omega$	0.38	0.5	0.65	**0.3**	**0.7**	µs
Dead Time Channel Matching	$R_{DEL} = 10k\Omega$	-	7	15	**-**	**20**	%
Lower Turn-off Propagation Delay (xLI to xLO turn-off) (Figures 3 or 4)	No Load	-	30	45	**-**	**65**	ns
Upper Turn-off Propagation Delay ($\overline{xHI}$ to xHO turn-off) (Figures 3 or 4)	No Load	-	75	90	**-**	**100**	ns
Lower Turn-on Propagation Delay (xLI to xLO turn-on) (Figures 3 or 4)	No Load	-	45	75	**-**	**90**	ns
Upper Turn-on Propagation Delay ($\overline{xHI}$ to xHO turn-on) (Figures 3 or 4)	No Load	-	65	90	**-**	**100**	ns
Rise Time	$C_{GATE} = 1000pF$	-	20	40	**-**	**50**	ns
Fall Time	$C_{GATE} = 1000pF$	-	10	20	**-**	**25**	ns
Disable Turn-off Propagation Delay (DIS to xLO turn-off) (Figure 5)		-	55	80	**-**	**90**	ns
Disable Turn-off Propagation Delay (DIS to xHO turn-off) (Figure 5)		-	80	90	**-**	**100**	ns
$\overline{Disable}$ to Lower Turn-on Propagation Delay ($\overline{DIS}$ to xLO turn-on) (Figure 5)		-	55	80	**-**	**100**	ns
$\overline{Disable}$ to Upper Enable ($\overline{DIS}$ to xHO turn-on) (Figure 5)	$R_{DEL} = 10k\Omega$, C_{RFSH} Open	-	2.0	-	**-**	**-**	µs

To (page 6) :

AC Electrical Specifications

$V_{DD} = V_{xHB} = 12V$, $V_{SS} = V_{xHS} = 0V$, $C_{GATE} = 1000pF$, $R_{DEL} = 10k$, unless otherwise specified. **Boldface limits apply across the operating junction temperature range, -40°C to +150°C.**

PARAMETER	TEST CONDITIONS	$T_J = +25°C$			$T_J = -40°C$ TO +150°C		UNIT
		MIN (Note 9)	TYP	MAX (Note 9)	MIN (Note 9)	MAX (Note 9)	
TURN-ON DELAY AND PROPAGATION DELAY							
Dead Time (Figure 4)	$R_{DEL} = 100k\Omega$	3	4.5	7.2	**3**	**8**	µs
	$R_{DEL} = 10k\Omega$	0.38	0.5	0.75	**0.3**	**0.8**	µs
Dead Time Channel Matching	$R_{DEL} = 10k\Omega$	-	7	15	-	**20**	%
Lower Turn-Off Propagation Delay (xLI to xLO Turn-Off) (Figures 4 or 5)	No load	-	30	55	-	**75**	ns
Upper Turn-Off Propagation Delay ($\overline{xHI}$ to xHO Turn-Off) (Figures 4 or 5)	No load	-	75	110	-	**135**	ns
Lower Turn-On Propagation Delay (xLI to xLO Turn-On) (Figures 4 or 5)	No load	-	45	82	-	**100**	ns
Upper Turn-On Propagation Delay ($\overline{xHI}$ to xHO Turn-On) (Figures 4 or 5)	No load	-	65	110	-	**158**	ns
Rise Time	$C_{GATE} = 1000pF$	-	20	40	-	**60**	ns
Fall Time	$C_{GATE} = 1000pF$	-	10	20	-	**40**	ns
$\overline{Disable}$ Lower Turn-Off Propagation Delay ($\overline{DIS}$ to xLO turn-off) (Figure 6)		-	55	80	-	**104**	ns
$\overline{Disable}$ Upper Turn-Off Propagation Delay ($\overline{DIS}$ to xHO turn-off) (Figure 6)		-	80	116	-	**147**	ns
$\overline{Disable}$ to Lower Turn-On Propagation Delay ($\overline{DIS}$ to xLO turn-on) (Figure 6)		-	55	85	-	**120**	ns
$\overline{Disable}$ to Upper Turn-On Propagation Delay ($\overline{DIS}$ to xHO turn-on) (Figure 6)	$R_{DEL} = 10k\Omega$, C_{RFSH} open	-	2.0	-	-	-	µs

From (page 11) :

Charge Pump

The internal charge pump of the HIP4086/A is used to maintain the bias on the boot cap for 100% duty cycle. There is no limit for the duration of this period. The user must understand that this charge pump is only intended to provide the static bias current of the high-side drivers and the gate leakage current of the high-side bridge FETs. It cannot provide in a reasonable time, the majority of the charge on the boot cap that is consumed, when the xHO drivers source the gate charge to turn on the high-side bridge FETs. The boot caps should be sized so that they do not discharge excessively when sourcing the gate charge. See "Application Information" on page 11 for methods to size the boot caps.

The charge pump has sufficient capacity to source a worst-case minimum of 50µA to the external load. The gate leakage current of most power MOSFETs is about 100nA so there is more than sufficient current to maintain the charge on the boot caps. Because the charge pump current is small, a gate-source resistor on the high-side bridge FETs is not recommended. When calculating the leakage load on the outputs of xHS, also include the leakage current of the boot capacitor. This is rarely a problem but it could be an issue with electrolytic capacitors at high temperatures.

To (page 11) :

Charge Pump

The internal charge pump of the HIP4086/A is used to maintain the bias on the boot capacitor for 100% duty cycle. There is no limit for the duration of this period. The user must understand that this charge pump is only intended to provide the static bias current of the high-side drivers and the gate leakage current of the high-side bridge FETs. It cannot provide in a reasonable time, the majority of the charge on the boot capacitor that is consumed, when the xHO drivers source the gate charge to turn on the high-side bridge FETs. The boot capacitors should be sized so that they do not discharge excessively when sourcing the gate charge. See "Application Information" for methods to size the boot capacitors.

The charge pump has sufficient capacity to source a worst-case minimum of 40µA to the external load. The gate leakage current of most power MOSFETs is about 100nA so there is more than sufficient current to maintain the charge on the boot capacitors. Because the charge pump current is small, a gate-to-source resistor on the high-side bridge FETs is not recommended. When calculating the leakage load on the outputs of xHS, also include the leakage current of the boot capacitor. This is rarely a problem but it could be an issue with electrolytic capacitors at high temperatures.

From (page 11) :

These values of C_{boot} will sustain the high side driver bias during Period with only a small amount of Ripple. But in the case of the HIP4086, the charge pump reduces the value of C_{boot} even more. The specified charge pump current is a minimum of 50µA which is more than sufficient to source I_{gate_leak}. Also, because the specified charge pump current is in excess of what is needed for I_{HB}, the total charge required to be sourced by the boot capacitor is shown by Equation 2.

$$Q_C = Q_{gate80V} \text{ or } C_{boot} = 0.13\mu F \quad \text{(EQ. 2)}$$

To (page 11) :

These values of C_{boot} will sustain the high-side driver bias during Period with only a small amount of Ripple. But in the case of the HIP4086, the charge pump reduces the value of C_{boot} even more. The specified charge pump current is a minimum of 40µA, which is more than sufficient to source I_{gate_leak}. Also, because the specified charge pump current is in excess of what is needed for I_{HB}, the total charge required to be sourced by the boot capacitor is shown by Equation 2.

$$Q_C = Q_{gate80V} \text{ or } C_{boot} = 0.13\mu F \quad \text{(EQ. 2)}$$