

## NDP7050 / NDB7050

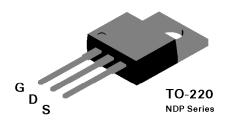
### N-Channel Enhancement Mode Field Effect Transistor

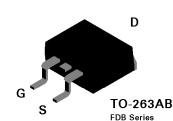
### **General Description**

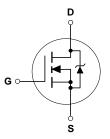
These N-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, high cell density, DMOS technology. This very high density process is especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulses in the avalanche and commutation modes. These devices are particularly suited for low voltage applications such as automotive, DC/DC converters, PWM motor controls, and other battery powered circuits where fast switching, low in-line power loss, and resistance to transients are needed.

#### **Features**

- 75A, 50V.  $R_{DS(ON)} = 0.013\Omega$  @  $V_{GS} = 10V$ .
- Critical DC electrical parameters specified at elevated temperature.
- Rugged internal source-drain diode can eliminate the need for an external Zener diode transient suppressor.
- 175°C maximum junction temperature rating.
- High density cell design for extremely low R<sub>DS(ON)</sub>.
- TO-220 and TO-263 (D<sup>2</sup>PAK) package for both through hole and surface mount applications.







#### **Absolute Maximum Ratings** T<sub>c</sub> = 25°C unless otherwise noted

Symbol	Parameter	NDP7050	NDB7050	Units
V <sub>DSS</sub>	Drain-Source Voltage		V	
$V_{DGR}$	Drain-Gate Voltage ( $R_{GS} \le 1 \text{ M}\Omega$ )		V	
V <sub>GSS</sub>	Gate-Source Voltage - Continuous	±	V	
	- Nonrepetitive (t <sub>P</sub> < 50 μs)	±		
I <sub>D</sub>	Drain Current - Continuous		А	
	- Pulsed	2		
P <sub>D</sub>	Maximum Power Dissipation @ T <sub>C</sub> = 25°C	1	W	
	Derate above 25°C		W/°C	
T <sub>J</sub> ,T <sub>STG</sub>	Operating and Storage Temperature Range	-65	.€	
T <sub>L</sub>	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds	2	275	°C

Symbol	Parameter	Conditions	Min	Тур	Max	Units	
DRAIN-S	OURCE AVALANCHE RATINGS (Note 1)	·					
W <sub>DSS</sub>	Single Pulse Drain-Source Avalanche Energy	$V_{DD} = 25 \text{ V}, I_{D} = 75 \text{ A}$				550	mJ
I <sub>AR</sub>	Maximum Drain-Source Avalanche Curre			75	Α		
OFF CH	ARACTERISTICS						
$BV_{DSS}$	Drain-Source Breakdown Voltage	$V_{GS} = 0 \text{ V}, I_{D} = 250 \mu\text{A}$		50			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}$	T <sub>.</sub> = 125°C			250 1	μA mA
I <sub>GSSF</sub>	Gate - Body Leakage, Forward	$V_{GS} = 20 \text{ V}, V_{DS} = 0 \text{ V}$	J			100	nA
I <sub>GSSR</sub>	Gate - Body Leakage, Reverse	$V_{GS} = -20 \text{ V}, V_{DS} = 0 \text{ V}$				-100	nA
ON CHAP	RACTERISTICS (Note 1)						
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_{D} = 250 \mu\text{A}$		2	2.8	4	V
			T <sub>J</sub> = 125°C	1.4	2.1	3.6	
R <sub>DS(ON)</sub>	Static Drain-Source On-Resistance	$V_{GS} = 10 \text{ V}, I_{D} = 40 \text{ A}$			0.01	0.013	Ω
			$T_J = 125^{\circ}C$		0.015	0.023	
I <sub>D(on)</sub>	On-State Drain Current	$V_{GS} = 10 \text{ V}, V_{DS} = 10 \text{ V}$	·	75			Α
g <sub>FS</sub>	Forward Transconductance	$V_{DS} = 10 \text{ V}, I_{D} = 37.5 \text{ A}$		15	39		S
DYNAMIC	CHARACTERISTICS						
$C_{iss}$	Input Capacitance	$V_{DS} = 25 \text{ V}, V_{GS} = 0 \text{ V},$ f = 1.0 MHz			2960	3600	pF
Coss	Output Capacitance	f = 1.0 MHz			1130	1600	pF
C <sub>rss</sub>	Reverse Transfer Capacitance				380	800	pF
SWITCHI	NG CHARACTERISTICS (Note 1)	- 1		ı		II.	
t <sub>D(on)</sub>	Turn - On Delay Time	$V_{DD} = 30 \text{ V}, I_{D} = 75 \text{ A},$			17	30	nS
t <sub>r</sub>	Turn - On Rise Time	$V_{GS} = 10 \text{ V}, R_{GEN} = 5 \Omega$		128	400	nS	
t <sub>D(off)</sub>	Tum - Off Delay Time			54	80	nS	
t <sub>f</sub>	Tum - Off Fall Time				90	200	nS
$\overline{Q_g}$	Total Gate Charge	$V_{DS} = 48 \text{ V},$ $I_{D} = 75 \text{ A}, V_{GS} = 10 \text{ V}$			100	115	nC
$Q_{gs}$	Gate-Source Charge	$I_D = 75 \text{ A}, \ V_{GS} = 10 \text{ V}$			14.5		nC
$Q_{gd}$	Gate-Drain Charge				51		nC

Symbol	Parameter	Min	Тур	Max	Units		
DRAIN-S	OURCE DIODE CHARACTERISTICS			•	•		•
l <sub>s</sub>	Maximum Continuos Drain-Source Diode			75	Α		
SM	Maximum Pulsed Drain-Source Diode Fo			225	Α		
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}, I_{S} = 37.5 \text{ A (Note 1)}$			0.9	1.3	V
			T <sub>J</sub> = 125°C		0.84	1.2	
· Tr	Reverse Recovery Time	$V_{GS} = 0 \text{ V}, I_F = 75 \text{ A}, dI_F/dt = 100 \text{ A}$	Vµs		80	150	ns
rr	Reverse Recovery Current			2	4.8	10	Α
THERMA	L CHARACTERISTICS	<u> </u>					•
R <sub>øJC</sub>	Thermal Resistance, Junction-to-Case			1	°C/M		
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient			62.5	°C/M		

Note: 1. Pulse Test: Pulse Width  $\leq$  300  $\mu$ s, Duty Cycle  $\leq$  2.0%.

## **Typical Electrical Characteristics**

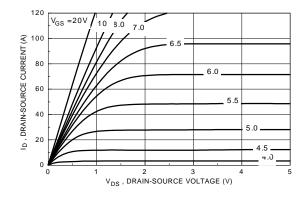
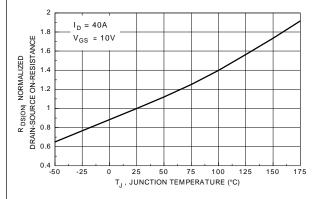


Figure 1. On-Region Characteristics.

Figure 2. On-Resistance Variation with Gate Voltage and Drain Current.



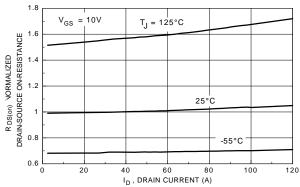
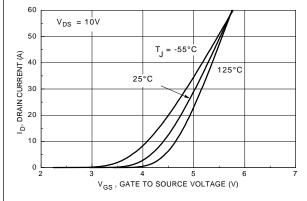


Figure 3. On-Resistance Variation with Temperature.

Figure 4. On-Resistance Variation with Drain Current and Temperature.



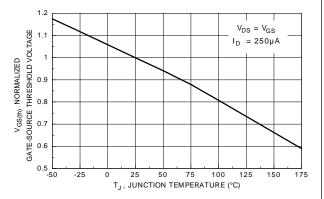


Figure 5. Transfer Characteristics.

Figure 6. Gate Threshold Variation with Temperature.

## **Typical Electrical Characteristics (continued)**

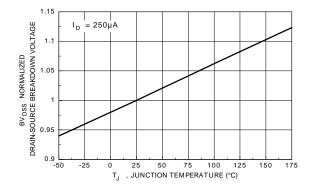


Figure 7. Breakdown Voltage Variation with Temperature.

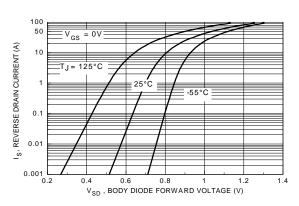


Figure 8. Body Diode Forward Voltage
Variation with Current and Temperature.

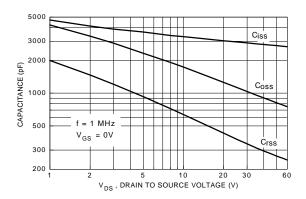


Figure 9. Capacitance Characteristics.

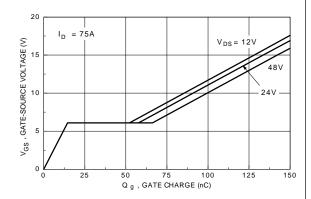


Figure 10. Gate Charge Characteristics.

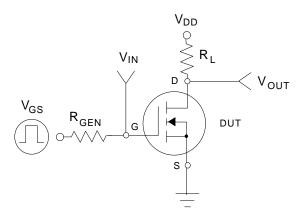


Figure 11. Switching Test Circuit.

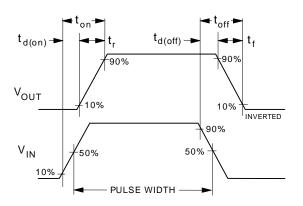
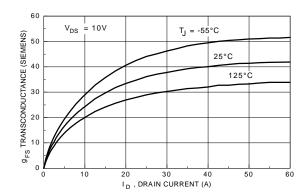


Figure 12. Switching Waveforms.

## **Typical Electrical Characteristics (continued)**



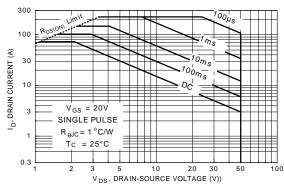


Figure 13. Transconductance Variation with Drain Current and Temperature.

Figure 14. Maximum Safe Operating Area.

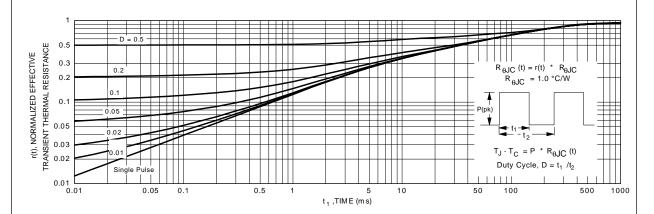
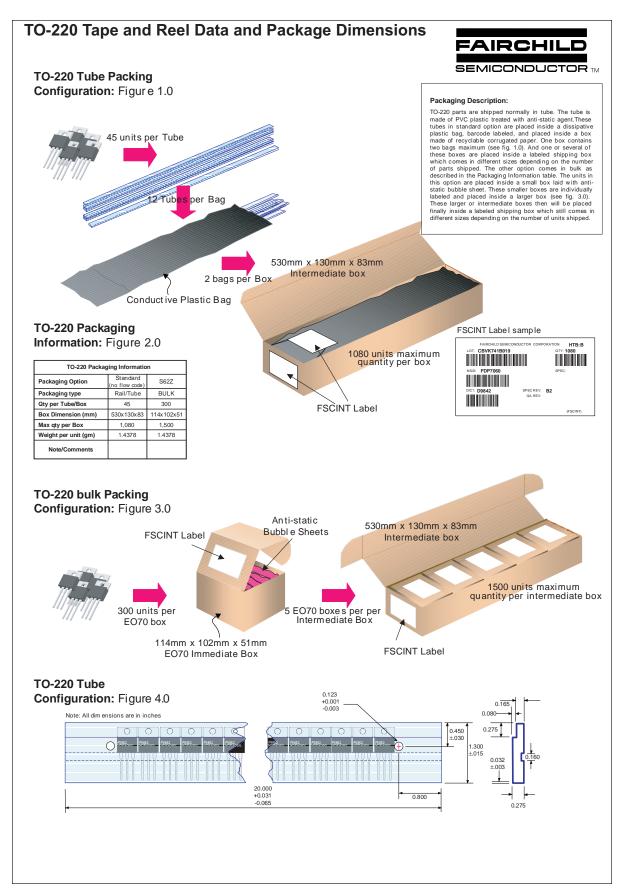
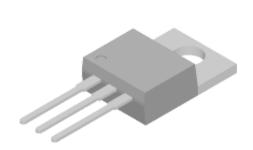


Figure 15. Transient Thermal Response Curve.

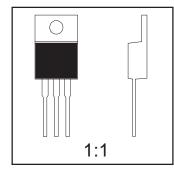


## TO-220 Tape and Reel Data and Package Dimensions, continued

# TO-220 (FS PKG Code 37)

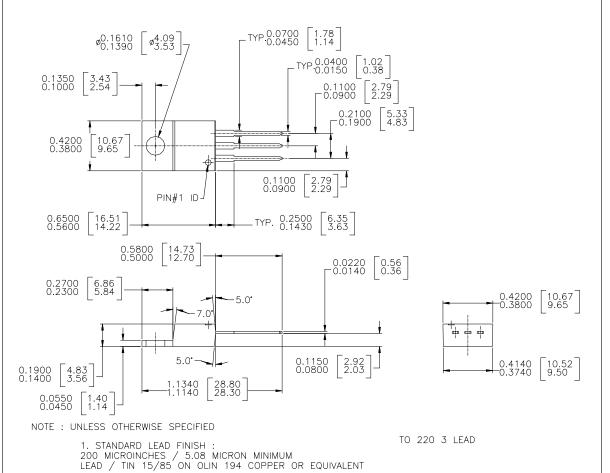


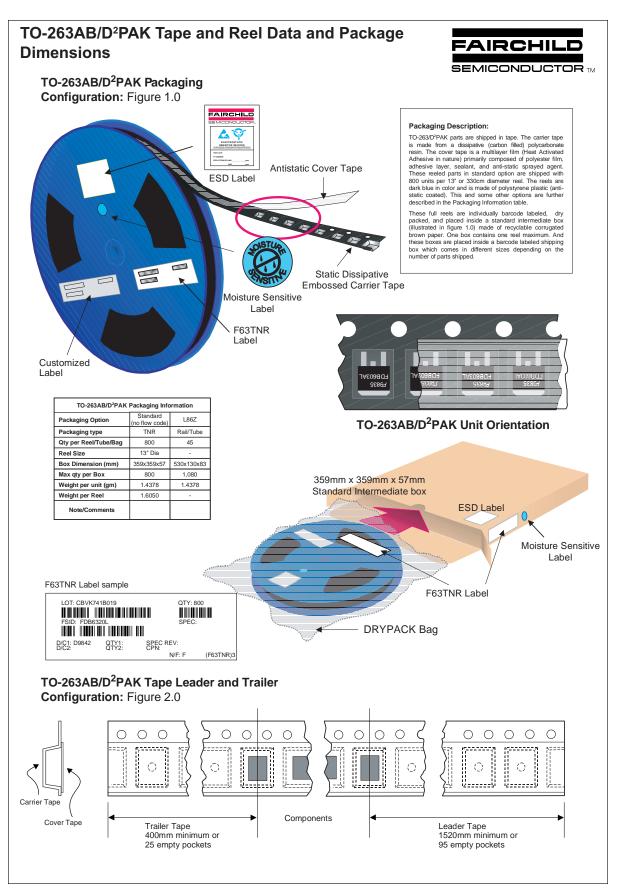
2. DIMENSION BASED ON JEDEC STANDARD TO-220 VARIATION AB, ISSUE J, DATED 3/24/87



Scale 1:1 on letter size paper
Dimensions shown below are in:
inches [millimeters]

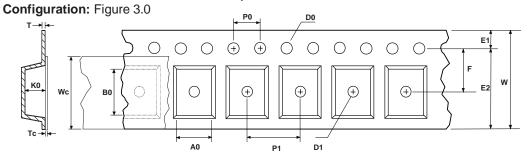
Part Weight per unit (gram): 1.4378





## TO-263AB/D<sup>2</sup>PAK Tape and Reel Data and Package Dimensions, continued

## TO-263AB/D<sup>2</sup>PAK Embossed Carrier Tape



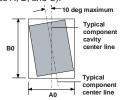
# User Direction of Feed

Dimensions are in millimeter														
Pkg type	Α0	В0	w	D0	D1	E1	E2	F	P1	P0	K0	Т	Wc	Тс
TO263AB/ D <sup>2</sup> PAK (24mm)	10.60 +/-0.10	15.80 +/-0.10	24.0 +/-0.3	1.55 +/-0.05	1.60 +/-0.10	1.75 +/-0.10	22.25 min	11.50 +/-0.10	16.0 +/-0.1	4.0 +/-0.1	4.90 +/-0.10	0.450 +/-0.150	21.0 +/-0.3	0.06 +/-0.02

Notes: A0, B0, and K0 dimensions are determined with respect to the EIA/Jedec RS-481 rotational and lateral movement requirements (see sketches A, B, and C).



Sketch A (Side or Front Sectional View)
Component Rotation

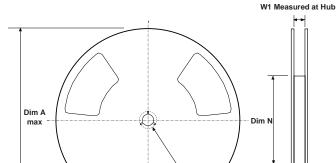


Sketch B (Top View)
Component Rotation

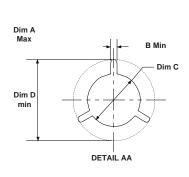


Sketch C (Top View)
Component lateral movement

# **TO-263AB/D<sup>2</sup>PAK Reel Configuration:** Figure 4.0







W2 max Measured at Hub

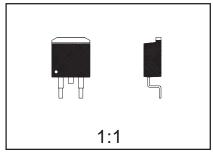
See detail AA

Dimensions are in inches and millimeters									
Tape Size	Reel Option	Dim A	Dim B	Dim C	Dim D	Dim N	Dim W1	Dim W2	Dim W3 (LSL-USL)
24mm	13" Dia	13.00 330	0.059 1.5	512 +0.020/-0.008 13 +0.5/-0.2	0.795 20.2	4.00 100	0.961 +0.078/-0.000 24.4 +2/0	1.197 30.4	0.941 - 0.1.079 23.9 - 27.4

## TO-263AB/D<sup>2</sup>PAK Tape and Reel Data and Package Dimensions, continued

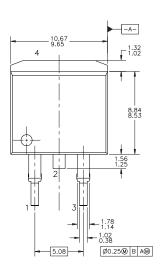
# TO-263AB/D<sup>2</sup>PAK (FS PKG Code 45)

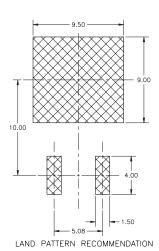


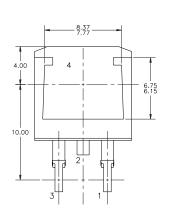


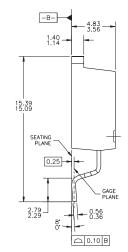
Scale 1:1 on letter size paper Dimensions shown below are in: inches [millimeters]

Part Weight per unit (gram): 1.4378









- NOTES: UNLESS OTHERWISE SPECIFIED

  A) ALL DIMENSIONS ARE IN MILLIMETERS.
  B) STANDARD LEAD FINISH:
  200 MICROINCHES / 5.08 MICROMETERS MIN.
  LEAD/TIN 15/85 ON OLIN 194 COPPER OR
  EQUIVALENT.
  C) MAXIMUM YERTICAL BURR ON HEATSINK NOT
  TO EXCEED 0.003 INCH / 0.05mm.
  D) NO PACKAGE CHIPS, CRACKS OR SURFACE
  IDENTIFICATION ALLOWED AFTER FORMING.
  E) REFERENCE JEDEC, TO—265, ISSUE C,
  VARIATION AB, DATED 2/92.

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### PRODUCT STATUS DEFINITIONS

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Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
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