BLF2425M9LS140

Power LDMOS transistor

AMPLEON

Rev. 2 — 21 October 2016

Product data sheet

1. Product profile

1.1 General description

140 W LDMOS power transistor for Industrial, Scientific and Medical (ISM) applications at frequencies from 2400 MHz to 2500 MHz.

The BLF2425M9LS140 is designed for high power CW applications and is assembled in a high performance ceramic package.

Table 1. Typical performance

Typical RF performance at T_{case} = 25 °C, I_{Dq} = 60 mA in a common source class-AB production test circuit.

Test signal	f	V _{DS}	P _{L(AV)}	Gp	η_{D}
	(MHz)	(V)	(W)	(dB)	(%)
CW	2450	28	140	20	60

1.2 Features and benefits

- High efficiency
- High power gain
- Excellent ruggedness
- Excellent reliability
- Integrated ESD protection
- Designed for broadband operation (2400 MHz to 2500 MHz)
- Internally matched
- Compliant to Directive 2002/95/EC, regarding restriction of hazardous substances (RoHS)

1.3 Applications

Industrial, scientific and medical applications in the frequency range 2400 MHz to 2500 MHz

2. Pinning information

Table 2. Pinning

Pin	Description	Simplified outline	Graphic symbol
1	drain		_
2	gate		ئے ا
3	source	[1]	2 3 sym112

^[1] Connected to flange.

3. Ordering information

Table 3. Ordering information

Type number	Packag	Package		
	Name	Description	Version	
BLF2425M9LS140	-	earless flanged ceramic package; 2 leads	SOT502B	

4. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage		-	65	V
V_{GS}	gate-source voltage		-6	+13	V
T _{stg}	storage temperature		-65	+150	°C
Tj	junction temperature	[1]	-	225	°C

^[1] Continuous use at maximum temperature will affect the reliability, for details refer to the online MTF calculator.

5. Thermal characteristics

Table 5. Thermal characteristics

Symbol	Parameter	Conditions	Тур	Unit
R _{th(j-c)}	thermal resistance from junction to case	T_{case} = 100 °C; P_{L} = 140 W	0.23	K/W

6. Characteristics

Table 6. DC characteristics

 T_i = 25 °C unless otherwise specified.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0 \text{ V}; I_D = 1.806 \text{ mA}$	65	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	V _{DS} = 10 V; I _D = 180.6 mA	1.5	2.08	3.1	V
I _{DSS}	drain leakage current	V _{GS} = 0 V; V _{DS} = 32 V	-	-	4.2	μА
I _{DSX}	drain cut-off current	$V_{GS} = V_{GS(th)} + 3.75 \text{ V};$ $V_{DS} = 10 \text{ V}$	-	36	-	Α
I_{GSS}	gate leakage current	V _{GS} = 11 V; V _{DS} = 0 V	-	-	420	nA
g _{fs}	forward transconductance	V_{DS} = 10 V; I_{D} = 9 A	-	13	-	S
R _{DS(on)}	drain-source on-state resistance	$V_{GS} = V_{GS(th)} + 3.75 \text{ V};$ $I_D = 6.32 \text{ A}$	-	69	-	mΩ

Table 7. RF characteristics

Test signal: CW; f = 2450 MHz; V_{DS} = 28 V; I_{Dq} = 60 mA; T_{case} = 25 °C unless otherwise specified in a class-AB production test circuit.

Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Gp	power gain	P _L = 140 W	17.5	19	-	dB
RLin	input return loss	P _L = 140 W	-	-10	-6	dB
η_{D}	drain efficiency	P _L = 140 W	53	58	-	%

7. Test information

7.1 Ruggedness in class-AB operation

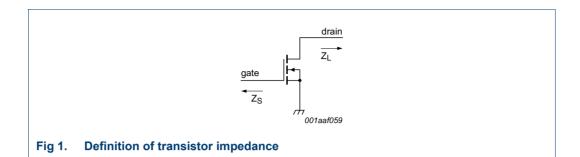
The BLF2425M9LS140 is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 28 V; I_{Dg} = 60 mA; P_L = 140 W (CW); f = 2450 MHz.

7.2 Impedance information

Table 8. Typical impedance

Measured load-pull data. Typical values unless otherwise specified. I_{Dq} = 60 mA; V_{DS} = 28 V. Z_S and Z_L defined in <u>Figure 1</u>.

f	Z _S	Z _L
(MHz)	(Ω)	(Ω)
2400	1.85 – j4.12	1.40 – j1.28
2450	1.81 – j5.00	1.32 – j1.48
2500	4.06 – j2.98	1.22 – j1.66



7.3 Circuit information

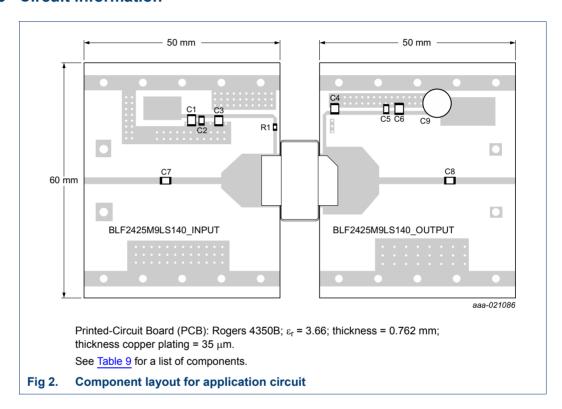


Table 9. List of components For test circuit see Figure 2.

Component	Description	Value	Remarks
C1, C6	multilayer ceramic chip capacitor	10 μF, 50 V	Murata
C2, C5	multilayer ceramic chip capacitor	1 μF, 50 V	Murata
C3, C4, C7, C8	multilayer ceramic chip capacitor	10 pF	ATC 800B
C9	electrolytic capacitor	1000 μF, 100 V	
R1	resistor	5.1 Ω	SMD 0805

- [1] Murata or capacitor of same quality
- [2] American Technical Ceramics type 800B or capacitor of same quality

7.4 Graphical data

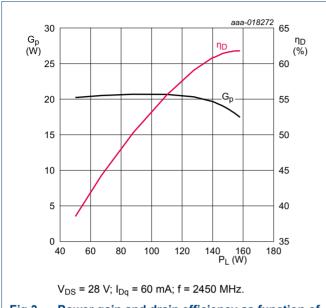


Fig 3. Power gain and drain efficiency as function of output power, typical values

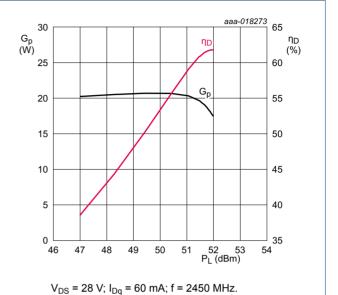
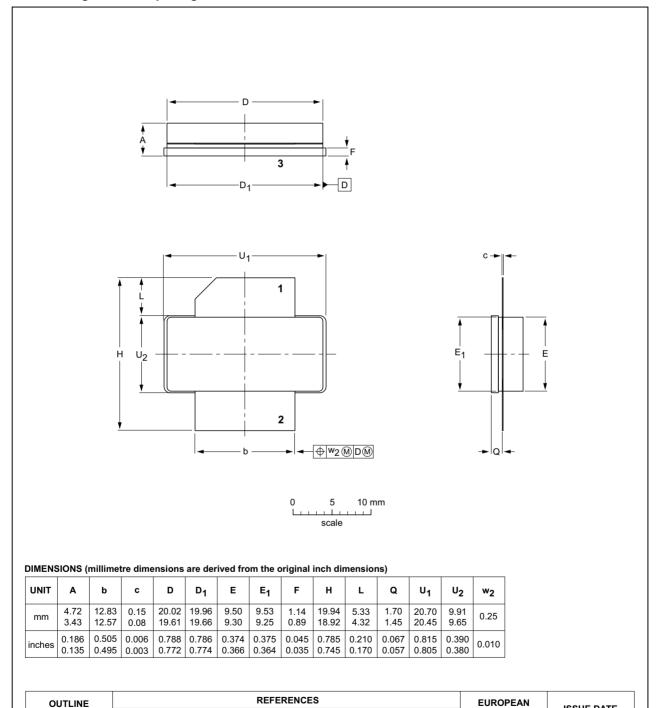


Fig 4. Power gain and drain efficiency as function of output power, typical values

Package outline

Earless flanged ceramic package; 2 leads

SOT502B



Package outline SOT502B Fig 5.

IEC

JEDEC

VERSION

SOT502B

JEITA

ISSUE DATE

07-05-09

12-05-02

PROJECTION

9. Handling information

CAUTION



This device is sensitive to ElectroStatic Discharge (ESD). Observe precautions for handling electrostatic sensitive devices.

Such precautions are described in the ANSI/ESD S20.20, IEC/ST 61340-5, JESD625-A or equivalent standards.

10. Abbreviations

Table 10. Abbreviations

Acronym	Description	
CW	Continuous Wave	
ESD	lectroStatic Discharge	
LDMOS	aterally Diffused Metal-Oxide Semiconductor	
MTF	Median Time to Failure	
SMD	Surface Mounted Device	
VSWR	Voltage Standing Wave Ratio	

11. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes	
BLF2425M9LS140 v.2	20161021	Product data sheet	-	BLF2425M9LS140 v.1	
Modifications:	• Table 4 on page 2: changed V _{GS} minimum value from -0.5 V to -6 V				
BLF2425M9LS140 v.1	20160602	Product data sheet	-	-	

12. Legal information

12.1 Data sheet status

Document status[1][2]	Product status[3]	Definition	
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.	
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.	
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