

# ON Semiconductor

## Is Now

The logo for onsemi, featuring the word "onsemi" in a dark teal, lowercase, sans-serif font. The letter "i" is stylized with a white dot and a teal vertical bar. A small orange triangle is positioned above the top right of the "i". A trademark symbol (TM) is located to the right of the logo.

To learn more about onsemi™, please visit our website at  
[www.onsemi.com](http://www.onsemi.com)

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# MOSFET - Power, N-Channel, UniFET™ II, Ultra FRFET™ 500 V, 2 A, 3 Ω

## FDT4N50NZU

### Description

UniFET II MOSFET is ON Semiconductor's high voltage MOSFET family based on advanced planar stripe and DMOS technology. This advanced MOSFET family has the smallest on-state resistance among the planar MOSFET, and also provides superior switching performance and higher avalanche energy strength. In addition, internal gate-source ESD diode allows UniFET II MOSFET to withstand over 2 kV HBM surge stress. UniFET II Ultra FRFET MOSFET has much superior body diode reverse recovery performance. Its  $t_{rr}$  is less than 50 nsec and the reverse  $dv/dt$  immunity is 20 V/nsec while normal planar MOSFETs have over 200 nsec and 4.5 V/nsec respectively. Therefore UniFET II Ultra FRFET MOSFET can remove additional component and improve system reliability in certain applications that require performance improvement of the MOSFET's body diode. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.

### Features

- Typ.  $R_{DS(on)} = 2.42 \Omega$
- Ultra Low Gate Charge (Typ.  $Q_g = 9.1 \text{ nC}$ )
- 100% Avalanche Tested
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

### Applications

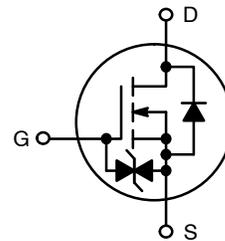
- Computing / Display Power Supplies
- Industrial Power Supplies
- Consumer Power Supplies



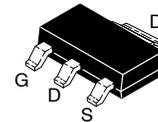
ON Semiconductor®

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$V_{DSS}$	$R_{DS(on)} \text{ MAX}$	$I_D \text{ MAX}$
500 V	3 Ω @ 10 V	2 A

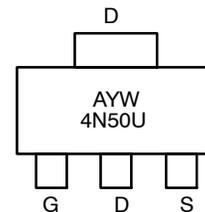


POWER MOSFET



SOT-223  
(TO-261)  
CASE 318E

### MARKING DIAGRAM



A = Assembly Location  
Y = Year  
W = Work Week  
4N50U = Device Code

### ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

# FDT4N50NZU

## ABSOLUTE MAXIMUM RATINGS (T<sub>C</sub> = 25°C, Unless otherwise noted)

Symbol	Parameter	Value	Unit	
V <sub>DSS</sub>	Drain to Source Voltage	500	V	
V <sub>GSS</sub>	Gate to Source Voltage	- DC	±25	V
I <sub>D</sub>	Drain Current	- Continuous (T <sub>C</sub> = 25°C)	2	A
		- Continuous (T <sub>C</sub> = 100°C)	1.2	
I <sub>DM</sub>	Drain Current	- Pulsed (Note 1)	6	A
E <sub>AS</sub>	Single Pulsed Avalanche Energy (Note 2)	46	mJ	
I <sub>AS</sub>	Avalanche Current (Note 2)	2	A	
E <sub>AR</sub>	Repetitive Avalanche Energy (Note 1)	2	mJ	
dv/dt	Peak Diode Recovery dv/dt (Note 3)	20	V/ns	
P <sub>D</sub>	Power Dissipation	(T <sub>C</sub> = 25°C)	2	W
		- Derate Above 25°C	0.02	W/°C
T <sub>J</sub> , T <sub>STG</sub>	Operating and Storage Temperature Range	-55 to +150	°C	
T <sub>L</sub>	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 seconds	300	°C	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

NOTE: Drain current limited by maximum junction temperature.

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2. I<sub>AS</sub> = 2 A, R<sub>G</sub> = 25 Ω, starting T<sub>J</sub> = 25°C.
3. I<sub>SD</sub> ≤ 3 A, di/dt ≤ 100 A/μs, V<sub>DD</sub> ≤ 400 V, starting T<sub>J</sub> = 25°C.

## THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
R <sub>θJA</sub>	Thermal Resistance, Junction to Ambient, (1 in <sup>2</sup> Pad of 2 oz. Copper) Max.	60	°C/W

## PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Packing Method	Reel Size	Tape Width	Quantity
FDT4N50NZU	FDT4N50NZU	SOT-223	Tape & Reel†	330 mm	12 mm	4000 Units

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# FDT4N50NZU

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### OFF CHARACTERISTICS

$BV_{DSS}$	Drain to Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}, T_J = 25^\circ\text{C}$	500			V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 1\ \text{mA}$ , Referenced to $25^\circ\text{C}$		0.55		V/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 500\ \text{V}, V_{GS} = 0\ \text{V}$			1	$\mu\text{A}$
		$V_{DS} = 400\ \text{V}, T_C = 125^\circ\text{C}$		4.6		
$I_{GSS}$	Gate to Body Leakage Current	$V_{GS} = \pm 25\ \text{V}, V_{DS} = 0\ \text{V}$			$\pm 10$	$\mu\text{A}$

### ON CHARACTERISTICS

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	3.5		5.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\ \text{V}, I_D = 1\ \text{A}$		2.42	3	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 20\ \text{V}, I_D = 1\ \text{A}$		1		S

### DYNAMIC CHARACTERISTICS

$C_{iss}$	Input Capacitance	$V_{DS} = 25\ \text{V}, V_{GS} = 0\ \text{V}, f = 1\ \text{MHz}$		476		pF
$C_{oss}$	Output Capacitance			43		pF
$C_{rss}$	Reverse Transfer Capacitance			2.7		pF
$Q_{g(tot)}$	Total Gate Charge at 10 V	$V_{DS} = 400\ \text{V}, I_D = 3\ \text{A}, V_{GS} = 10\ \text{V}$ (Note 4)		9.1		nC
$Q_{gs}$	Gate to Source Gate Charge			2.9		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			3.3		nC

### SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 250\ \text{V}, I_D = 3\ \text{A}, V_{GS} = 10\ \text{V},$ $R_g = 25\ \Omega$ (Note 4)		16		ns
$t_r$	Turn-On Rise Time			16		ns
$t_{d(off)}$	Turn-Off Delay Time			34		ns
$t_f$	Turn-Off Fall Time			15		ns

### SOURCE-DRAIN DIODE CHARACTERISTICS

$I_S$	Maximum Continuous Source to Drain Diode Forward Current			2		A
$I_{SM}$	Maximum Pulsed Source to Drain Diode Forward Current			6		A
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\ \text{V}, I_{SD} = 1\ \text{A}$			1.2	V
$t_{rr}$	Reverse Recovery Time	$V_{DD} = 400\ \text{V}, I_{SD} = 3\ \text{A}, dI_F/dt = 100\ \text{A}/\mu\text{s}$		24		ns
$Q_{rr}$	Reverse Recovery Charge			18		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.

# FDT4N50NZU

## TYPICAL CHARACTERISTICS

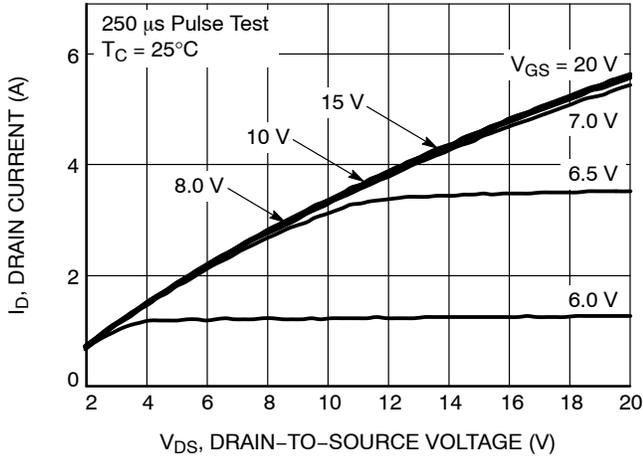


Figure 1. On-Region Characteristics

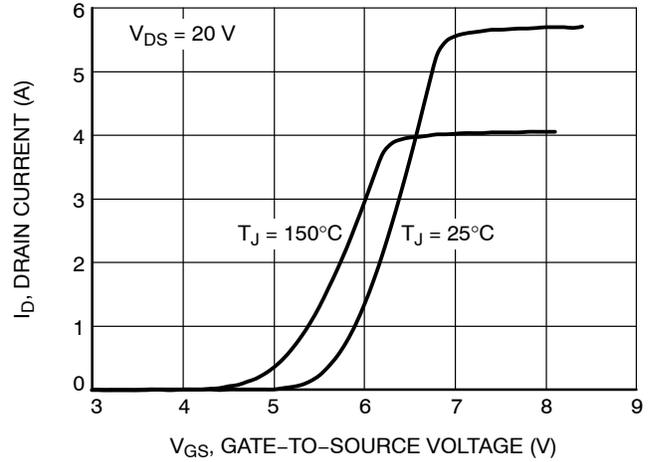


Figure 2. Transfer Characteristics

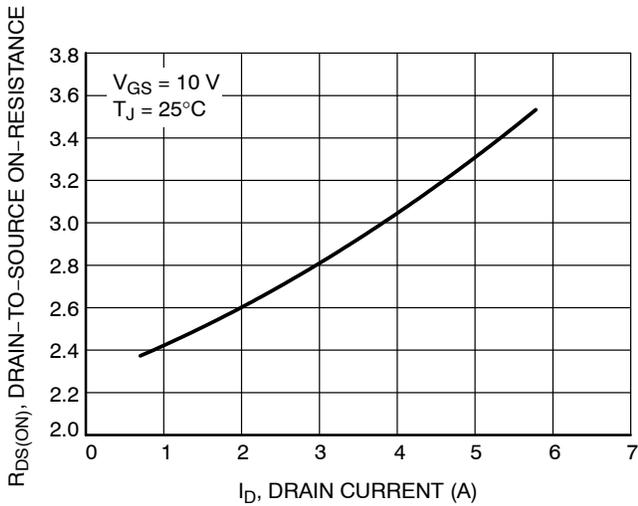


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

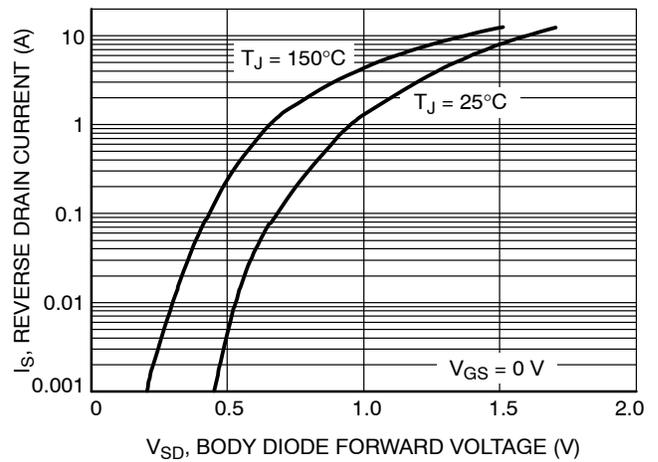


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

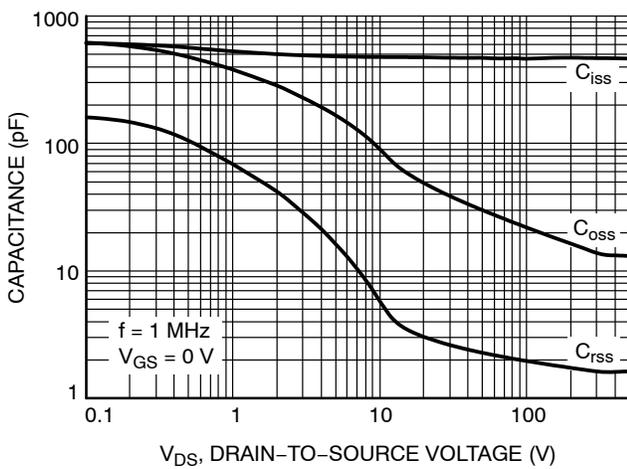


Figure 5. Capacitance Characteristics

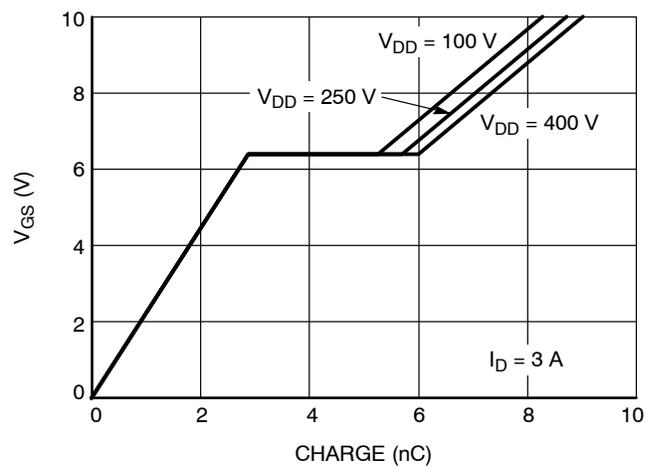
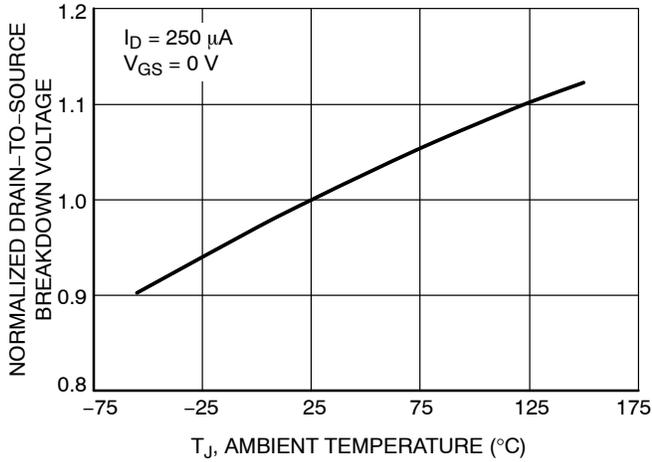


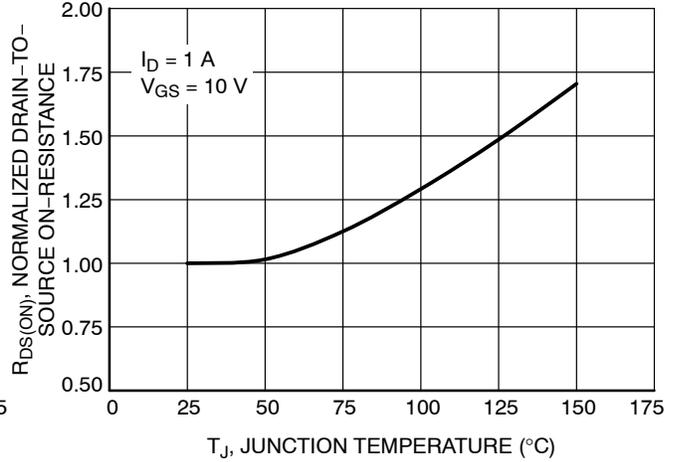
Figure 6. Gate Charge Characteristics

# FDT4N50NZU

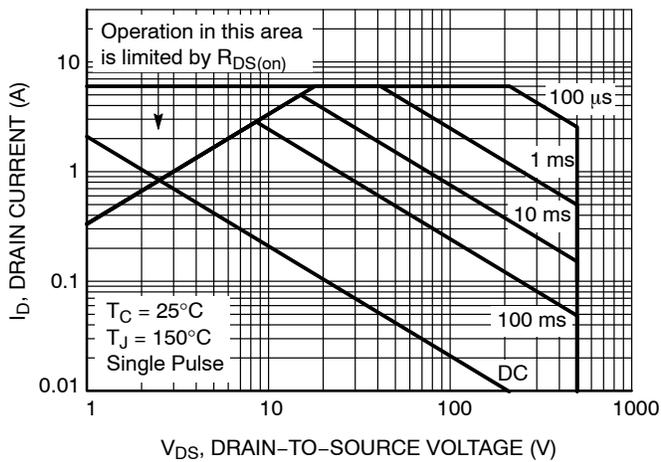
## TYPICAL CHARACTERISTICS



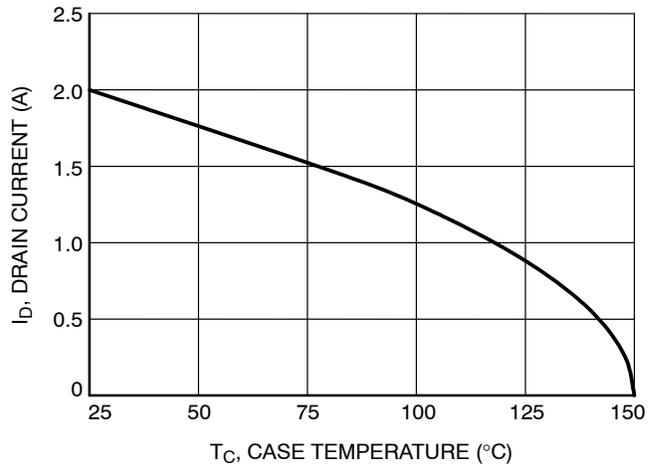
**Figure 7. Breakdown Voltage Variation vs. Temperature**



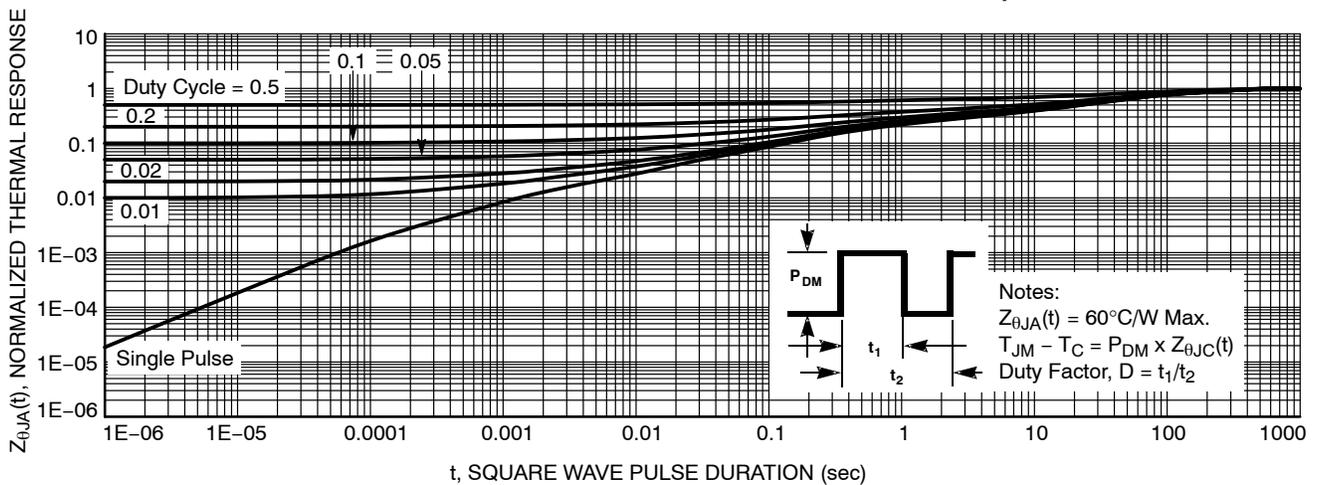
**Figure 8. On-Resistance Variation vs. Temperature**



**Figure 9. Maximum Safe Operating Area**



**Figure 10. Maximum Drain Current vs. Case Temperature**



**Figure 11. Transient Thermal Response**

# FDT4N50NZU

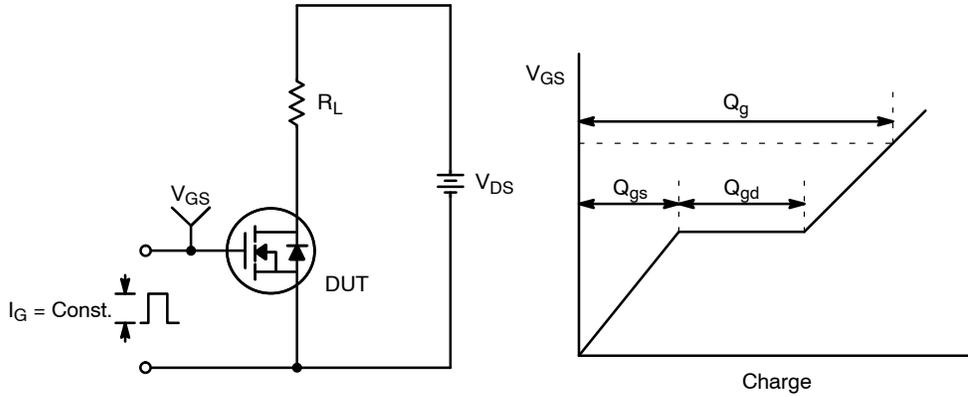


Figure 12. Gate Charge Test Circuit & Waveform

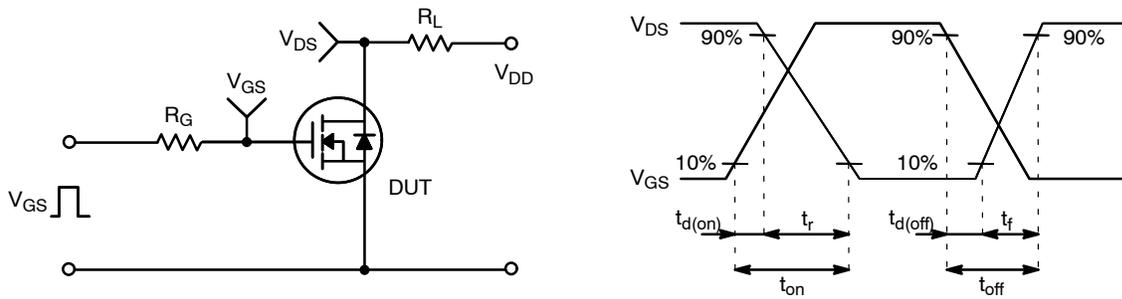


Figure 13. Resistive Switching Test Circuit & Waveforms

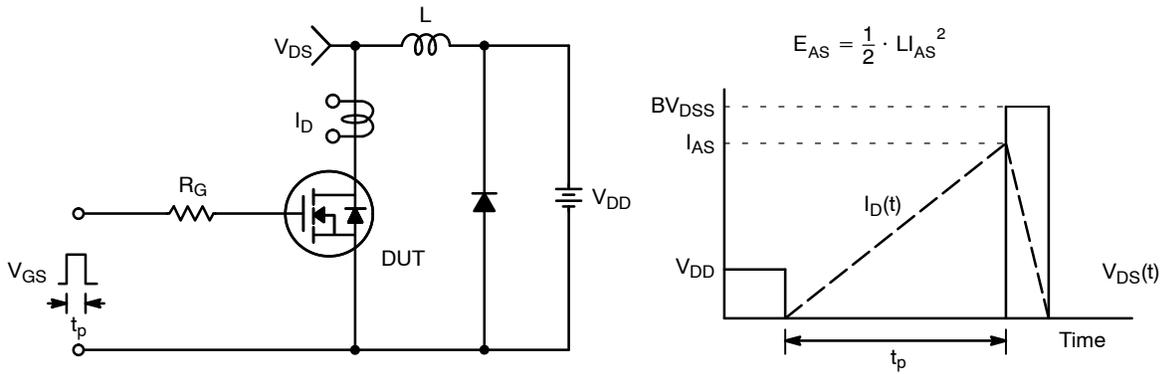
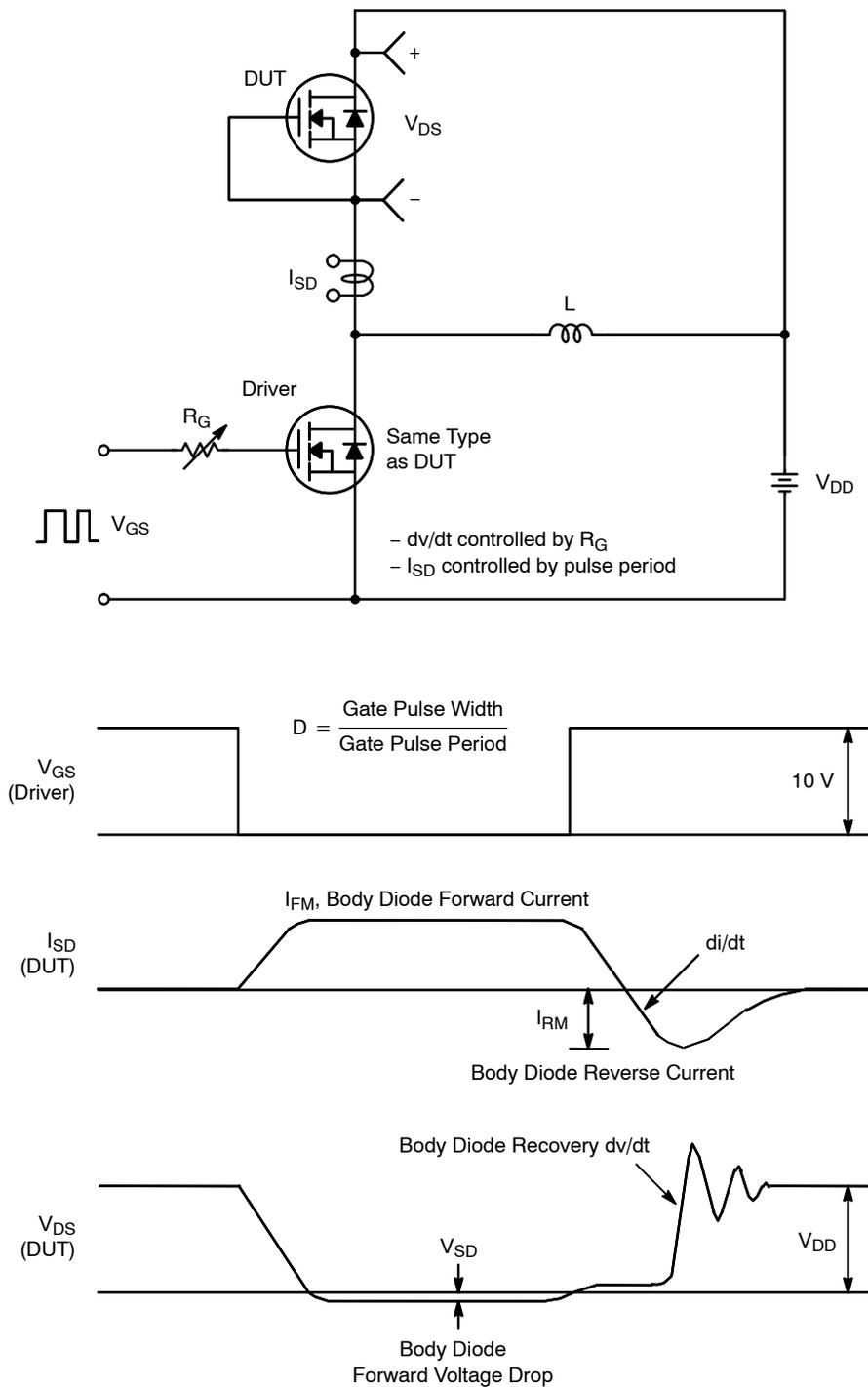


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

# FDT4N50NZU

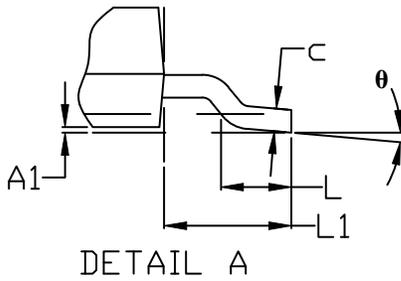
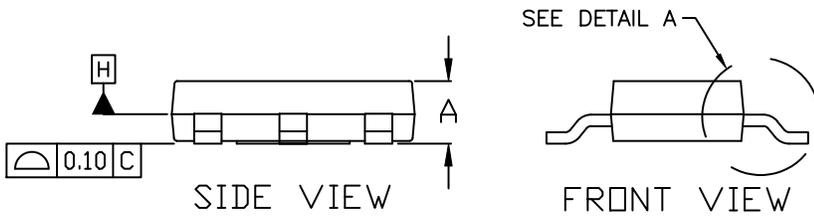
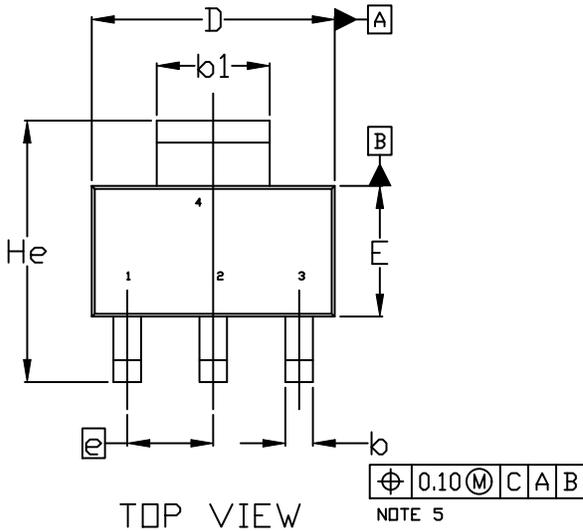


**Figure 15. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms**

# FDT4N50NZU

## PACKAGE DIMENSIONS

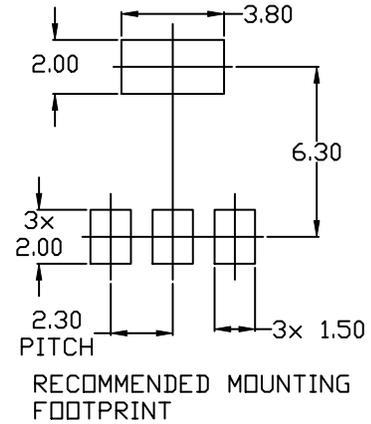
SOT-223 (TO-261)  
CASE 318E-04  
ISSUE R



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.200MM PER SIDE.
4. DATUMS A AND B ARE DETERMINED AT DATUM H.
5. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
6. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	1.50	1.63	1.75
A1	0.02	0.06	0.10
b	0.60	0.75	0.89
b1	2.90	3.06	3.20
c	0.24	0.29	0.35
D	6.30	6.50	6.70
E	3.30	3.50	3.70
e	2.30 BSC		
L	0.20	---	---
L1	1.50	1.75	2.00
He	6.70	7.00	7.30
$\theta$	0°	---	10°



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