MAX77503 I²C-Compatible Serial Interface Implementation Guide

UG6640; Rev 1; 3/19

Abstract

This document serves as a guide to engineers designing with the MAX77503 serial interface. It details the various communication protocols implemented in the 2-wire serial interface block of the MAX77503, as well as some general information on the I²C specification.

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Overview

The MAX77503 I2C communication controller features a Revision 3.0 I2C-compatible, 2-wire serial interface consisting of a bidirectional serial data line (SDA) and a serial clock line (SCL). As shown in the simplified block diagram (Figure 1), the I2C SDA and SCL signals are internally decoded by the devices used to communicate with the top-level control logic. The MAX77503 is a slave-only device that relies on an external bus master to generate SCL. SCL clock rates from 0Hz to 3.4MHz are supported. I2C is an open-drain bus and, therefore, SDA and SCL require pullups.

The MAX77503 implements 7-bit slave addressing. An I2C bus master initiates communication with the slave by issuing a START condition followed by the slave address. The I2C address is factory programmable to one of four options. Any slave addresses not mentioned in the slave address table (Table 1) are not acknowledged.

The device uses 8-bit registers with 8-bit register addressing. It supports standard communication protocols:

- Writing to a single register
- Writing to multiple sequential registers with an automatically incrementing data pointer
- Reading from a single register
- Reading from multiple sequential registers with an automatically incrementing data pointer

For additional information on the I2C protocols, refer to the NXP® I2C bus specification.

Features

- I²C Revision 3.0-Compatible Serial Communications Channel
- 0Hz to 100kHz (Standard Mode)
- 0Hz to 400kHz (Fast Mode)
- 0Hz to 1MHz (Fast Mode Plus)
- 0Hz to 3.4MHz (High-Speed Mode)
- Does not utilize I²C clock stretching

Simplified Block Diagram

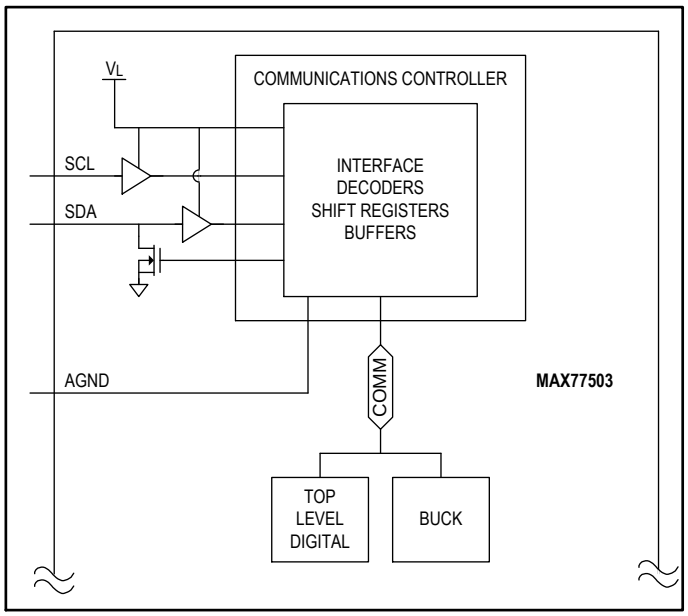

Figure 1. Simplified block diagram.

System Configuration

The I²C bus is a multimaster bus. The maximum number of devices that can attach to the bus is limited only by bus capacitance.

A device on the I²C bus that sends data to the bus is called a transmitter. A device that receives data from the bus is called a receiver. The device that initiates a data transfer and generates the SCL clock signals to control the data transfer is a master. Any device that is being addressed by the master is considered a slave. The MAX77503 I²C-compatible interface operates as a slave on the I²C bus with transmit and receive capabilities.

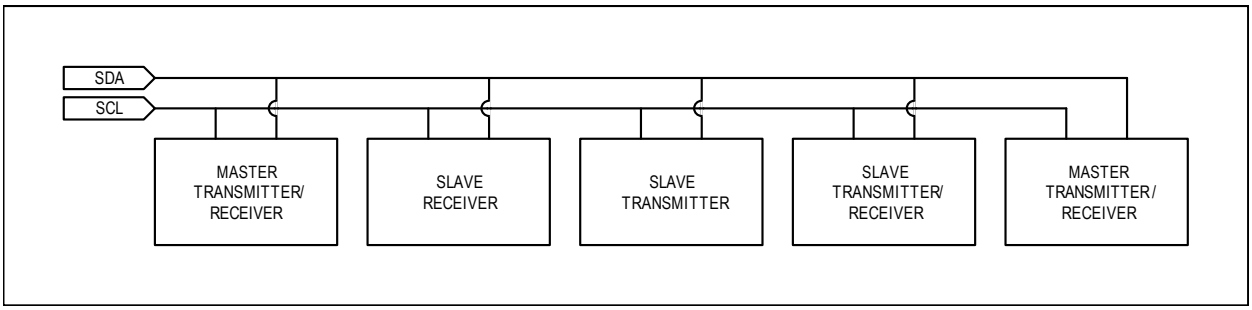

Figure 2. I²C system configuration.

Hardware Implementation and Interface Power

The MAX77503 I²C interface derives its power internally from the V_L regulator. V_L is an integrated 1.8V linear regulator that provides power to the MAX77503 internal digital circuitry as well as to the switching FET gate drivers. The I²C interface is enabled whenever the V_L regulator is on. V_L turns on when either BIASEN or EN is asserted logic high. For more information about the V_L regulator, see the *VL Regulator* section in the MAX77503 device data sheet.

SDA and SCL are high impedance whenever the MAX77503 is shut down. Note that I²C is an open-drain bus and requires pullup resistors. Typical applications place these pullups near the host controller.

Data Transfer

One data bit is transferred during each SCL clock cycle. The data on SDA must remain stable during the high period of the SCL clock pulse. Changes in SDA while SCL is high are control signals. See the *START and STOP Conditions* section. Each transmit sequence is framed by a START (S) condition and a STOP (P) condition. Each data packet is 9 bits long: 8 bits of data followed by an acknowledge bit. Data is transferred with the MSB first.

START and STOP Conditions

When the serial interface is inactive, SDA and SCL idle high. A master device initiates communication by issuing a START condition. A START condition is a high-to-low transition on SDA while SCL high. A STOP condition is a low-to-high transition on SDA while SCL is high. See *Figure 3*.

A START condition from the master signals the beginning of a transmission to the MAX77503. The master terminates the transmission by issuing a not-acknowledge followed by a STOP condition (see the *Acknowledge Bit* section for information on not-acknowledge). The STOP condition frees the bus. To issue a series of commands to the slave, the master can issue repeated START (Sr) commands instead of a STOP command to maintain control of the bus. In general, a repeated START command is functionally equivalent to a regular START command.

When a STOP condition or incorrect address is detected, the MAX77503 internally disconnects SCL from the serial interface until the next START condition, minimizing digital noise and feedthrough.

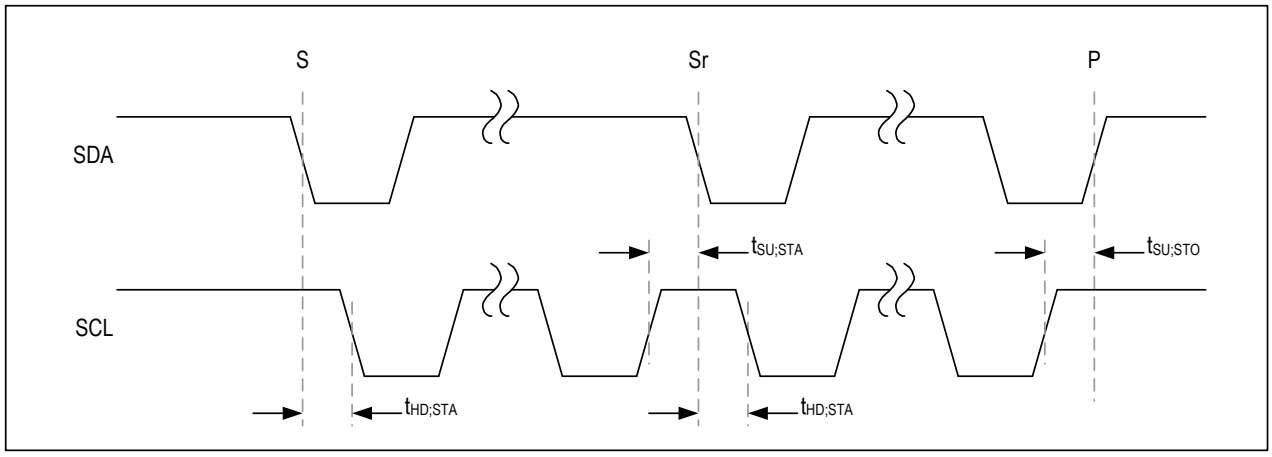

Figure 3. I²C START and STOP conditions.

Acknowledge Bit

Both the I²C bus master and the MAX77503 (slave) generate acknowledge bits when receiving data. The acknowledge bit is the last bit of each 9-bit data packet. To generate an acknowledge (A), the receiving device must pull SDA low before the rising edge of the acknowledge-related clock pulse (ninth pulse) and keep it low during the high period of the clock pulse. See *Figure 4*. To generate a not-acknowledge (NA), the receiving device allows SDA to be pulled high before the rising edge of the acknowledge-related clock pulse and leaves it high during the high period of the clock pulse.

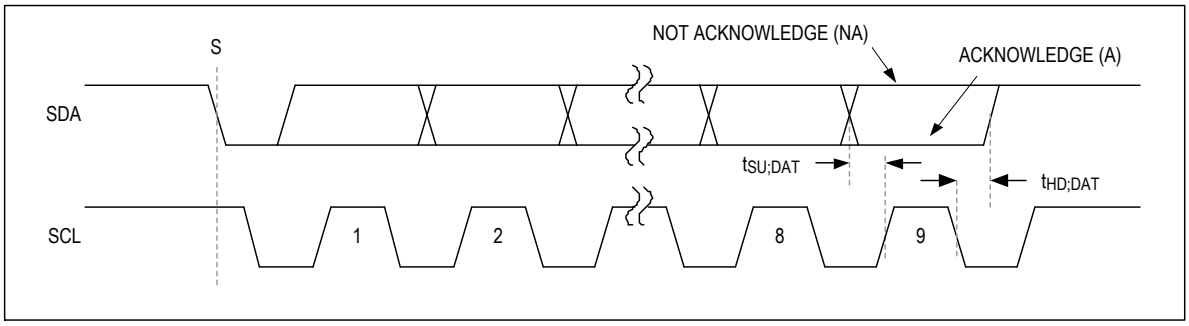

Figure 4. Acknowledge bit.

Monitoring the acknowledge bits allows for detection of unsuccessful data transfers. An unsuccessful data transfer occurs if a receiving device is busy or if a system fault has occurred. In the event of an unsuccessful data transfer, the bus master should reattempt communication at a later time.

The MAX77503 issues an acknowledge for all register addresses in the possible address space even if the particular register does not exist.

Slave Address

The I2C controller implements 7-bit slave addressing. An I2C bus master initiates communication with the slave by issuing a START condition followed by the slave address (*Figure 5)*. The slave address is factory programmable to one of four options (*Table 1*). Refer to the *I2C Serial Interface* and the *Ordering Information* section in the MAX77503 device data sheet for the slave address associated with each orderable part number.

Table 1. MAX77503 Slave Addresses

FACTORY OPTION	7-BIT SLAVE ADDRESS	8-BIT WRITE ADDRESS	8-BIT READ ADDRESS
SID_OTP = 0b00	0x1E, 0b 001 1110	0x3C, 0b0011 1100	0X3D, 0b 0011 1101
SID_OTP = 0b01	0x24, 0b010 0100	0x48, 0b 0100 1000	0x49, 0b 0100 1001
SID_OTP = 0b10	0x37, 0b 011 0111	0x6E, 0b 0110 1110	0x6F, 0b 0110 1111
SID_OTP = 0b11	0x77, 0b 111 0111	0xEE, 0b 1110 1110	0xEF, 0b 1110 1111

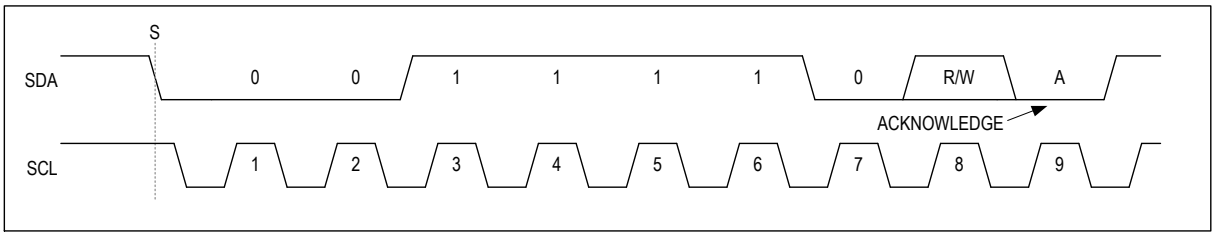

Figure 5. Slave address example.

Clock Stretching

In general, the clock signal generation for the I2C bus is the responsibility of the master device. The I2C specification allows slow slave devices to alter the clock signal by holding down the clock line. The process in which a slave device holds down the clock line is typically called clock stretching. The MAX77503 does not use any form of clock stretching to hold down the clock line.

General Call Address

The MAX77503 does not implement the I2C specification's general call address. If the MAX77503 sees the general call address (0b 0000 0000), it does not issue an acknowledge.

Device ID

The MAX77503 does not support the I2C Device ID feature.

Communication Speed

The MAX77503 is compatible with all four communication speed ranges as defined by the I²C Revision 3.0 specification:

- 0Hz to 100kHz (Standard Mode)
- 0Hz to 400kHz (Fast Mode)
- 0Hz to 1MHz (Fast Mode Plus)
- 0Hz to 3.4MHz (High-Speed Mode)

Operating in standard mode, fast mode, and fast mode plus does not require any special protocols. The main consideration when changing the bus speed through this range is the combination of the bus capacitance and pullup resistors. Higher time constants created by the bus capacitance and pullup resistance (C × R) slow the bus operation. Therefore, when increasing bus speeds, the pullup resistance must be decreased to maintain a reasonable time constant. Refer to the *Pullup Resistor Sizing* section of the I²C bus specification and user manual (available for free online) for detailed guidance on the pullup resistor selection. In general, for bus capacitances of 200pF, a 100kHz bus needs 5.6kΩ pullup resistors, a 400kHz bus needs approximately 1.5kΩ pullup resistors, and a 1MHz bus needs 680Ω pullup resistors. Note that when the open-drain bus is low, the pullup resistor is dissipating power, and lower value pullup resistors dissipate more power (V^2/R).

Operating in high-speed mode requires some special considerations. For a full list of considerations, refer to the I²C bus specification and user manual. Major considerations with respect to the MAX77503 include the following:

- The I²C bus master should use current source pullups to shorten the signal rise time.
- The I²C slave must use a different set of input filters on its SDA and SCL lines to accommodate for the higher bus speed.
- The communication protocols must utilize the high-speed master code.

At power-up and after each STOP condition, the MAX77503 input filters are set for standard mode, fast mode, and fast mode plus (i.e., 0Hz to 1MHz). To switch the input filters for high-speed mode, use the high-speed master code protocols that are described in the *Communication Protocols* section of this implementation guide.

Communication Protocols

The MAX77503 supports both writing and reading from its registers.

Writing to a Single Register

Figure 6 shows the protocol for the I2C master device to write one byte of data to the MAX77503. This protocol is the same as the SMBus specification's write-byte protocol.

The write-byte protocol is as follows:

1. The master sends a START command (S).
2. The master sends the 7-bit slave address followed by a write bit (R/W = 0).
3. The addressed slave asserts an acknowledge (A) by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a data byte.
7. The slave updates with the new data
8. The slave acknowledges or not-acknowledges the data byte. The next rising edge on SDA loads the data byte into its target register and the data becomes active.
9. The master sends a STOP condition (P) or a repeated START condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.

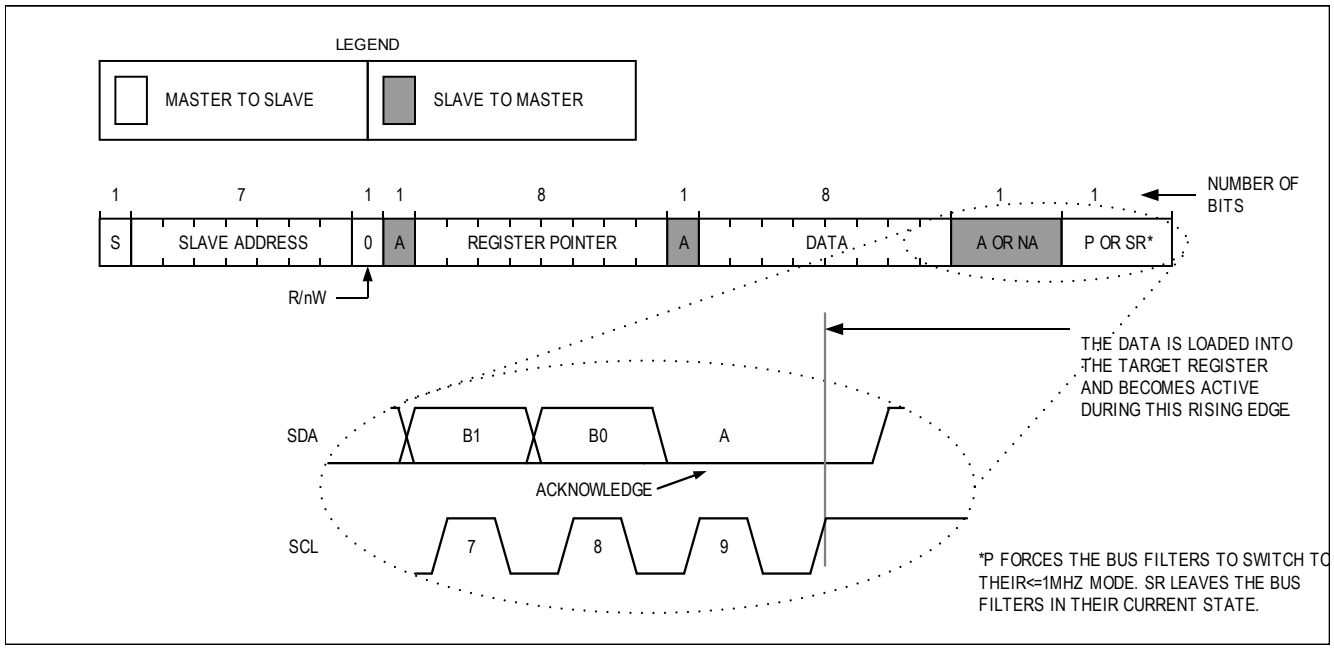

Figure 6. Writing to a single register.

Writing Multiple Bytes to Sequential Registers

Figure 7 shows the protocol for writing to sequential registers. This protocol is similar to the write-byte protocol above, except the master continues to write after it receives the first byte of data. When the master is done writing it issues a STOP or repeated START.

The writing to sequential registers protocol is as follows:

1. The master sends a START command (S).
2. The master sends the 7-bit slave address followed by a write bit (R/$\overline{W}$ = 0).
3. The addressed slave asserts an acknowledge (A) by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a data byte.
7. The slave acknowledges the data byte. The next rising edge on SDA loads the data byte into its target register, and the data becomes active.
8. Steps 6 to 7 are repeated as many times as the master requires.
9. During the last acknowledge-related clock pulse, the master can issue an acknowledge or a not-acknowledge.
10. The master sends a STOP condition (P) or a repeated START condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.

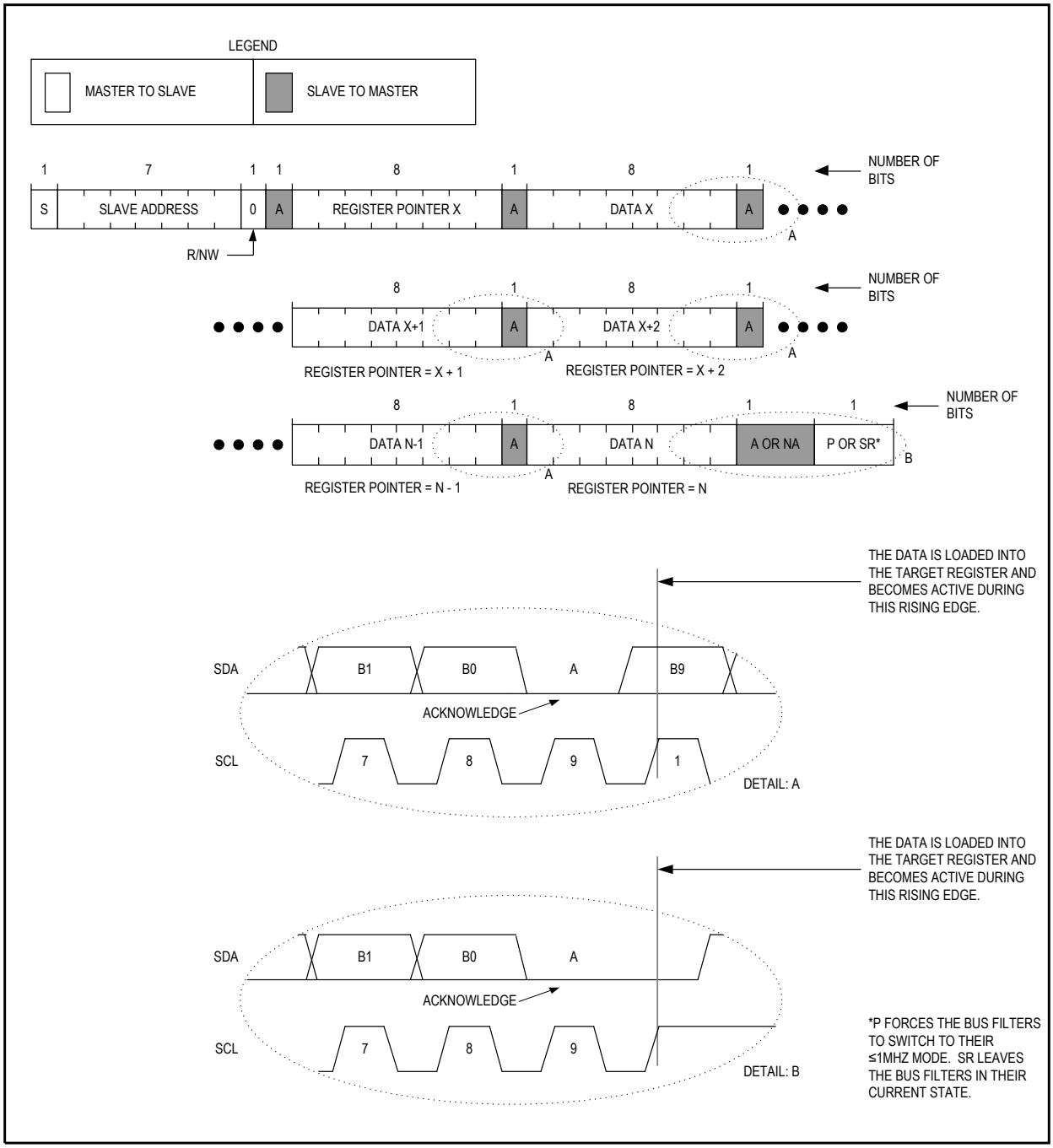

Figure 7. Writing sequential registers.

Reading from a Single Register

Figure 8 shows the protocol for the I2C master device to read one byte of data from the MAX77503. This protocol is the same as the SMBus specification's read-byte protocol.

The read byte protocol is as follows:

1. The master sends a START command (S).
2. The master sends the 7-bit slave address followed by a write bit (R/$\overline{W}$ = 0).
3. The addressed slave asserts an acknowledge (A) by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a repeated START command (Sr).
7. The master sends the 7-bit slave address followed by a read bit (R/$\overline{W}$ = 1).
8. The addressed slave asserts an acknowledge by pulling SDA low.
9. The addressed slave places 8 bits of data on the bus from the location specified by the register pointer.
10. The master issues a not-acknowledge (nA).
11. The master sends a STOP condition (P) or a repeated START condition (Sr). Issuing a P ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.

Note that when the MAX77503 receives a STOP, it does not modify the register pointer.

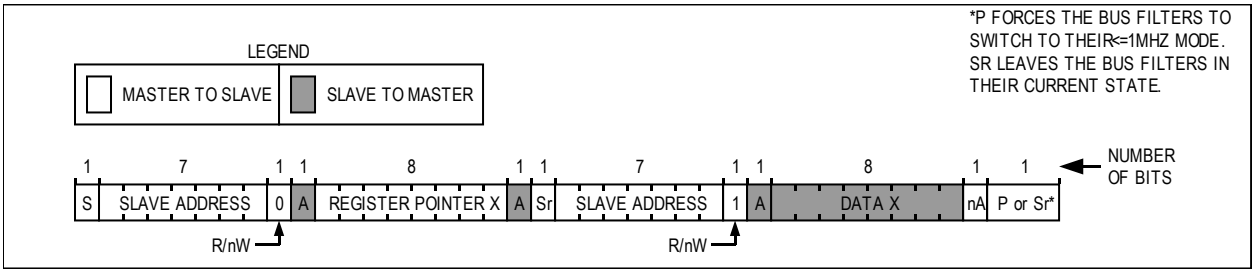

Figure 8. Reading from a single register.

Reading from Sequential Registers

Figure 9 shows the protocol for reading from sequential registers. This protocol is similar to the read-byte protocol, but with this one, the master issues an acknowledge to signal the slave that it wants more data. When the master has all the data it requires, it issues a not-acknowledge (nA) and a STOP (P) to end the transmission.

The continuous read from sequential registers protocol is as follows:

1. The master sends a START command (S).
2. The master sends the 7-bit slave address followed by a write bit (R/$\overline{W}$ = 0).
3. The addressed slave asserts an acknowledge (A) by pulling SDA low.
4. The master sends an 8-bit register pointer.
5. The slave acknowledges the register pointer.
6. The master sends a repeated START command (Sr).
7. The master sends the 7-bit slave address followed by a read bit (R/$\overline{W}$ = 1). When reading the RTC timekeeping registers, secondary buffers are loaded with the timekeeping register data during this operation.
8. The addressed slave asserts an acknowledge by pulling SDA low.
9. The addressed slave places 8 bits of data on the bus from the location specified by the register pointer.
10. The master issues an acknowledge (A) signaling the slave that it wishes to receive more data.
11. Steps 9 to 10 are repeated as many times as the master requires. Following the last byte of data, the master must issue a not-acknowledge (nA) to signal that it wishes to stop receiving data.
12. The master sends a STOP condition (P) or a repeated START condition (Sr). Issuing a STOP (P) ensures that the bus input filters are set for 1MHz or slower operation. Issuing an Sr leaves the bus input filters in their current state.

Note that when the MAX77503 receives a STOP, it does not modify the register pointer.

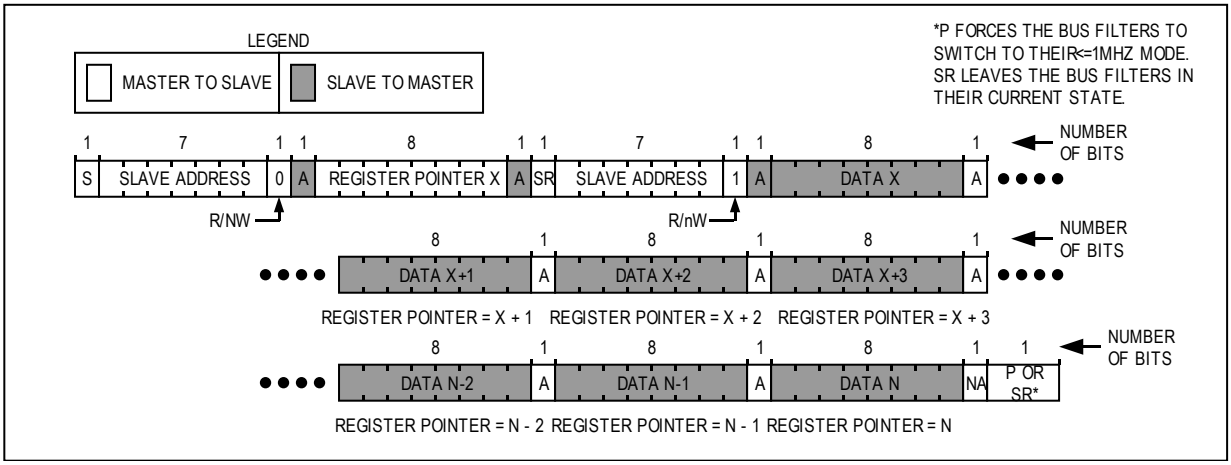

Figure 9. Reading from multiple registers.

Engaging High-Speed Mode for Operations Up to 3.4MHz

Figure 10 shows the protocol for engaging high-speed mode operation. High-speed mode allows for bus operating speeds of up to 3.4MHz.

The high-speed mode protocol is as follows:

1. Begin the protocol while operating at a bus speed of 1MHz or lower.
2. The master sends a START command (S).
3. The master sends the 8-bit master code of 0b0000 1XXX where 0bXXX are don't-care bits.
4. The addressed slave issues a not-acknowledge (nA).
5. The master can now increase its bus speed up to 3.4MHz and issue any read/write operation.

The master can continue to issue high-speed read/write operations until a stop (P) is issued. To continue operations in high-speed mode, use repeated START (Sr).

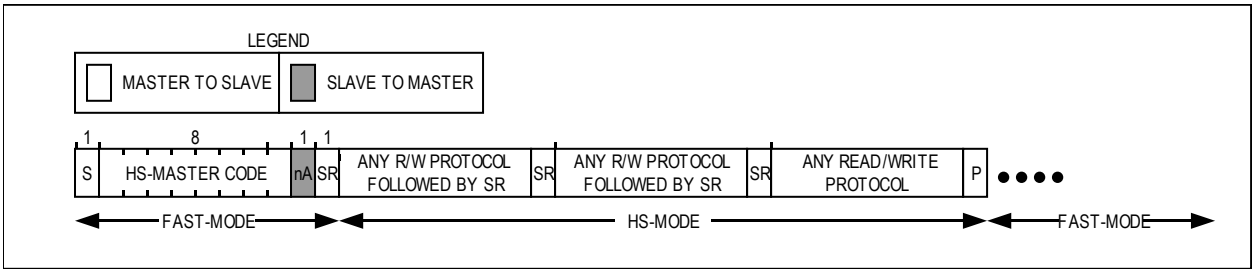

Figure 10. Engaging high-speed mode.

Revision History

REV NUMBER	REV DATE	DESCRIPTION	PAGES CHANGED
0	3/18	Initial release	—
1	3/19	Updated Figure 7.	13