



Keywords: No-opto flyback, synchronous flyback converter, peak current mode controller

APPLICATION NOTE 6394

HOW TO DESIGN A NO-OPTO FLYBACK CONVERTER WITH SECONDARY-SIDE SYNCHRONOUS RECTIFICATION

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Abstract: This application note explains the procedure for designing a no-opto flyback converter with secondary-side synchronous rectification using the MAX17690 and MAX17606 to achieve high efficiency and better thermal management.

Introduction

Using a flyback converter for low- and medium-power applications is the preferred design choice due to the flyback converter's simplicity and low cost. However, in isolated applications, the use of optocoupler or auxiliary winding for voltage feedback across the isolation boundary increases the number of components, and design complexity. The [MAX17690](#), a no-opto flyback controller, eliminates the optocoupler or auxiliary winding, and achieves $\pm 5\%$ output voltage regulation over line, load, and temperature variations.

In low output voltage and high output current applications, the diode on the secondary side of the flyback converter dissipates a significant amount of power; this power loss reduces the converter's efficiency. The [MAX17606](#), a secondary-side synchronous MOSFET driver, helps in replacing the secondary diode with a MOSFET. This improves the efficiency and simplifies thermal management.

This application note provides the step-by-step procedure for designing the different components of the MAX17690 + MAX17606-based synchronous flyback design.

Design Example

The following specification is selected to demonstrate the design calculations for the MAX17690 and the MAX17606-based flyback converter. Figure 1 shows the typical application circuit for this application.

D_{max} is the maximum operating duty cycle. If the calculated duty cycle is > 0.65 , then choose D_{max} to be 0.65p.u.

Switching Frequency Selection

Use the below equations to calculate the maximum possible switching frequency, f_{sw} .

$$f_{sw} \leq \left(\frac{600000 \times D_{max} \times V_{INmin}}{V_{INmax}} \right)$$

$$f_{sw} \leq \left(\frac{600000 \times 0.5 \times 18}{36} \right)$$

$$f_{sw} \leq 150\text{kHz}$$

For the present application, the switching frequency is selected as 150kHz. The R_{RT} is calculated for the selected f_{sw} .

$$R_{RT} = \frac{5 \times 10^9}{F_{sw}}$$

$$R_{RT} = \frac{5 \times 10^9}{150000} = 33.3\text{k}$$

A standard resistor of 33.2k is selected.

Transformer Magnetizing Inductance and Turns Ratio

The MAX17690 and the MAX17606 are specifically designed for the isolated flyback converters operating in Discontinuous Conduction Mode (DCM) or Border Conduction Mode (BCM). Use the below equations to select the transformer magnetizing inductance (L_{MAG}) for DCM operation.

$$L_{MAG} = \frac{0.43 \times (V_{INmin} \times D_{max})^2}{V_{OUT} \times I_{OUT} \times f_{sw}}$$

$$L_{MAG} = \frac{0.43 \times (18 \times 0.5)^2}{5 \times 1 \times 150000} = 46.4\mu\text{H}$$

For the present design L_{MAG} is selected to be 46.4uH, and the allowable tolerance on the L_{MAG} is $\pm 10\%$. For the selected f_{sw} and the L_{MAG} , recalculate the D_{max} using the equations below:

$$D_{max} = \frac{\sqrt{2.3 \times L_{MAG} \times V_{OUT} \times I_{OUT} \times f_{sw}}}{V_{INmin}}$$

$$D_{max} = \frac{\sqrt{2.3 \times 46.5 \times 10^{-6} \times 5 \times 1 \times 150000}}{18} = 0.5\text{p.u}$$

The MAX17606 programs the turn-off trip point and decides the instant at which the secondary MOSFET is

turned off. Due to the variation on the turn-off point, the secondary MOSFET conduction time changes. To guarantee the DCM operation of the converter for the variations on the turn-off threshold, magnetizing inductance ($\pm 10\%$), and the switching frequency ($\pm 6\%$), select the turns-ratio (K) based on the below equations:

$$K = \frac{N_s}{N_p} = \frac{0.64 \times V_{OUT} \times (1-D)}{D_{max} \times V_{INmin}}$$

$$K = \frac{N_s}{N_p} = \frac{0.64 \times 5 \times (1-0.5)}{0.5 \times 18} = 0.177$$

For the present design, K is chosen as $0.18 \pm 1\%$.

Selection of Current-Sense Resistor

For the selected L_{MAG} and f_{SW} , the primary peak current is calculated using the equation below:

$$I_{LIM} = \sqrt{\frac{2.3 \times V_{OUT} \times I_{OUT}}{L_{MAG} \times f_{sw}}} = 1.28A$$

The threshold voltage of the peak current-limit comparator is set at 100mV (typ) and 90mV (min). With the expected tolerance of $\pm 10\%$ on the L_{MAG} and the $\pm 6\%$ on the f_{SW} , to deliver the full-load power in all operating conditions, use the equations given below to calculate the current-sense resistor (R_{CS}) value.

$$R_{CS} = \frac{0.08}{I_{LIM}}$$

$$R_{CS} = \frac{0.08}{1.28} = 62.5m$$

A standard resistor of $62.5m \pm 1\%$ is selected.

Selection of EN/UVLO and OVI Resistive Divider

The values of the resistor-divider can be selected so that the EN/UVLO pin voltage exceeds the 1.215V (typ) turn-on threshold at the desired input bus voltage (V_{START}). The same resistor-divider can be modified with an additional resistor (R_{OVI}) to implement input overvoltage (V_{OVI}) protection in addition to the EN/UVLO functionality, as shown in **Figure 1**. When the voltage at the OVI pin exceeds 1.215V (typ), the device stops switching. With the preselected value of 10k for R_{OVI} :

$$R_{EN} = R_{OVI} \left(\frac{V_{OVI}}{V_{START}} - 1 \right)$$

For the present application V_{START} and V_{OVI} are selected to be 17.5V and 36.2V.

$$R_{EN} = 10 \times 1000 \times \left(\frac{36.2}{17.5} - 1 \right) = 10.7k\Omega$$

$$R_{EN-TOP} = (R_{EN} + R_{OVI}) \times \left(\frac{V_{START}}{1.215} - 1 \right)$$

$$R_{EN-TOP} = (10000 + 10700) \times \left(\frac{17.5}{1.215} - 1 \right) = 277k\Omega$$

A standard resistor of 280k is selected.

Selection of R_{TC} Resistor

Since in this design the secondary MOSFET is always programmed to conduct at the sampling instant of the output voltage, there is no need to compensate the diode forward-voltage temp coefficient on the primary. For details on how to select the R_{TC} resistor for the other applications, refer to the MAX17690 IC data sheet.

$$R_{TC} = \text{OPEN}$$

Selection of R_{IN} , R_{FB} , and R_{SET} Resistor

The R_{IN} , R_{FB} , and the R_{SET} resistors program the output voltage and sampling instant for proper sampling of the output voltage. Use the below equations to calculate these values:

$$R_{SET} = 10k\Omega, R_{FB} = \left(\frac{V_{OUT} \times R_{SET}}{K} \right) \text{ and } R_{IN} = 0.6 \times R_{FB}$$

$$R_{FB} = \left(\frac{5 \times 10000}{0.18} \right) = 277.7k\Omega$$

Use the combination of standard resistors 274k and 3.74k to meet the required R_{FB} value of 277.7k .

$$R_{IN} = 0.6 \times 277.7 \times 10^3 = 166.6k$$

A standard resistor of 165k is selected for this application.

In practice, due to the drop across the secondary leakage inductance of the transformer, the measured output voltage can deviate from the target output voltage. Use the below equations to readjust the output voltage to the desired value:

$$R_{FB(new)} = \frac{V_O(\text{Target})}{V_O(\text{Measured})} \times R_{FB}$$

$$R_{IN(new)} = 0.6 \times R_{FB(new)}$$

Soft-Start Capacitor Selection

For the desired soft-start time($t_{SS} = 10ms$), the SS capacitor is selected using:

$$C_{SS} = 5 \times t_{SS} = 50nF$$

The soft-start capacitor selected is 47nF for the present design.

Selection of R_{VCM} Resistor

The resistor connected between the VCM pin and SGND is used to scale the common-mode voltage of internal circuits within the operating range. Follow the below steps to select the R_{VCM} resistor value for proper operation.

1. Calculate the internal scaling factor:

$$Kc = \frac{100\mu \times (1-D)}{3 \times f_{sw} \times 10^{-12}}$$

$$Kc = \frac{100 \times 10^{-6} \times (1-0.5)}{3 \times 150000 \times 10^{-12}} = 111.1 = 111.1$$

2. From the below table, choose the row that has the equal or higher value for Kc with respect to the calculated Kc in Step 1. Select the row with Kc = 160 for the present design.

Kc	R_{VCM} ()
640	0
320	75k
160	124k
80	220k
40	Open

3. Select the resistor value from the corresponding row as the R_{VCM} ($R_{VCM}=124k$).

Primary MOSFET Selection

MOSFET selection criteria includes maximum drain voltage, primary peak/RMS current, the on-state resistance ($R_{DS(ON)}$), total gate charge (Q_G), the parasitic capacitance (C_{OSS}), and the maximum allowable power dissipation of the package without exceeding the junction temperature limits. The voltage seen by the MOSFET drain is the sum of the input voltage, the reflected secondary voltage on the transformer primary, and the leakage inductance spike. The MOSFET's absolute maximum V_{DS} rating must be higher than the worst-case drain voltage.

$$V_{DSmax} = V_{INmax} + \left(\frac{2.5 \times (V_{OUT})}{K} \right)$$

$$V_{DSmax} = 36 + \left(\frac{2.5 \times (5)}{0.18} \right) = 105.4V$$

The "RCD and RC Snubber Circuit" section covers the selection of snubber components to limit the drain-to-source voltage to V_{DSmax} value selected in the above equation.

The RMS current in the MOSFET can be calculated using the below equation:

$$I_{MOSFET(RMS)} = \sqrt{I_{LIM}^2 \times D / 3}$$

$$I_{\text{MOSFET(RMS)}} = \sqrt{1.28^2 \times 0.5 / 3}$$

$$I_{\text{MOSFET(RMS)}} = 0.522\text{A}$$

In the present application, the FDMS86252 part is selected as the primary MOSFET to achieve high efficiency. From the MOSFET data sheet $R_{\text{DS(ON)}}$ value, the conduction loss in the MOSFET can be calculated using the equation given below:

$$P_{\text{Conduction}} = I_{\text{MOSFET}}^2(\text{RMS}) \times R_{\text{DS(ON)}}$$

$$P_{\text{Conduction}} = 0.522^2 \times 48 \times 10^{-3} = 13\text{mW}$$

For the selected MOSFET, the equation below gives another loss component, switching loss.

$$P_{\text{COSS}} = \frac{1}{2} \times C_{\text{oss}} \times (V_{\text{DS}})^2 \times f_{\text{sw}}$$

From the MOSFET data sheet, the C_{OSS} at 100V is given as 60pF.

$$P_{\text{COSS}} = \frac{1}{2} \times 60 \times 10^{-12} \times (105.4)^2 \times 150000 = 50\text{mW}$$

It is important to verify the maximum junction temperature of the MOSFET for the calculated losses using the below equation.

$$T_{\text{J}} = T_{\text{A}} + P_{\text{MOSFET}} \times R_{\text{TH(JA)}}$$

where T_{A} is the ambient temperature, the $R_{\text{TH(JA)}}$ is the MOSFET thermal resistance from junction-to-ambient, and the P_{MOSFET} is the total MOSFET losses.

In this high-efficiency design, for the selected MOSFET the total losses are a very small portion of output power, and its junction temperature is within the limits.

Use the below equation to calculate the IC driver losses for the selected MOSFET:

$$P_{\text{INTVCC}} = I_{\text{TVCC}} \times Q_{\text{G}} \times f_{\text{sw}}$$

$$P_{\text{INTVCC}} = 7 \times 8 \times 10^{-9} \times 150000 = 8.4\text{mW}$$

Secondary MOSFET Selection

The voltage seen by the MOSFET drain is the sum of the output voltage and the reflected input voltage on the transformer secondary. Make sure that the maximum secondary V_{DS} voltage, when the primary MOSFET is turned ON is less than 60V. The MOSFET's absolute maximum V_{DS} rating must be higher than the worst-case drain voltage.

$$V_{\text{DSmax}} = V_{\text{OUT}} + (V_{\text{INmax}} \times K)$$

$$V_{DSmax} = 5 + (36 \times 0.18) = 11.48V$$

For the secondary MOSFET, the RMS current equation is given below:

$$I_{sy_MOSFET} = \sqrt{\frac{2 \times I_{OUT} \times I_{secpk}}{3}}$$

For the stable operation of MAX17690 + MAX17606-based designs over the entire operating conditions, it is recommended to select the $R_{DS(ON)}$ of the secondary MOSFET such that the voltage across the MOSFET (at room temperature) is greater than the 100mV when the peak secondary current is flowing through the MOSFET.

$$I_{secpk} = I_{LIM} / K$$

$$I_{secpk} = 1.28 / 0.18 = 7.1A$$

$$R_{DS(ON)} = 0.1 / 7.1 = 14m\Omega$$

In the present application, STL51N3LLH5 is selected as the secondary MOSFET.

The losses in the secondary MOSFET can be calculated using the loss equations provided in the primary MOSFET selection section and the maxim junction temperature can be verified to be within limits.

RCD and RC Snubber Circuit

Ideally, the primary external MOSFET experiences a drain-source voltage stress equal to the sum of the input voltage and reflected voltage across the primary winding during the OFF period of the MOSFET. In practice, parasitic inductors and capacitors in the circuit, such as leakage inductance of the flyback transformer, cause voltage overshoot and ringing in addition to the ideally expected voltage stress. Snubber circuits are used to limit the voltage overshoots to safe levels within the voltage rating of the external MOSFET. The typical RCD snubber circuit and the relevant waveforms are shown in **Figure 2** and **Figure 3**.

Use the following equations to calculate the snubber components:

$$P_{snub} = 0.833 \times L_{lk} \times (I_{LIM})^2 \times f_{sw}$$

$$R_{snub} = \frac{6.25 \times (V_{OUT})^2}{K^2 \times P_{snub}}$$

$$C_{snub} = \frac{2 \times L_{lk} \times I_{LIM}^2 \times K^2}{(V_{OUT})^2}$$

where $K = \frac{N_s}{N_p}$

The voltage rating of the snubber diode is:

$$V_{D2} = V_{inmax} + (2.5 \times \frac{V_{OUT}}{K})$$

The RC component values are selected to be 60.4k , 2.2nF.

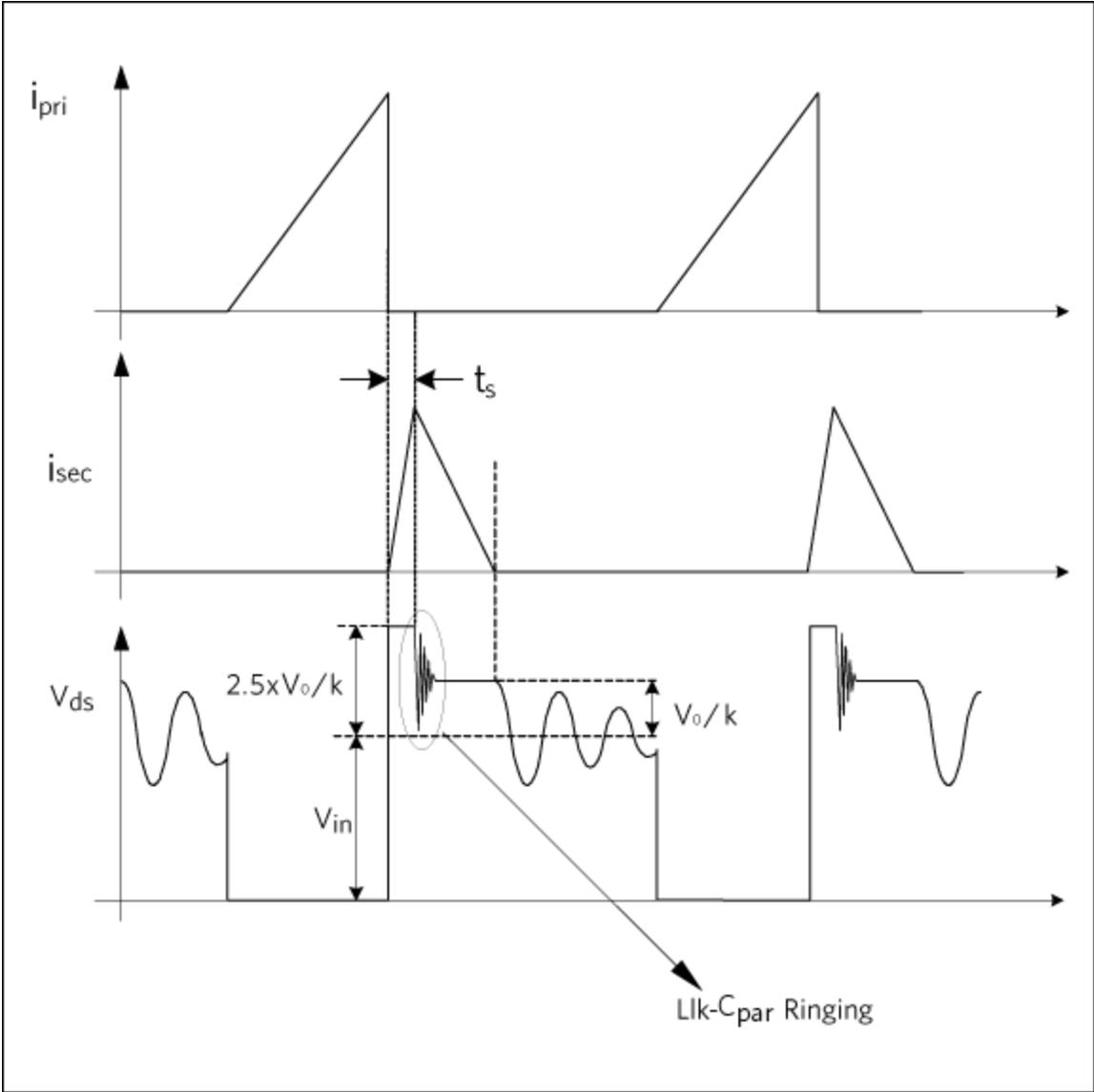


Figure 2. Waveforms with RCD clamp.

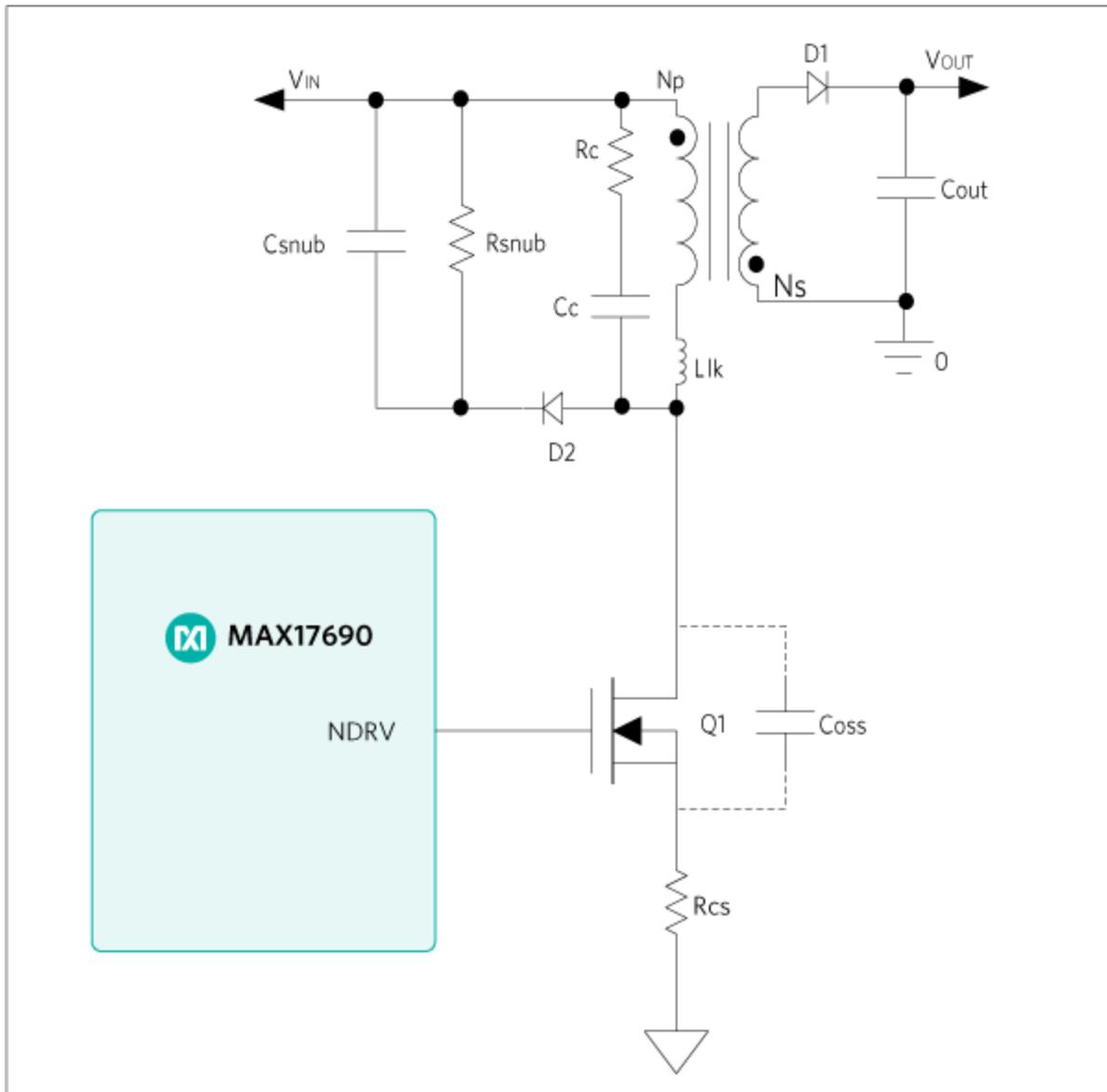


Figure 3. RC and RCD clamp circuitry.

The RCD clamp only limits the maximum voltage stress on the primary MOSFET, but the ringing due to interaction between L_{lk} and C_{par} on the drain node is not damped. Because the MAX17690 uses the drain voltage information to sample the output voltage, it is important to damp this ringing within 350ns from the NDRV falling. In designs where this ringing is dominant, an RC snubber placed across the transformer primary winding damps this ringing. Use the following steps for designing an effective RC snubber:

1. Measure the ringing time period from the drain node voltage.

$$t_1 = 2\pi\sqrt{L_{lk} \times C_{par}}$$

2. Add a test capacitance starting with 100pF until the time period of the ringing is 1.5 to 2 x t_1 . For the added capacitance C_D , measure the new ringing time period:

$$t_2 = 2\pi\sqrt{L_{lk} \times (C_{par} + C_D)}$$

3. Use the following equation to calculate the drain node capacitance:

$$C_{par} = \frac{C_D}{\left(\frac{t_2}{t_1}\right)^2 - 1}$$

4. Use the following equation to calculate the leakage inductance:

$$L_{lk} = \frac{t_1^2}{(4 \times \pi^2 \times C_{par})}$$

5. Now, use the following equations to calculate the RC snubber values:

$$C_c = 1.5 \text{ to } 2 \times \text{the } C_{par}$$

$$R_c = \sqrt{\frac{L_{lk}}{C_{par}}}$$

The R_c and C_c values are selected to be 47 Ω and 220pF.

Selection of RTOFF Resistor

The MAX17606 IC data sheet explains the details of the R_{TOFF} requirement and the selection. For a new design, assume the minimum blanking time required to be 1.5 μ s. The value of the R_{TOFF} for the corresponding blanking time is 145k Ω . The standard resistor of 147k Ω can be selected for most of the designs to check the ringing time and to determine the actual value of R_{TOFF} .

Based on the actual ringing time (t_R) on the secondary MOSFET drain node shown in **Figure 4**, the new value of R_{TOFF} can be selected using the equation below:

$$R_{TOFF} = \frac{t_R - 13}{10.25}, \text{ where } R_{TOFF} \text{ is in k}\Omega \text{ and } t_R \text{ is in ns.}$$

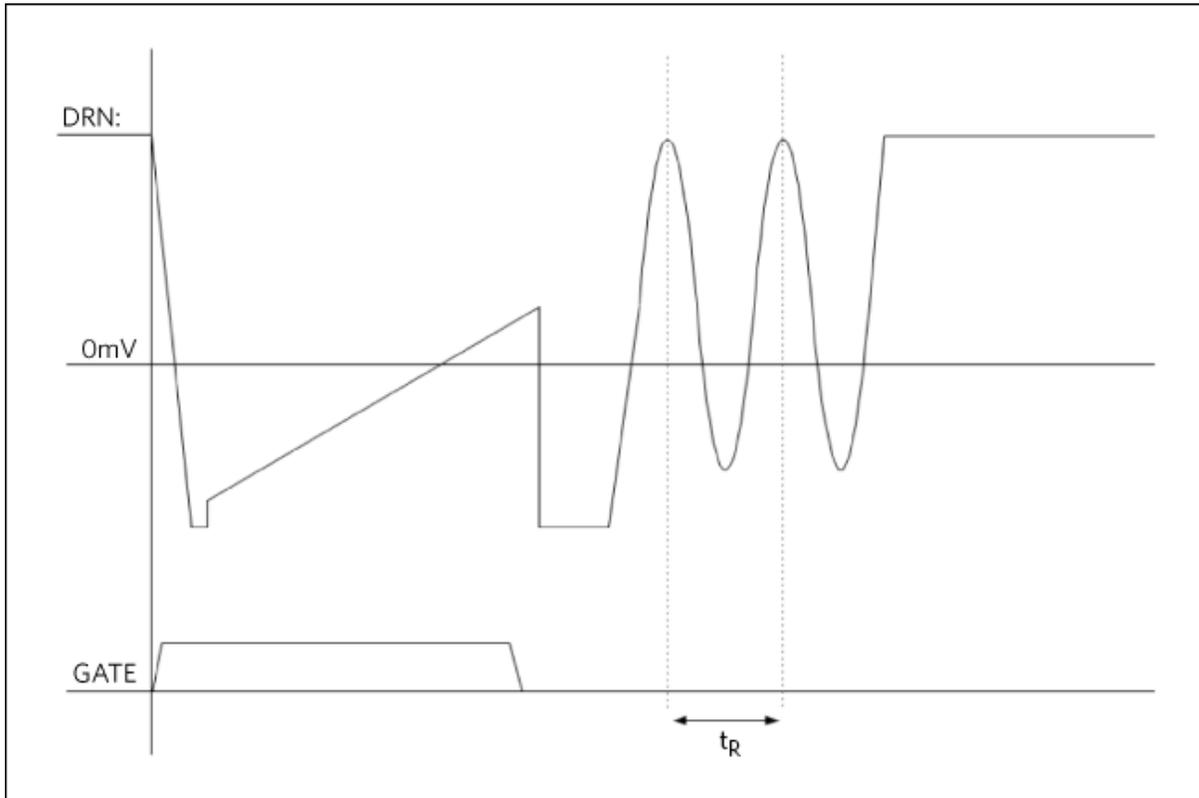


Figure 4. Secondary waveforms during synchronous MOSFET conduction.

Selection of R_{DRN} Resistor

A resistor connected between drain node of the MOSFET and the DRN pin of the MAX17606 decides the secondary MOSFET turn-off instant. The below equation can be arrived using the equivalent circuit shown in **Figure 5** depicting various parameters of the MOSFET and the MAX17606 associated components.

$$R_{DRN} = \frac{R_{TOFF}}{1.21} \times \left(0.03 + V_{trip} - L_{stray} \frac{di_{sec}}{dt} \right)$$

where:

L_{stray} is the MOSFET package lead inductance (see **Table 2** for lead inductance of various packages).

$$\frac{di_{sec}}{dt} = \frac{V_{OUT}}{K^2 \times L_{MAG}}$$

V_{trip} : V_{trip} should be selected as 0mV (corresponds to zero secondary current instant) for $f_{sw} < 100\text{kHz}$ and -6mV for $f_{sw} > 100\text{kHz}$. This ensures the proper output voltage sampling and stable operation of the MAX17690 + MAX17606-based design.

where:

$$V_{\text{DELAY}} = (t_{\text{DELAY}} + t_{\text{OFF}}) \times R_{\text{DS(ON)}} \times \frac{di_{\text{sec}}}{dt}, t_{\text{DELAY}} \text{ can be calculated using Table 3.}$$

Table 3. MAX17606 Turn-Off Delay

S.No	$R_{\text{DS(ON)}} \times \frac{di_{\text{sec}}}{dt}$ (mV/ μ s)	t_{DELAY} (ns)
1	100.00	41
2	66.67	45
3	44.44	47
4	29.63	53
5	19.75	56
6	13.17	63
7	8.78	65
8	5.85	80

For the present design:

$$V_{\text{DELAY}} = (47 \times 10^{-9} + 5.6 \times 10^{-9}) \times 14 \times 10^{-3} \times 3.4 \times 10^6 = 2.5 \text{ mV}$$

$$R_{\text{DRN}} = \frac{147 \times 10^3}{1.21} \times (0.03 - 0.006 - 1.8 \times 10^{-9} \times 3.4 \times 10^6 + 0.0025) = 2.47\text{k}$$

A standard resistor of 2.49k is selected to be the DRN resistor.

Short Circuit Protection

The MAX17690 offers a hiccup scheme that protects and reduces power dissipation in the circuit under output short-circuit conditions. One occurrence of the runaway current limit, or output voltage less than 70% of regulated voltage, would trigger a hiccup mode that protects the converter by immediately suspending the switching for the period of 16,384 clock cycles. The threshold voltage of the runaway current limit comparator is set at 120mV (typ).

Minimum Load Requirement

The MAX17690 samples the output voltage feedback when the primary MOSFET is turned off and energy stored during the "ON time" is being delivered to the secondary. Therefore, it is mandatory to switch the external MOSFET to sample the reflected output voltage. Due to the default switching, a minimum amount energy is delivered to the output capacitor under no-load conditions. This small minimum load can easily be provided on the output by connecting a fixed resistor. In the absence of a minimum load, or a load less than the "minimum load," the output voltage rises to higher values. To protect for this condition, a Zener diode of

appropriate breakdown voltage rating can be installed on the output. Care should be taken to ensure that the Zener breakdown voltage is outside the output voltage envelope in both steady-state and transient conditions.

Under ideal circuit working conditions, the MAX17690 is designed to regulate the output voltage with 1% of full-load rated current on the output. With nonidealities, in most of the designs the current required to regulate the output voltage is less than 2% of the full-load rated current.

Note: Refer to the MAX17690 IC data sheet for more information.

Zener and the Series Resistor Selection

A Zener diode with a Zener breakdown of 10% to 15% higher than the output voltage can serve as a minimum load if preloading is not acceptable. For a 5V output voltage, the Zener breakdown ($V_{ZenerBR}$) is selected to be 5.6V. The maximum power dissipation in the Zener diode at no-load is calculated as:

$$P_{Zener} = I_{minload} \times V_{ZenerBR}$$

$$P_{Zener} = 0.02 \times 5.6 = 112mW$$

where $I_{minload}$ is the minimum load required.

In the present design, the 2% of full-load current is 20mA.

For the present design, a 5.6V, 0.5W MMSZ5232B Zener is selected. The resistor in series with the Zener is calculated based on the Zener breakdown voltage and the desired no-load output voltage.

$$R_{zener} = \frac{V_{OUT(NL)} - V_{ZenerBR}}{I_{minload}}$$

For the present design, the output voltage at absolute no load is set at 6V.

$$R_{zener} = \frac{6 - 5.6}{0.02} = 20\Omega$$

A standard resistor of 22 Ω is selected.

The power dissipation in this resistor is given by:

$$P_{Rzener} = I_{minload}^2 \times R_{zener}$$

$$P_{Rzener} = 0.02^2 \times 22 = 8.8mW$$

Input Capacitor Selection

For DC-DC applications, X7R ceramic capacitors are preferred due to their stability and a low effective series resistance (ESR) and effective series inductance (ESL) over temperature. The minimum value of the input capacitor is expressed as:

$$C_{IN} = \frac{D_{max} \times I_{LIM} \times (1 - (D_{max} / 2))^2}{2 \times f_{SW} \times V_{IN_RIPPLE}}$$

Considering a 2% ripple on the minimum supply voltage, the input capacitance is:

$$C_{IN} = \frac{0.5 \times 1.28 \times (1 - (0.5 / 2))^2}{2 \times 150000 \times 0.02 \times 18} = 3.3 \mu F$$

Two 2.2 μ F, 100V 1210 capacitors have been used in the present design considering the DC-biasing.

Output Capacitor Selection

The output capacitor is selected to limit the output voltage dip to 3% of output voltage for a 50% load step of the rated output current, using the equations below. The recommended bandwidth for the MAX17690-based converter is between $f_{SW}/20$ and $f_{SW}/40$. For the present design, the bandwidth is selected as 7kHz.

$$t_{RESPONSE} \cong \left(\frac{0.33}{f_c} + \frac{1}{f_{SW}} \right)$$

$$t_{RESPONSE} \cong \left(\frac{0.33}{7000} + \frac{1}{150000} \right)$$

$$t_{RESPONSE} \cong 53.8 \mu s$$

$$C_{OUT} = \frac{I_{STEP} \times t_{RESPONSE}}{2 \times \Delta V_{OUT}}$$

$$C_{OUT} = \frac{0.5 \times 54.2 \times 10^{-6}}{2 \times 0.03 \times 5} = 89.6 \mu F$$

From the DC-bias characteristics, the 100 μ F, 6.3V 1210 capacitor offers 43mF at 5V. Hence, two 100 μ F, 6.3V 1210 capacitors are selected for the present design.

The output voltage ripple is determined by the bulk capacitance and ESR (R_{ESR}) of the output capacitor. When using ceramic capacitors, the ESR ripple can be neglected in most of the cases. For the high-ripple current aluminum capacitor, the capacitance calculation begins with the maximum acceptable ripple voltage and how this ripple should be divided between the ESR step and the ripple offered by the bulk capacitance.

For a 1% contribution to the total ripple voltage, the ESR of the output capacitor should be:

$$R_{ESR} \leq \frac{0.01 \times V_{OUT} \times (1 - D_{MAX})}{2 \times I_{OUT}}$$

For a 1% contribution to the total ripple voltage, the bulk capacitance should be:

$$C_{OUT} < \frac{I_{OUT}}{0.01 \times V_{OUT} \times f_{sw}}$$

Loop Compensation

The loop compensation values are calculated as follows:

$$\text{Load pole } f_p = \frac{I_{OUT}}{\pi \times V_{OUT} \times C_{OUT}} = \frac{1}{\pi \times 5 \times 86 \times 10^{-6}} = 740.1 \text{ Hz}$$

$$R_Z = 12500 \times R_{CS} \left(\frac{f_c}{f_p} \right) \sqrt{\frac{V_{OUT} \times I_{OUT}}{2 \times L_{PRI} \times F_{SW}}}$$

$$R_Z = 12500 \times 0.062 \left(\frac{7000}{746.4} \right) \sqrt{\frac{5 \times 1}{2 \times 46.4 \times 10^{-6} \times 150000}}$$

$$R_Z = 4.39 \text{ k}$$

A standard resistor of 4.3k is selected.

$$C_Z = \frac{1}{2\pi \times R_Z \times f_p}$$

$$C_Z = \frac{1}{2\pi \times 4300 \times 740.1} = 50 \text{ nF}$$

A standard capacitor of 47nF is selected.

$$C_p = \frac{1}{\pi \times R_Z \times f_{SW}} = \frac{1}{\pi \times 4300 \times 150000} = 493 \text{ pF}$$

A standard capacitor of 470pF is selected.

Note: When the ESR zero of the output capacitor is significant, the compensator pole capacitor (C_p) should be selected to cancel the ESR zero.

$$C_p = \frac{1}{2 \times \pi \times R_Z \times f_{ESR}}$$

PCB Guidelines

Careful PCB layout is critical to achieve stable operation of any power-supply design. Follow the below guidelines for good PCB layout:

1. Keep the loop area of paths carrying the pulsed currents as small as possible. In flyback design, the loop created by the V_{IN} bypass capacitor, transformer primary winding, MOSFET switch, and sense resistor is critical. Similarly, the high-frequency current path for the MOSFET gate switching from the INTVCC capacitor through the source of the MOSFET and sense resistor is also critical.
2. The INTVCC bypass capacitor should be connected right across the INTVCC and PGND pins of the MAX17690.
3. A bypass capacitor should be connected across the V_{IN} and SGND pins and should be placed close to MAX17690.
4. The IC's exposed pad should be directly connected to the MAX17690's SGND pin. The exposed pad

should also be connected to the SGND plane in other layers by means of thermal vias under the exposed pad so that the heat flows to the large “signal ground” (SGND) plane.

5. The R_{FB} resistor trace length should be kept as small as possible.
6. The PGND connection from the INTVCC capacitor and the SGND plane should be star connected at the negative terminal of the current-sense resistor.
7. The proper sensing of drain-to-source voltage across the secondary MOSFET is critical in MAX17606. The R_{DRN} should be Kelvin connected to the drain of the synchronous MOSFET. The source pin of the MOSFET should also be Kelvin connected to the MAX17606 GND pin.
8. Connect the R_{TOFF} resistor directly between TOFF pin and the MAX17606 GND pin. The return path should not be connected to ground plane.

Reference Design: MAX17690EVKITA#

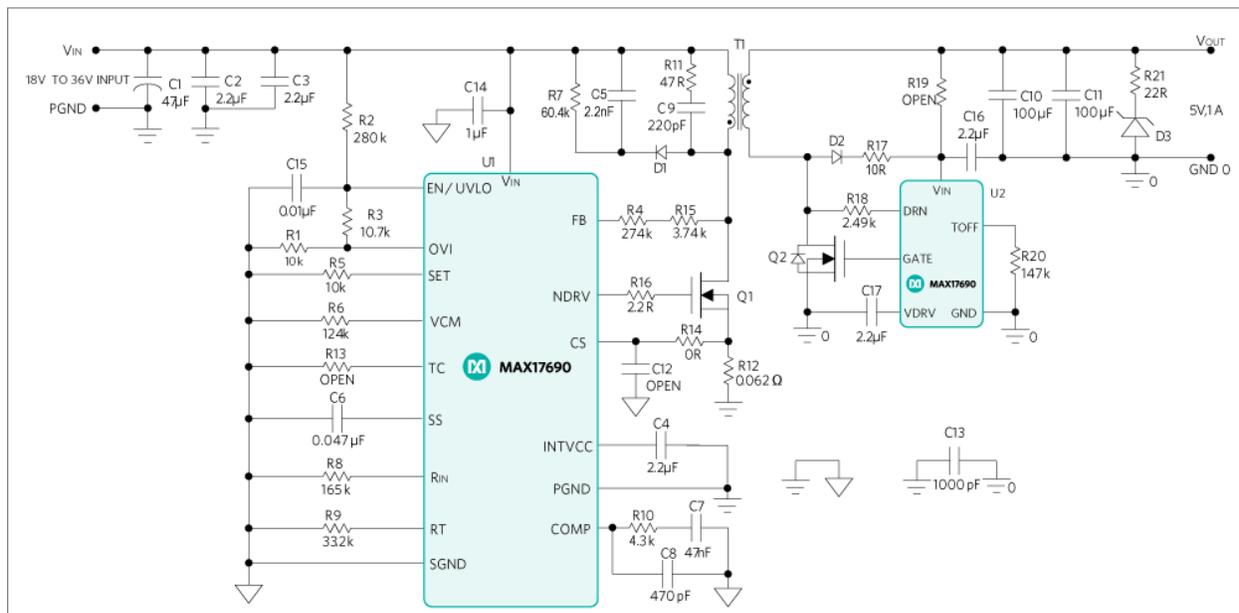


Figure 6. MAX17690EVKITA# schematic.

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Related Parts		
MAX17606	Secondary-Side Synchronous MOSFET Driver for Flyback Converters	Free Samples
MAX17690	60V, No-Opto Isolated Flyback Controller	Free Samples
MAX17690EVKITA	Evaluation Kit for the MAX17690	

More Information

For Technical Support: <https://www.maximintegrated.com/en/support>

For Samples: <https://www.maximintegrated.com/en/samples>

Other Questions and Comments: <https://www.maximintegrated.com/en/contact>

Application Note 6394: <https://www.maximintegrated.com/en/an6394>

APPLICATION NOTE 6394, AN6394, AN 6394, APP6394, Appnote6394, Appnote 6394

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