2.5 V/3.3 V SiGe Differential Smart Gate with Output Level Select

NB7L86A

The NB7L86A is a multi-function differential Logic Gate which can be configured as an AND/NAND, OR/NOR, XOR/XNOR, or 2:1 MUX. This device is part of the GigaComm^M family of high performance Silicon Germanium products. The device is housed in a 3 x 3 mm 16 pin QFN package.

Differential inputs incorporate internal 50 Ω termination resistors and accept NECL (Negative ECL), PECL (Positive ECL), LVCMOS/LVTTL, CML, or LVDS. The Output Level Select (OLS) input is used to program the peak-to-peak output amplitude between 0 and 800 mV in five discrete steps.

The NB7L86A employs input default circuitry so that under open input condition (Dx, $\overline{\text{Dx}}$, VTDx, $\overline{\text{VTDx}}$, VTSEL) the Outputs of the device remains stable.

Features

- Maximum Input Clock Frequency > 8 GHz Typical
- Maximum Input Data Rate > 8 Gb/s Typical
- 165 ps Typical Propagation Delay
- 40 ps Typical Rise and Fall Times
- Selectable Swing PECL Output with Operating Range: $V_{CC} = 2.375$ V to 3.465 V with $V_{EE} = 0$ V
- Selectable Swing NECL Output with NECL Inputs with Operating Range: $V_{CC} = 0$ V with $V_{EE} = -2.375$ V to -3.465 V
- Selectable Output Level (0 V, 200 mV, 400 mV, 600 mV, or 800 mV Peak-to-Peak Output)
- 50 Ω Internal Input Termination Resistors
- This is a Pb-Free Device



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QFN16 3x3, 0.5P CASE 485G

MARKING DIAGRAM



(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 17 of this data sheet.

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Figure 1. QFN16 Pinout (Top View)

Table 1. PIN DESCRIPTION

Pin	Name	I/O	Description
1	OLS (Note 3)	Input	Input for OLS (Output Level Select) Pin. Refer Table 2
2	SEL	Input: LVCMOS/LVTTL, ECL/CML/LVDS	Input for Select Logic Pin, Single Ended or Inverted Differential
3	SEL	Input: LVCMOS/LVTTL, ECL/CML/LVDS	Input for Select Logic Pin, Single Ended or non-Inverted Differential
4	VTSEL (Note 1)		Pin with a common internal 50 Ω termination from SEL/SEL Pins. Refer Table 7 for usage with different Interface options
5	VTD1 (Note 1)		Pin with an internal 50 Ω termination from D1 Pin. Refer Table 7 for usage with different Interface options
6	D1	Input: LVCMOS/LVTTL, ECL/CML/LVDS	Input Pin, Non–inverted Differential or Single Ended with internal 75 k Ω connected to V_{EE}
7	D1	Input: LVCMOS/LVTTL, ECL/CML/LVDS	Input Pin, Inverted Differential or Single Ended with internal 75 k Ω connected to V_{EE} and 36.5 k Ω connected to V_{CC}
8	VTD1 (Note 1)		Pin with an internal 50 Ω termination from D1 Pin. Refer Table 7 for usage with different Interface options
9	V _{CC} (Note 2)		Positive Supply Voltage
10	Q	Output: Reduced Swing ECL	Output Pin, non–inverted Differential Output with typical 50 Ω termination to V_TT = V_{CC} – 2 V
11	Q	Output: Reduced Swing ECL	Output Pin, inverted Differential Output with typical 50 Ω termination to V_TT = V_{CC} – 2 V
12	V _{EE} (Note 2)		Negative Supply Voltage
13	VTD0 (Note 1)		Pin with an internal 50 Ω termination from D0 Pin. Refer Table 7 for usage with different Interface options
14	DO	Input: LVCMOS/LVTTL, ECL/CML/LVDS	Input Pin, Inverted Differential or Single Ended with internal 75 k Ω connected to V_{EE} and 36.5 k Ω connected to V_{CC}
15	D0	Input: LVCMOS/LVTTL, ECL/CML/LVDS	Input Pin, Non–inverted Differential or Single Ended with internal 75 $k\Omega$ connected to V_{EE}
16	VTD0 (Note 1)		Pin with an internal 50 Ω termination from D0 Pin. Refer Table 7 for usage with different Interface options
	EP		Exposed Pad (EP) is thermally connected to the die for improved heat transfer out of the package. The exposed pad can be connected electrically to V_{EE} on the PCB board

In the differential configuration when the input termination pins (VTD0/1, VTD0/1, VTSEL) are connected to a common termination voltage, or left open, and if no signal is applied then the device will be susceptible to self-oscillation.
 All V_{CC} and V_{EE} pins must be externally connected to Power Supply to guarantee proper operation.
 When an output level of 400 mV is desired and V_{CC} - V_{EE} > 3.0 V, 2 kΩ resistor should be connected from OLS pin to V_{EE}.

Table 2. OUTPUT LEVEL SELECT OLS

OLS	Q/Q VPP	OLS Sensitivity
V _{CC}	800 mV	OLS – 75 mV
V _{CC} – 0.4 V	200 mV	$OLS \pm 150 \text{ mV}$
V _{CC} – 0.8 V	600 mV	$OLS \pm 100 \text{ mV}$
V _{CC} – 1.2 V	0 mV	$OLS \pm 75 \text{ mV}$
V _{EE} (Note 4)	400 mV	$OLS \pm 100 \text{ mV}$
Float	600 mV	N/A

4. When an output level of 400 mV is desired and V_{CC} - V_{EE} > 3.0 V, 2 k Ω resistor should be connected from OLS to to V_{EE}.



Figure 2. Logic Diagram



Figure 3. Configuration for AND/NAND Function

Table 3. AND/NAND TRUTH TABLE (Note 5)

	α	β	α*β
D0	D1	SEL	Q
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1

5. D0, D1, SEL are inverse of D0, D1, SEL unless specified otherwise.



Figure 4. Configuration for OR/NOR Function



Figure 5. Configuration for XOR/XNOR Function



Figure 6. Configuration for 2:1 MUX Function

Table 4. OR/NOR TRUTH TABLE (*)

α		β	α or β
D0	D1	SEL	Q
0	1	0	0
0	1	1	1
1	1	0	1
1	1	1	1

*D0, D1, SEL are inverse of $\overline{D0}$, $\overline{D1}$, \overline{SEL} unless specified otherwise.

Table 5. XOR/XNOR TRUTH TABLE (*)

α		β	α XOR β
D0	D1	SEL	Q
0	1	0	0
0	1	1	1
1	0	0	1
1	0	1	0

*D0, D1, SEL are inverse of $\overline{D0}$, $\overline{D1}$, \overline{SEL} unless specified otherwise.

Table 6. 2:1 MUX TRUTH TABLE (*)

SEL	Q
1	D1
0	D0

*D0, D1, SEL are inverse of D0, D1, SEL unless specified otherwise.

Table 7. INTERFACING OPTIONS

INTERFACING OPTIONS	CONNECTIONS
CML	Connect VTD0, VTD0, VTSEL, VTD1, VTD1 TO V _{CC}
LVDS	Connect VTD0, VTD0, VTD1, and VTD1 together. Leave VTSEL open
AC-COUPLED	Bias $\overline{\text{VTD0}}$, VTD0, VTSEL, $\overline{\text{VTD1}}$, VTD1 and VTSEL inputs within the Common Mode range (VIHCMR)
RSECL, PECL, NECL	Standard ECL termination techniques
LVTTL, LVCMOS	An external voltage should be applied to the unused complementary differential input. Nominal voltage of 1.5 V for LVTTL and $V_{CC}/2$ for LVCMOS inputs

Table 8. ATTRIBUTES

Characteristics	Value
Internal Input Pulldown Resistors (R1)	75 kΩ
Internal Input Pullup Resistor (R ₂)	37.5 kΩ
ESD Protection:	
Human Body Model	\geq 4 kV
Charged Device Model	\geq 2 kV
Machine Model	≥ 200 V
Moisture Sensitivity (Note 6), Pb-Free	Level 1
Flammability Rating, Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

6. For additional information, see Application Note AND8003/D.

Table 9. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V _{CC}	Positive Power Supply	V _{EE} = 0 V		3.6	V
V_{EE}	Negative Power Supply	V _{CC} = 0 V		-3.6	V
VI	Positive Input	V _{EE} = 0 V	$VI \le V_{CC}$	3.6	V
	Negative Input	$V_{CC} = 0 V$	$VI \ge V_{EE}$	-3.6	V
V _{INPP}	Differential Input Voltage	$V_{CC} - V_{EE} \ge 2.8 \text{ V}$		2.8	V
* INPP	Dn – Dn , SEL – <u>SEL</u>	$V_{CC} - V_{EE} \le 2.8 \text{ V}$		$ V_{CC} - V_{EE} $	
I _{IN}	Input Current through RT (50 Ω Resistor)	Static		45	mA
IN		Surge		80	mA
I _{OUT}	Output Current	Continuous		25	mA
1001		Surge		50	mA
T _A	Operating Temperature Range			-40 to +85	°C
Tstg	Storage Temperature Range			-65 to +150	°C
θյΑ	Thermal Resistance (Junction-to-Ambient)	0 lfpm		41.6	°C/W
00/1	(Note 7)	500 lfpm		35.2	°C/W
θJC	Thermal Resistance (Junction-to-Case)	2S2P (Note 7)		4	°C/W
Tsol	Wave Solder (Pb-Free)	< 3 sec @ 260°C		265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

7. JEDEC standard multilayer board - 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

			-40°C			25°C			85°C		
Symbol	Characteristic	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
POWER	SUPPLY CURRENT					•					
I _{EE}	Negative Power Supply Current	23	30	39	23	30	39	23	30	39	mA
VPECL	OUTPUTS (Note 9)										
V _{OH}	Output HIGH Voltage	1460	1510	1570	1490	1540	1600	1515	1565	1625	mV
V _{OL}	Output LOW Voltage										mV
	(OLS = V _{CC})	555	705	855	595	745	895	625	775	925	
	$(OLS = V_{CC} - 0.4 V)$	1235	1295	1385	1270	1330	1420	1295	1355	1445	
	$(OLS = V_{CC} - 0.8 V, OLS = FLOAT)$	775	895	1015	810	930	1050	840	960	1080	
	(OLS = V _{CC} - 1.2 V)	1455	1505	1585	1490	1540	1620	1510	1560	1640	
	(OLS = V _{EE})	1005	1095	1215	1040	1130	1250	1065	1155	1275	
VOUTPP	Output Voltage Amplitude										mV
	(OLS = V _{CC})	670	800		660	795		655	790		
	$(OLS = V_{CC} - 0.4 V)$	125	215		120	210		120	210		
	$(OLS = V_{CC} - 0.8 V, OLS = FLOAT)$	510	615		505	610		500	605		
	(OLS = V _{CC} - 1.2 V)	0	5		0	0		0	5		
	(OLS = V _{EE})	325	415		320	410		320	410		
DIFFERE	ENTIAL CLOCK INPUTS DRIVEN SING	LE END	ED (Figu	re 11 & 10	3) (Note 1	10)					
V _{IH}	Input HIGH Voltage (Single-Ended): D, D, SEL, SEL	1200		V _{CC}	1200		V _{CC}	1200		V _{CC}	mV
V _{IL}	Input LOW Voltage (Single-Ended): D, D, SEL, SEL	0		V _{CC} – 150	0		V _{CC} – 150	0		V _{CC} – 150	mV
Vth	Input Threshold Reference Voltage Range (Note 11)	950		V _{CC} -75	950		V _{CC} -75	950		V _{CC} -75	mV
V _{ISE}	Single-Ended Input Voltage (V _{IH} - V _{IL})	150		2600	150		2600	150		2600	mV
DIFFERE		LLY (Fig	oure 12) (Note 12)							
V _{IHD}	Differential Input HIGH Voltage (D, D, SEL, SEL)	1200	jui e 1 <u>–</u>) (V _{CC}	1200		V _{CC}	1200		V _{CC}	mV
V _{ILD}	Differential Input LOW Voltage (D, D̄, SEL, SEL)	0		V _{CC} – 75	0		V _{CC} – 75	0		V _{CC} – 75	mV
V_{ID}	Differential Input Voltage (V _{IHD} -V _{ILD}) (D, D, SEL, <u>SEL</u>)	75		2600	75		2600	75		2600	mV
VIHCMR	Input HIGH Voltage Common Mode Range (Differential Configuration) (Note 13) (Figure 15)	1200		2500	1200		2500	1200		2500	mV
I _{IH}	Input HIGH Current (@ V _{IH}) D, D,		30	100		30	100		30	100	μA
	SEL, SEL		5	50		5	50		5	50	•
١ _{IL}	Input LOW Current (@ V_{IL}) D, \overline{D} ,		20	100		20	100		20	100	μA
	SEL, SEL		5	50		5	50		5	50	,
ERMIN	ATION RESISTORS		8	8	8	1	8	1	8	1	
R _{TIN}	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	Ω
	arametric performance is indicated in th										

Table 10. DC CHARACTERISTICS, INPUT WITH I VPECI, OUTPUT: $V_{CC} = 2.5 \text{ V}$, $V_{CC} = 0.4 \text{ T}_{A} = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ (Note 8)

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

8. Input and output parameters vary 1:1 with V_{CC}. 9. LVPECL outputs loaded with 50 Ω to (V_{CC} - 2 V) for proper operation. 10. V_{th}, V_{IH}, V_{IL}, and V_{ISE} parameters must be complied with simultaneously. 11. V_{th} is applied to the complementary input when operating in single–ended mode. V_{th} = (V_{IH} - V_{IL}) / 2.

12. V_{IHD} , V_{ILD} , V_{ID} and V_{CMR} parameters must be complied with simultaneously. 13. V_{IHCMR} min varies 1:1 with V_{EE} , V_{IHCMR} max varies 1:1 with V_{CC} . The V_{IHCMR} range is referenced to the most positive side of the differential input signal.

IEE Net VOH Ou VOH Ou VOL Ou VOUTPP Ou OIFFERENTI Ou VIH In VIL In VISE Si VIHD Di VILD Di VID OU VID OU	CharacteristicsUPPLY CURRENTegative Power Supply CurrentTPUTS (Note 15)utput Note 15)utput LOW Voltage(OLS = V _{CC} - 0.4 V)(OLS = V _{CC} - 0.4 V)(OLS = V _{CC} - 0.4 V)(OLS = V _{CC} - 0.8 V, OLS = FLOAT)(OLS = V _{CC} - 1.2 V)(OLS = V _{CC} - 0.4 V)(OLS = V _{CC} - 0.4 V)(OLS = V _{CC} - 0.4 V)(OLS = V _{CC} - 0.8 V, OLS = FLOAT)(OLS = V _{CC} - 0.8 V, OLS = FLOAT)(OLS = V _{CC} - 1.2 V)(OLS = V _{CC} - 0.4 V)	2030 1550 2260 1785 705 130 535	Typ 30 2310 1470 2090 1670 2310 1875 815 220	Max 39 2370 1620 2180 1790 2390 1995	Min 23 2290 1360 2065 1585 2290 1820	Typ 30 2340 1510 2125 1705 2340 1910	Max 39 2400 1660 2215 1825 2420	Min 23 2315 1390 2090 1615	Typ 30 2365 1540 2150 1735	Max 39 2425 1690 2240 1855	Unit mA mV mV
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DIFFERENTI VIH INI (S D, VIL INI (S D, VIL INI (S D, VIL INI (S D, VIL INI (S D, VIL INI (S D, VIL D, VIL D, VIL D, VIL D, VIL D, VIL D, VIL D, VIL D, D, VIL D, D, VIL D, D, VIL D, D, D, D, D, D, D, D, D, D, D, D, D,	$(OLS = V_{CC})$ $(OLS = V_{CC} - 0.4 \text{ V})$ $(OLS = V_{CC} - 0.8 \text{ V},$ $OLS = FLOAT)$ $(OLS = V_{CC} - 1.2 \text{ V})$	130 535					2030	1850	1940	2060	
DIFFERENTI VIH IN S D, VIH IN S D, VIL IN S D, VIL IN S D, VIL IN S D, VIL IN S D, VIL IN S VIL IN S VIL IN S VIL IN S VI VIL IN S VI VIL IN S VI VIL IN S VI VI VI VI VI VI VI VI VI VI VI VI VI	$(OLS = V_{CC} - 0.4 V)$ $(OLS = V_{CC} - 0.8 V,$ $OLS = FLOAT)$ $(OLS = V_{CC} - 1.2 V)$	130 535					I I				mV
V _{IH} In (S D, V _{IL} In (S D, V _{th} In Ra V _{ISE} Si (V DIFFERENTI V _{IHD} Di (D V _{ILD} Di (D V _{ILD} Di (V V _{ILD} Di (V V _{ILD} Di	(OLS = V _{CC} - 0.8 V, OLS = FLOAT) (OLS = V _{CC} - 1.2 V)	535	220	1	695	805		690	800		
V _{IH} In (S D, V _{IL} In (S D, V _{th} In Ra V _{ISE} Si (V DIFFERENTI V _{IHD} Di (D V _{ILD} Di (D V _{ILD} Di (V V _{ILD} Di (V V _{ILD} Di	(OLS = V _{CC} - 0.8 V, OLS = FLOAT) (OLS = V _{CC} - 1.2 V)	535			125	215		125	215		
V _{IH} In (S D, V _{IL} In (S D, V _{th} In Ra V _{ISE} Si (V DIFFERENTI V _{IHD} Di (D V _{ILD} Di (D V _{ILD} Di (V V _{ILD} Di (V V _{ILD} Di			640		530	635		525	630		
V _{IH} In (S D, V _{IL} In (S D, V _{th} In Ra V _{ISE} Si (V DIFFERENTI V _{IHD} Di (D V _{ILD} Di (D V _{ID} Di (V V _{IHCMR} In		0	0		0	0		0	0		
V _{IH} In (S D, V _{IL} In (S D, V _{th} In Ra V _{ISE} Si (V DIFFERENTI V _{IHD} Di (D V _{ILD} Di (D V _{ILD} Di (V V _{ILD} Di (V V _{ILD} Di	(OLS = VFF) (NOLE 20)		435		340	430		335	425		
VIL IN VIL IN VIL IN S D, Vth IN Ri VISE SI VISE (V DIFFERENTI VIHD DI (D VILD DI VID DI VID DI VID DI	IAL CLOCK INPUTS DRIVEN SING		DED (Fig	ure 11 & 1	3) (Note	16)	I I			1	
V _{IL} In (S D, V _{th} In Ra V _{ISE} (V DIFFERENTI V _{IHD} Di (D V _{IHD} Di (D V _{ID} Di (V V _{IHCMR} In	put HIGH Voltage Single-Ended) , D, SEL, SEL	1200		V _{CC}	1200		V _{CC}	1200		V _{CC}	mV
VISE Si VISE (V DIFFERENTI VIHD Di VILD Di VILD Di VID Di VID Di VID Di VID DI	put LOW Voltage Single – Ended) , D, SEL, SEL	0		V _{CC} - 150	0		V _{CC} - 150	0		V _{CC} - 150	mV
VIHCMR IN	put Threshold Reference Voltage ange (Note 17)	950		V _{CC} –75	950		V _{CC} –75	950		V _{CC} –75	mV
V _{IHD} Di (D V _{ILD} V _{ID} V _{ID} V _{IHCMR} In	ingle–Ended Input Voltage / _{IH} – V _{IL})	150		2600	150		2600	150		2600	mV
V _{ILD} (D V _{ILD} Di (D V _{ID} Di (V V _{IHCMR} In	IAL INPUTS DRIVEN DIFFERENTIA	ALLY (Fig	gure 12)	(Note 18)							
(D V _{ID} Di (V V _{IHCMR} In	ifferential Input HIGH Voltage), D, SEL, SEL)	1200		V _{CC}	1200		V _{CC}	1200		V _{CC}	mV
(V V _{IHCMR} Inj	ifferential Input LOW Voltage), D, SEL, SEL)	0		V _{CC} - 75	0		V _{CC} - 75	0		V _{CC} - 75	mV
	ifferential Input Voltage / _{IHD} − V _{ILD}) (D, D, SEL, <u>SEL</u>)	75		2600	75		2600	75		2600	mV
(N	put HIGH Voltage Common Mode ange (Differential Configuration) Note 19) (Figure 15)	1200		3300	1200		3300	1200		3300	mV
l _{IH} In			30	100		30	100		30	100	μA
	put HIGH Current (@V _{IH}) D, D		5	50		5	50		5	50	
l _{IL} In	iput HIGH Current (@V _{IH}) D, D SEL, SEL		20	100		20	100		20	100	μA
			5	50		5	50		5	50	1
TERMINATI	SEL, SEL										
R _{TIN} Int	SEL, SEL put LOW Current (@V _{IL}) D, D										

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit

bevice with meet the specifications after thermal equilibrium has been established when modified in a test socket of printed circuit board with maintained transverse airflow greater than 500 lfpm.
14. Input and output parameters vary 1:1 with V_{CC}.
15. LVPECL outputs loaded with 50 Ω to (V_{CC} - 2 V) for proper operation.
16. V_{th}, V_{IH}, V_{IL}, and V_{ISE} parameters must be complied with simultaneously.
17. V_{th} is applied to the complementary input when operating in single–ended mode. V_{th} = (V_{IH} - V_{IL}) / 2.
18. V_{IHD}, V_{ILD}, V_{ID} and V_{CMR} parameters must be complied with simultaneously.
19. V_{IHCMR} min varies 1:1 with V_{EE}, V_{IHCMR} max varies 1:1 with V_{CC}. The V_{IHCMR} range is referenced to the most positive side of the differential input signal. input signal.

20. When an output level of 400 mV is desired and V_{CC} – V_{EE} > 3.0 V, a 2 k Ω resistor should be connected from OLS to V_{EE}.

Table 12. DC CHARACTERISTICS, NECL INPUT WITH NECL OUTPUT

 V_{CC} = 0 V; V_{EE} = –3.465 V to –2.375 V, T_A = –40°C to +85°C (Note 21)

			–40°C			25°C			85°C		
Symbol	Characteristics	Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
POWER S	UPPLY CURRENT	-	-	-	-	-	-	-	-	-	
I _{EE}	Negative Power Supply Current	23	30	39	23	30	39	23	30	39	mA
VPECL C	DUTPUTS (Note 22)										
V _{OH}	Output HIGH Voltage	-1040	-990	-930	-1010	-960	-900	-985	-935	-875	mV
V _{OL}	Output LOW Voltage:										mV
	$-3.465 \text{ V} \le \text{V}_{EE} \le -3.0 \text{ V}$										1
	(OLS = V _{CC})	-1980	-1830	-1680	-1940	-1790	-1640	-1910	-1760	-1610	1
	(OLS = V _{CC} - 0.4 V)	-1270	-1210	-1120	-1235	-1175	-1085	-1210	-1150	-1060	1
	$(OLS = V_{CC} - 0.8 V, OLS = FLOAT)$	-1750	-1630	-1510	-1715	-1595	-1475	-1685	-1565	-1445	1
	(OLS = V _{CC} - 1.2 V)	-1040	-990	-910	-1010	-960	-880	-985	-935	-855	1
	(OLS = V _{EE}) (Note 27)	-1515	-1425	-1305	-1480	-1390	-1270	-1450	-1360	-1240	1
	$-3.0 \text{ V} < \text{V}_{\text{EE}} \le -2.375 \text{ V}$										1
	(OLS = V _{CC})	-1945	-1795	-1645	-1905	-1755	-1605	-1875	-1725	-1575	
	(OLS = V _{CC} - 0.4 V)	-1265	-1205	-1115	-1230	-1170	-1080	-1205	-1145	-1055	1
	$(OLS = V_{CC} - 0.8 V, OLS = FLOAT)$	-1725	-1605	-1485	-1690	-1570	-1450	-1660	-1540	-1420	1
	(OLS = V _{CC} - 1.2 V)	-1045	-995	-915	-1010	-960	-880	-990	-940	-860	1
	(OLS = V _{EE})	-1495	-1405	-1285	-1460	-1370	-1250	-1435	-1345	-1225	1
V _{OUTPP}	Output Voltage Amplitude:										m٧
	$-3.465 \text{ V} \le \text{V}_{EE} \le -3.0 \text{ V}$										1
	(OLS = V _{CC})	705	815		695	805		690	800		1
	(OLS = V _{CC} - 0.4 V)	130	220		125	215		125	215		1
	$(OLS = V_{CC} - 0.8 V, OLS = FLOAT)$	535	640		530	635		525	630		1
	(OLS = V _{CC} - 1.2 V)	0	0		0	0		0	0		1
	(OLS = V _{EE}) (Note 27)	345	435		340	430		335	425		1
	$-3.0 \text{ V} < \text{V}_{\text{EE}} \le -2.375 \text{ V}$										1
	(OLS = V _{CC})	670	800		660	795		655	790		1
	(OLS = V _{CC} - 0.4 V)	125	215		120	210		120	210		1
	$(OLS = V_{CC} - 0.8 V, OLS = FLOAT)$	510	615		505	610		500	605		1
	(OLS = V _{CC} - 1.2 V)	0	5		0	0		0	5		1
	(OLS = V _{EE})	325	415		320	410		320	410		1
DIFFEREN	NTIAL CLOCK INPUTS DRIVEN SINGLE-	ENDED	(Figure	11 & 13)	(Note 23	;)					
V _{IH}	Input HIGH Voltage (Single-Ended) D, D, SEL, SEL	V _{EE} + 1200		V _{CC}	V _{EE} + 1200		V _{CC}	V _{EE} + 1200		V _{CC}	m∨
V _{IL}	Input LOW Voltage (Single-Ended)	V_{EE}	1	V _{IH} - 150	V_{EE}		V _{IH-} 150	VEE		V _{IH} - 150	m∖

	D, D, OLL, OLL	1200		1200		1200		
V _{IL}	Input LOW Voltage (Single-Ended) D, D, SEL, SEL	V _{EE}	V _{IH} - 150	V _{EE}	V _{IH-} 150	VEE	V _{IH} - 150	mV
V _{th}	Input Threshold Reference Voltage Range (Note 24)	V _{EE} + 950	V _{CC} -75	V _{EE} + 950	V _{CC} -75	V _{EE} + 950	V _{CC} -75	mV
V _{ISE}	Single–Ended Input Voltage (V _{IH} – V _{IL})	150	2600	150	2600	150	2600	mV

Table 12. DC CHARACTERISTICS, NECL INPUT WITH NECL OUTPUT

 V_{CC} = 0 V; V_{EE} = -3.465 V to -2.375 V, T_A = -40°C to +85°C (Note 21)

haracteristics DRIVEN DIF Dut HIGH Volta EL) Dut LOW Voltage EL) Dut Voltage (D, D, SEL, SE	ge ge	V _{EE} + 1200 V _{EE}	Typ e 12) (No	Max ote 25) V _{CC} V _{CC} - 75	Min V _{EE} + 1200 V _{EE}	Тур	Max V _{CC} V _{CC} -	Min V _{EE} + 120	Тур	Max V _{CC}	Unit mV
out HIGH Volta EL) out LOW Voltag EL) out Voltage	ge ge	V _{EE} + 1200 V _{EE}	e 12) (No	V _{CC}	1200			120		V _{CC}	mV
EL) out LOW Voltag EL) out Voltage	ge	1200 V _{EE}		V _{CC} -	1200			120		V _{CC}	mV
EL) out Voltage					V_{EE}		Vcc-				
	 -\						75	V _{EE}		V _{CC} - 75	mV
(, _ , , ,	=L)	75		2600	75		2600	75		2600	mV
oltage Commo ential Configura ure 15)		V _{EE} + 1200		0	V _{EE} + 1200		0	V _{EE} + 1200		0	μΑ
Current (@V _{IH}) D, <u>D</u> ,		30	100		30	100		30	100	μA
	SEL, <u>SEL</u>		5	50		5	50		5	50	1
Current (@V _{IL})	$D, \overline{D},$		20	100		20	100		20	100	μA
	SEL, SEL		5	50		5	50		5	50	1
ն	urrent (@V _{IL})				SEL, SEL 5 50					SEL, SEL 5 50 5 50 5	SEL, SEL 5 50 5 50 5 50

R _{TIN}	Internal Input Termination Resistor	45	50	55	45	50	55	45	50	55	Ω	
Droduct par	amotric porformance is indicated in the El	ootrical (Charaoto	rictics fo	r the liet	ad tost of	onditione	unloce	othonwic	a notod	Product	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

21. Input and output parameters vary 1:1 with V_{CC} . 22. LVPECL outputs loaded with 50 Ω to ($V_{CC} - 2$ V) for proper operation. 23. V_{th} , V_{IH} , V_{IL} , and V_{ISE} parameters must be complied with simultaneously. 24. V_{th} is applied to the complementary input when operating in single-ended mode. $V_{th} = (V_{IH} - V_{IL}) / 2$. 25. V_{IHD} , V_{ILD} , and V_{CMR} parameters must be complied with simultaneously. 26. V_{uccurr} min varies 1:1 with V_{err} . V_{uccurr} max varies 1:1 with V_{err} .

26. VIHCMR min varies 1:1 with VEE, VIHCMR max varies 1:1 with VCC. The VIHCMR range is referenced to the most positive side of the differential input signal.

27. When an output level of 400 mV is desired and V_{CC} - V_{EE} > 3.0 V, a 2 kΩ resistor should be connected from OLS to V_{EE}.

0	Oh and a training the			–40°C		25°C			85°C			
Symbol	Characteristic		Min	Тур	Max	Min	Тур	Max	Min	Тур	Max	Unit
f _{max}	Maximum Input Clock Frequency (See Figure 7) (Note 28)		7	8		7	8		7	8		GHz
VOUTPP	1 3 1	_{in} < 7 GHz	590	730		470	720		540	700		mV
00111	$(OLS = V_{CC})$ f _i	_{in} = 8 GHz	270	440		230	420		180	390		mV
t _{PLH}	Propagation Delay to Output Differential											
t _{PHL}	(Figure 15) D/SEL \rightarrow Q		110	160	210	115	165	215	120	170	220	ps
t _{SKEW}	Duty Cycle Skew (Note 29)			5	15		5	15		5	15	ps
t _{SKEW}	Channel Skew C	$Q \rightarrow D/SEL$		5	20		5	20		5	20	ps
t _S	Set–Up Time (Dx to SEL)		30			30			30			ps
t _H	Hold–Up Time (Dx to SEL)		35			35			35			ps
t _{JITTER}	RMS Random Clock Jitter (See Figure 7) (Note 31) fin \leq 7 GF	Ηz		0.5	1.5		0.5	1.5		0.5	1.5	ps
	Peak–to–Peak Data Dependent Jitter (Note 32) fin ≤ 7 Gb/s			12			12			12		
V _{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration) (Note 30)		75		1890	75		1890	75		1890	mV
t _r , t _f	Output Rise/ Fall Times	t _r	30	45	65	30	45	65	30	45	65	ps
	(20% – 80%) (Q, Q) @ 1 GHz	t _f	17	35	65	17	35	65	17	35	65	

Table 13. AC CHARACTERISTICS $V_{CC} = 0 V$; $V_{EE} = -3.465 V$ to -2.37	75 V or $V_{CC} = 2.375$ V to 3.465 V: $V_{EE} = 0$ V

28. Measured using a 500 mV source, 50% duty cycle clock source. All loading with 50 Ω to V_{CC} – 2.0 V. Input edge rates 40 ps (20% – 80%). 29. t_{SKEW} = |t_{PLH} – t_{PHL}| for a nominal 50% differential clock input waveform. See Figure 15. 30. V_{INPP} (max) cannot exceed V_{CC} – V_{EE}. 31. Additive RMS jitter with 50% duty cycle clock signal at 7 GHz. 32. Additive Peak-to-Peak data dependent jitter with NRZ PRBS 2³¹–1 data rate at 7 Gb/s.



NOTE: Output Voltage Amplitude (V_{OUTPP}) / RMS Jitter vs. Input Frequency (f_{in}) for 2:1 MUX Mode, Repetitive 1010 Input Data Pattern. *When an output level of 400 mV is desired and $V_{CC} - V_{EE} > 3.0$ V, a 2 k Ω resistor should be connected from OLS to V_{EE} .



NOTE: Output Voltage Amplitude (V_{OUTPP}) / RMS Jitter vs. Input Frequency (f_{in}) for 2:1 MUX Mode, Repetitive 1010 Input Data Pattern. *When an output level of 400 mV is desired and $V_{CC} - V_{EE} > 3.0$ V, a 2 k Ω resistor should be connected from OLS to V_{EE} .

Figure 8. ($V_{CC} - V_{EE} = 3.3 \text{ V} @ 25^{\circ}\text{C}$)



Figure 9. Typical OLS Input Current vs. OLS Input Voltage (V_{CC} – V_{EE} = 3.3 V @ 25°C)



Figure 10. OLS Operating Area



Figure 11. Differential Input Driven Single Ended



Figure 12. Differential Input Driven Differentially











Figure 15. VIHCMR Diagram



Figure 16. AC Reference Measurement



Figure 17. \mbox{SEL}_X to \mbox{Q}_X Timing Diagram

APPLICATION INFORMATION

All NB7L86A inputs can accept PECL, CML, LVTTL, LVCMOS and LVDS signal levels. The limitations for differential input signal (LVDS, PECL, or CML) are minimum input swing of 75 mV and the maximum input swing of 2500 mV. Within these conditions, the input

voltage can range from V_{CC} to 1.2 V. Examples interfaces are illustrated below in a 50 Ω environment (Z = 50 Ω). For output termination and interface, refer to application note AND8020/D.

Table 14. INTERFACING OPTIONS

INTERFACING OPTIONS	CONNECTIONS
CML	Connect VTD and VTD to V _{CC} (refer Figure 18)
LVDS	Connect VTD and VTD together. (refer Figure 19)
AC-COUPLED	Bias VTD and VTD inputs within the Common Mode range (V_{CMR}) (refer Figure 20)
RSECL, PECL, NECL	Standard ECL termination techniques (refer Figure 21)
LVTTL, LVCMOS	An external voltage (V _{THR}) should be applied to the unused complementary differential input. Nominal V _{THR} is 1.5 V for LVTTL and V _{CC} /2 for LVCMOS inputs. This voltage must be within the V _{THR} specification (refer Figure 22)



D

Figure 19. LVDS Interface

V_{EE}Ó

o V_{EE}



*Vbias must be within common mode range limits (V_{CMR})

Figure 20. PECL Interface



Figure 21. Typical termination for Output Driver and Device Evaluation (refer AND8020/D – termination of ECL Logic Devices)



Figure 22. LVCMOS/LVTTL Interface

ORDERING INFORMATION

Device	Package Type	Shipping [†]
NB7L86AMNG	QFN16 (Pb-Free / Halide-Free)	123 Units / Rail
NB7L86AMNHTBG	QFN16 (Pb-Free / Halide-Free)	100 / Tape & Reel

+For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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