

MOSFET – N-Channel, POWERTRENCH[®], SyncFET[™]

30 V, 22 A, 4.3 mΩ

FDMS0310AS

General Description

The FDMS0310AS has been designed to minimize losses in power conversion application. Advancements in both silicon and package technologies have been combined to offer the lowest $R_{DS(on)}$ while maintaining excellent switching performance. This device has the added benefit of an efficient monolithic Schottky body diode.

Features

- Max $R_{DS(on)} = 4.3 \text{ m}\Omega$ at $V_{GS} = 10 \text{ V}$, $I_D = 19 \text{ A}$
- Max $R_{DS(on)} = 5.2 \text{ m}\Omega$ at $V_{GS} = 4.5 \text{ V}$, $I_D = 17 \text{ A}$
- Advanced Package and Silicon Combination for Low R_{DS(on)} and High Efficiency
- SyncFET Schottky Body Diode
- MSL1 Robust Package Design
- 100% UIL Tested
- Pb-Free, Halide Free and RoHS Compliant

Applications

- Synchronous Rectifier for DC/DC Converters
- Notebook Vcore/GPU Low Side Switch
- Networking Point of Load Low Side Switch
- Telecom Secondary Side Rectification

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage (Note 4)	±20	V
I _D		22 80 19 100	A
E _{AS}	Single Pulse Avalanche Energy (Note 3)	33	mJ
P _D	Power Dissipation: $T_C = 25^{\circ}C$ $T_A = 25^{\circ}C$ (Note 1a)	41 2.5	W
T _J , T _{STG}	Operating and Storage Junction Temperature Range	–55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

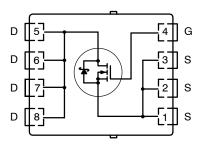
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V _{DS}	R _{DS(on)} MAX	I _D MAX
30 V	4.3 m Ω @ 10 V	22 A
	5.2 mΩ @ 4.5 V	



PQFN8 5 × 6, 1.27P (Power 56) CASE 483AE

ELECTRICAL CONNECTION



N-CHANNEL MOSFET

MARKING DIAGRAM

&Z&3&K FDMS 0310AS

&Z = Assembly Plant Code &3 = 3-Digit Date Code (Year and Week) &K = 2-Digit Lot Run Code FDMS0310AS = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping [†]
FDMS0310AS	PQFN8 5X6, 1.27P (Pb-Free, Halide Free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{ heta JC}$	Thermal Resistance, Junction to Case	3.0	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Тур	Max	Unit
OFF CHARA	ACTERISTICS		•		•	
BV _{DSS}	Drain to Source Breakdown Voltage	I _D = 1 mA, V _{GS} = 0 V	30	-	_	V
BV _{DSST}	Drain to Source Breakdown Voltage Transient	V _{GS} = 0 V, Transient = 100 ns	33	-	-	٧
$\frac{\Delta BV_{DSS}}{\Delta T_{J}}$	Breakdown Voltage Temperature Coefficient	I _D = 10 mA, Referenced to 25°C	-	23	-	mV/°C
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} = 24 V, V _{GS} = 0 V	-	-	500	μΑ
I _{GSS}	Gate to Source Leakage Current, Forward	V _{GS} = 20 V, V _{DS} = 0 V	_	-	100	nA
ON CHARA	CTERISTICS (Note 2)					
V _{GS(th)}	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 1 \text{ mA}$	1.2	1.5	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I _D = 10 mA, Referenced to 25°C	-	-4	-	mV/°C
R _{DS(on)}	Static Drain to Source On Resistance	V _{GS} = 10 V, I _D = 19 A	-	3.6	4.3	mΩ
		V _{GS} = 4.5 V, I _D = 17 A	-	4.5	5.2]
		V _{GS} = 10 V, I _D = 19 A, T _J = 125°C	-	4.8	6.0	
9FS	Forward Transconductance	V _{DS} = 5 V, I _D = 19 A	-	103	-	S
DYNAMIC C	HARACTERISTICS					
C _{iss}	Input Capacitance	V _{DS} = 15 V, V _{GS} = 0 V, f = 1 MHz	-	1715	2280	pF
C _{oss}	Output Capacitance		_	655	870	pF
C _{rss}	Reverse Transfer Capacitance		-	75	110	pF
R _g	Gate Resistance		-	0.7	2.5	Ω
SWITCHING	CHARACTERISTICS					
t _{d(on)}	Turn-On Delay Time	$V_{DD} = 15 \text{ V}, I_D = 19 \text{ A}, V_{GS} = 10 \text{ V},$	-	9.0	18	ns
t _r	Rise Time	$R_{GEN} = 6 \Omega$	-	3.9	10	ns
t _{d(off)}	Turn-Off Delay Time		-	25	40	ns
t _f	Fall Time		-	3.2	10	ns
Qg	Total Gate Charge	$V_{GS} = 0 \text{ V to } 10 \text{ V}, V_{DD} = 15 \text{ V}, I_D = 19 \text{ A}$	-	27	37	nC
		$V_{GS} = 0 \text{ V to } 4.5 \text{ V}, V_{DD} = 15 \text{ V}, I_D = 19 \text{ A}$	-	13	19	nC
Q _{gs}	Gate to Source Charge	V _{DD} = 15 V, I _D = 19 A	_	4.2	-	nC
Q _{gd}	Gate to Drain "Miller" Charge	V _{DD} = 15 V, I _D = 19 A	_	3.7	_	nC

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted) (continued)

Symbol	Parameter	Test Condition	Min	Тур	Max	Unit
DRAIN-SOURCE DIODE CHARACTERISTICS						
V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _S = 2 A (Note 2)	-	0.6	0.8	V
		V _{GS} = 0 V, I _S = 19 A (Note 2)	-	0.8	1.2	
t _{rr}	Reverse Recovery Time	I _F = 19 A, di/dt = 300 A/μs	-	24	38	ns
Q _{rr}	Reverse Recovery Charge		-	24	38	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 50°C/W when mounted on a 1 in² pad of 2 oz copper.



b) 125°C/W when mounted on a minimum pad of 2 oz copper.

- Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
 E_{AS} of 33 mJ is based on starting T_J = 25°C, L = 0.3 mH, I_{AS} = 15 A, V_{DD} = 27 V, V_{GS} = 10 V.
 As an N-ch device, the negative Vgs rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

TYPICAL CHARACTERISTICS

(T_J = 25°C unless otherwise noted)

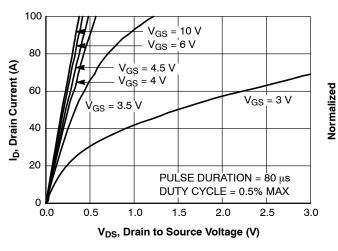


Figure 1. On Region Characteristics

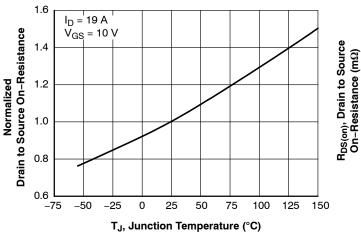


Figure 3. Normalized On–Resistance vs. Junction Temperature

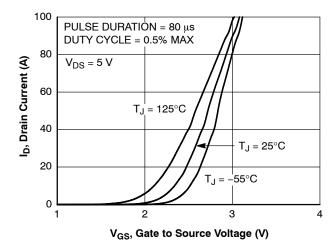


Figure 5. Transfer Characteristics

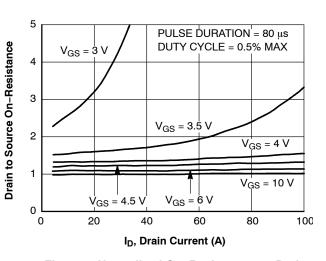


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

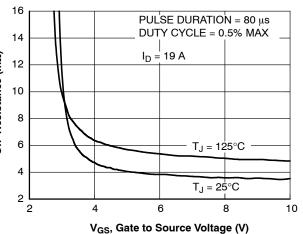


Figure 4. On-Resistance vs. Gate to Source Voltage

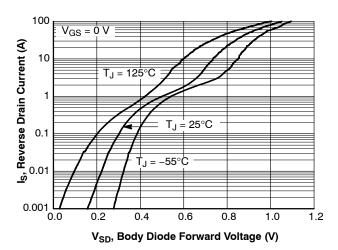


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (continued)

(T_J = 25°C unless otherwise noted)

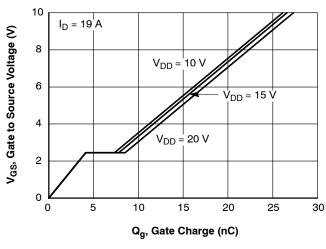


Figure 7. Gate Charge Characteristics

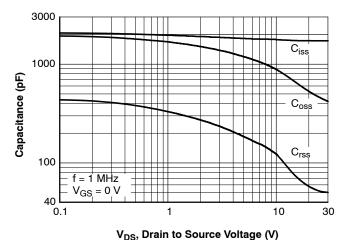


Figure 8. Capacitance vs. Drain to Source Voltage

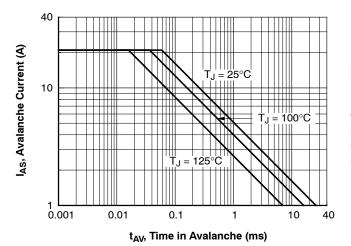


Figure 9. Unclamped Inductive Switching Capability

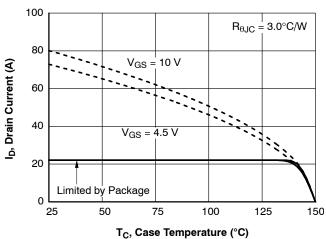


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

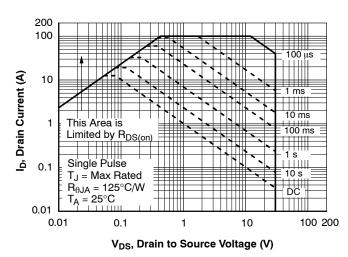


Figure 11. Forward Bias Safe Operating Area

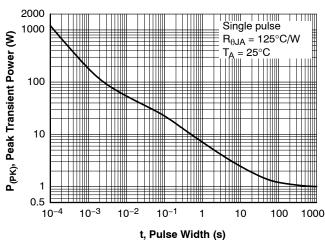


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (continued)

 $(T_J = 25^{\circ}C \text{ unless otherwise noted})$

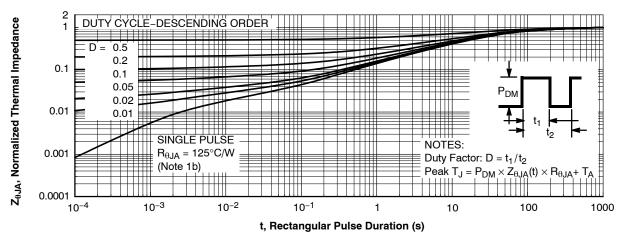


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

TYPICAL CHARACTERISTICS (continued)

SyncFET Schottky Body Diode Characteristics

onsemi's SyncFET process embeds a Schottky diode in parallel with POWERTRENCH MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 14 shows the reverse recovery characteristic of the FDMS0310AS.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

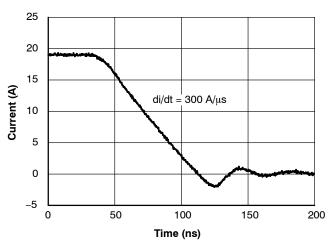


Figure 14. FDMS0310AS SyncFET Body Diode Reverse Recovery Characteristics

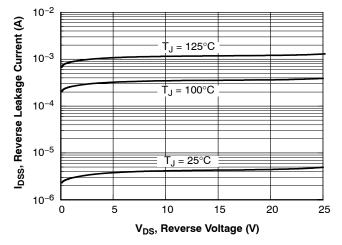


Figure 15. SyncFET Body Diode Reverse Leakage vs. Drain-Source Voltage

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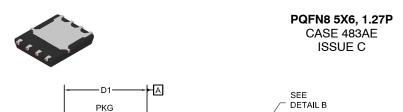
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PKG &

PIN 1

AREA



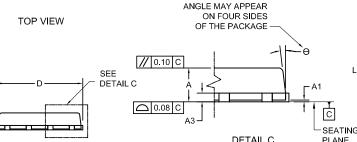


В

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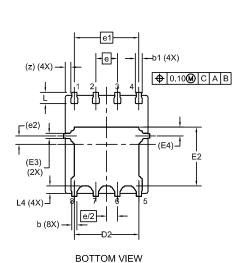
NOTES:

- 1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
- 2. CONTROLLING DIMENSION: MILLIMETERS
- 3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
- 4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
- 5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
- 6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

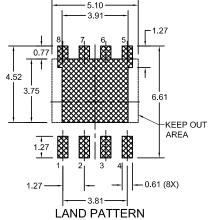


OPTIONAL DRAFT

L2· SEATING **DETAIL B DETAIL C** PLANE SCALE: 2:1 SCALE: 2:1



SIDE VIEW



*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

RECOMMENDATION

DIM	MILLIMETERS			
Diwi	MIN.	NOM.	MAX.	
Α	0.90	1.00	1.10	
A1	0.00	-	0.05	
b	0.21	0.31	0.41	
b1	0.31	0.41	0.51	
А3	0.15	0.25	0.35	
D	4.90	5.00	5.20	
D1	4.80	4.90	5.00	
D2	3.61	3.82	3.96	
Е	5.90	6.15	6.25	
E1	5.70	5.80	5.90	
E2	3.38	3.48	3.78	
E3	(0.30 REF		
E4	(0.52 REF		
е	,	1.27 BSC	;	
e/2	Ū	0.635 BS	С	
e1	• •	3.81 BSC	;	
e2	Ú	0.50 REF	:	
L	0.51	0.66	0.76	
L2	0.05	0.18	0.30	
L4	0.34	0.44	0.54	
Z	0.34 REF			
θ	0°	_	12°	

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