Hex Non-Inverting 3-State Buffer

The MC14503B is a hex non-inverting buffer with 3-state outputs, and a high current source and sink capability. The 3-state outputs make it useful in common bussing applications. Two disable controls are provided. A high level on the Disable A input causes the outputs of buffers 1 through 4 to go into a high impedance state and a high level on the Disable B input causes the outputs of buffers 5 and 6 to go into a high impedance state.

Features

- 3-State Outputs
- TTL Compatible Will Drive One TTL Load Over Full Temperature Range
- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- Two Disable Controls for Added Versatility
- Pin for Pin Replacement for MM80C97 and 340097
- Pb–Free Packages are Available*

MAXIMUM RATINGS (Voltages Referenced to V_{SS}) (Note 1)

Parameter	Symbol	Value	Unit
DC Supply Voltage Range	V _{DD}	-0.5 to +18.0	V
Input or Output Voltage Range (DC or Transient)	V _{in} , V _{out}	-0.5 to V _{DD} + 0.5	V
Input Current (DC or Transient) per Pin	l _{in}	±10	mA
Output Current (DC or Transient) per Pin	l _{out}	±25	mA
Power Dissipation, per Package (Note 2)	PD	500	mW
Ambient Temperature Range	T _A	-55 to +125	°C
Storage Temperature Range		-65 to +150	°C
Lead Temperature (8–Second Soldering)		260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Maximum Ratings are those values beyond which damage to the device may occur.

2. Temperature Derating:

Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high–impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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MARKING DIAGRAMS



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

PIN ASSIGNMENT

DIS A [1•	16	D V _{DD}
IN 1 [2	15] DIS B
OUT 1 [3	14] IN 6
IN 2 [4	13	
OUT 2 [5	12] IN 5
IN 3 [6	11] OUT 5
OUT 3 [7	10] IN 4
V _{SS} [8	9	

LOGIC DIAGRAM

15 DISABLE B o IN 5 0¹² 0 OUT 5 13 0 OUT 6 IN 60¹⁴ 3 OUT 1 2 IN 1 O 5 OUT 2 4 IN 2 O 7 OUT 3 IN 3 0 6 9 OUT 4 IN 4 0¹⁰ 1 DISABLE A O V_{DD} = PIN 16 V_{SS} = PIN 8

TRUTH TABLE

In _n	Appropriate Disable Input	Out _n
0	0	0
1	0	1
X	1	High Impedance

X = Don't Care

CIRCUIT DIAGRAM



*Diode protection on all inputs (not shown)

ORDERING INFORMATION

Device	Package	Shipping [†]
MC14503BCP	PDIP-16	
MC14503BCPG	PDIP-16 (Pb-Free)	25 / Rail
MC14503BD	SOIC-16	
MC14503BDG	SOIC-16 (Pb-Free)	48 / Rail
MC14503BDR2	SOIC-16	
MC14503BDR2G	SOIC-16 (Pb-Free)	2500 / Tape & Reel
MC14503BFEL	SOEIAJ-16	
MC14503BFELG	SOEIAJ-16 (Pb-Free)	2000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

				- 5	5°C		25°C		125	S°C	
Characteristic		Symbol	V _{DD} Vdc	Min	Мах	Min	Typ (Note 3)	Max	Min	Max	Unit
Output Voltage V _{in} = 0	"0" Level	V _{OL}	5.0 10 15	_ _ _	0.05 0.05 0.05	- - -	0 0 0	0.05 0.05 0.05	- - -	0.05 0.05 0.05	Vdc
V _{in} = V _{DD}	"1" Level	V _{OH}	5.0 10 15	4.95 9.95 14.95	- - -	4.95 9.95 14.95	5.0 10 15		4.95 9.95 14.95	- - -	Vdc
Input Voltage $(V_O = 3.6 \text{ or } 1.4 \text{ Vdc})$ $(V_O = 7.2 \text{ or } 2.8 \text{ Vdc})$ $(V_O = 11.5 \text{ or } 3.5 \text{ Vdc})$	"0" Level	V _{IL}	5.0 10 15	- - -	1.5 3.0 4.0	- - -	2.25 4.50 6.75	1.5 3.0 4.0	- - -	1.5 3.0 4.0	Vdc
$(V_{O} = 1.4 \text{ or } 3.6 \text{ Vdc})$ $(V_{O} = 2.8 \text{ or } 7.2 \text{ Vdc})$ $(V_{O} = 3.5 \text{ or } 11.5 \text{ Vdc})$	"1" Level	V _{IH}	5.0 10 15	3.5 7.0 11		3.5 7.0 11	2.75 5.50 8.25		3.5 7.0 11	- -	Vdc
Output Drive Current $(V_{OH} = 2.5 \text{ Vdc})$ $(V_{OH} = 2.5 \text{ Vdc})$ $(V_{OH} = 4.6 \text{ Vdc})$ $(V_{OH} = 9.5 \text{ Vdc})$ $(V_{OH} = 13.5 \text{ Vdc})$ $(V_{OH} = 13.5 \text{ Vdc})$	Source	I _{ОН}	4.5 5.0 5.0 10 15	- 4.3 - 5.8 - 1.2 - 3.1 - 8.2	- - - -	- 3.6 - 4.8 - 1.02 - 2.6 - 6.8	- 5.0 - 6.1 - 1.4 - 3.7 - 14.1		- 2.5 - 3.0 - 0.7 - 1.8 - 4.8	- - - -	mAdc
(V _{OL} = 0.4 Vdc) (V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Sink	I _{OL}	4.5 5.0 10 15	2.2 2.6 6.5 19.2		1.8 2.1 5.5 16.1	2.1 2.3 6.2 25		1.2 1.3 3.8 11.2		mAdc
Input Current		l _{in}	15	-	± 0.1	-	±0.00001	± 0.1	-	± 1.0	μAdc
Input Capacitance, (V _{in} = 0)	C _{in}	-	-	-	-	5.0	7.5	-	-	pF
Quiescent Current, (Per Pa	ackage)	lQ	5.0 10 15		1.0 2.0 4.0	- - -	0.002 0.004 0.006	1.0 2.0 4.0	_ _ _	30 60 120	μAdc
Total Supply Current (Note 4, 5) (Dynamic plus Quiescent, Per Package) (C_L = 50 pF on all outputs) (All outputs switching, 50% Duty Cycle)		Ι _Τ	5.0 10 15		<u>.</u>	$I_{T} = (6)$.5 μA/kHz) f 5.0 μA/kHz) f 10 μA/kHz) f	+ I _{DD}	<u> </u>	<u> </u>	μAdc
3-State Output Leakage C	urrent	I _{TL}	15	_	± 0.1	-	± 0.0001	± 0.1	-	± 3.0	μAdc

Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.
 The formulas given are for the typical characteristics only at 25°C.
 To calculate total supply current at loads other than 50 pF: I_T(C_L) = I_T(50 pF) + (C_L - 50) Vfk where: I_T is in μA (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.006.

SWITCHING CHARACTERISTICS (Note 6) (C_L = 50 pF, T_A = 25°C)

			All Ty	pes	
Characteristic	Symbol	V _{DD} V _{CC}	Typ (Note 7)	Max	Unit
Output Rise Time $t_{TLH} = (0.5 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{TLH} = (0.3 \text{ ns/pF}) C_L + 8.0 \text{ ns}$ $t_{TLH} = (0.2 \text{ ns/pF}) C_L + 8.0 \text{ ns}$	t _{TLH}	5.0 10 15	45 23 18	90 45 35	ns
Output Fall Time $t_{THL} = (0.5 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{THL} = (0.3 \text{ ns/pF}) C_L + 8.0 \text{ ns}$ $t_{THL} = (0.2 \text{ ns/pF}) C_L + 8.0 \text{ ns}$	t _{THL}	5.0 10 15	45 23 18	90 45 35	ns
Turn–Off Delay Time, all Outputs $t_{PLH} = (0.3 \text{ ns/pF}) C_L + 60 \text{ ns}$ $t_{PLH} = (0.15 \text{ ns/pF}) C_L + 27 \text{ ns}$ $t_{PLH} = (0.1 \text{ ns/pF}) C_L + 20 \text{ ns}$	t _{PLH}	5.0 10 15	75 35 25	150 70 50	ns
Turn–On Delay Time, all Outputs $t_{PHL} = (0.3 \text{ ns/pF}) C_L + 60 \text{ ns}$ $t_{PHL} = (0.15 \text{ ns/pF}) C_L + 27 \text{ ns}$ $t_{PHL} = (0.1 \text{ ns/pF}) C_L + 20 \text{ ns}$	tphl	5.0 10 15	75 35 25	150 70 50	ns
3–State Propagation Delay Time Output "1" to High Impedance	t _{PHZ}	5.0 10 15	75 40 35	150 80 70	ns
Output "0" to High Impedance	t _{PLZ}	5.0 10 15	80 40 35	160 80 70	ns
High Impedance to "1" Level	t _{PZH}	5.0 10 15	65 25 20	130 50 40	ns
High Impedance to "0" Level	t _{PZL}	5.0 10 15	100 35 25	200 70 50	ns

6. The formulas given are for the typical characteristics only at 25°C.
7. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.





Figure 1. Switching Time Test Circuit and Waveforms (t_{TLH}, t_{THL}, t_{PHL}, and t_{PLH})







PACKAGE DIMENSIONS

PDIP-16 CASE 648-08 ISSUE T



- NOTES: 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982. 2. CONTROLLING DIMENSION: INCH. 3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL. 4. DIMENSION B DOES NOT INCLUDE MOLD ELASH

- MOLD FLASH. 5. ROUNDED CORNERS OPTIONAL.

	INC	HES	MILLIN	IETERS	
DIM	MIN	MAX	MIN	MAX	
Α	0.740	0.770	18.80	19.55	
В	0.250	0.270	6.35	6.85	
С	0.145	0.175	3.69	4.44	
D	0.015	0.021	0.39	0.53	
F	0.040	0.70	1.02	1.77	
G	0.100	BSC	2.54 BSC		
н	0.050	BSC	1.27 BSC		
J	0.008	0.015	0.21	0.38	
κ	0.110	0.130	2.80	3.30	
L	0.295	0.305	7.50	7.74	
М	0 °	10 °	0 °	10 °	
S	0.020	0.040	0.51	1.01	

SOIC-16 CASE 751B-05 **ISSUE J**



NOTES:

- NO LES:

 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

 2. CONTROLLING DIMENSION: MILLIMETER.

 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.

 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006)

- MAXIMUM MOLD PHOTHUSIUM 0.13 (0.000) PER SIDE. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION. SHALL BE 0.127 (0.005) TAAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION. 5.

	MILLIN	IETERS	INC	HES
DIM	MIN	MIN MAX		MAX
Α	9.80	10.00	0.386	0.393
В	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27	1.27 BSC		BSC
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
М	0 °	7°	0°	7°
Р	5.80	6.20	0.229	0.244
R	0.25	0.50	0.010	0.019

PACKAGE DIMENSIONS

SOEIAJ-16 CASE 966-01 ISSUE A



 \frown

0.10 (0.004)

е

⊕ 0.13 (0.005) M





NOTES:

- DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
- CONTROLLING DIMENSION: MILLIMETER.
 DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE
- MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE. 4. TERMINAL NUMBERS ARE SHOWN FOR
- TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
 THE LEAD WIDTH DIMENSION (b) DOES NOT
- 5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

			-	
	MILLIN	IETERS	INC	HES
DIM	MIN	MIN MAX		MAX
Α		2.05		0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.10	0.20	0.007	0.011
D	9.90	10.50	0.390	0.413
Е	5.10	5.45	0.201	0.215
e	1.27	1.27 BSC) BSC
HE	7.40	8.20	0.291	0.323
L	0.50	0.85	0.020	0.033
LE	1.10	1.50	0.043	0.059
М	0 °	10 °	0 °	10 °
Q1	0.70	0.90	0.028	0.035
Z		0.78		0.031

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