

NB7L14

2.5V / 3.3V 7GHz/10Gbps Differential 1:4 LVPECL Fanout Buffer

Multi-Level Inputs w/ Internal Termination

Description

The NB7L14 is a differential 1:4 LVPECL fanout buffer. The NB7L14 produces four identical LVPECL output copies of Clock or Data operating up to 7 GHz or 10.7 Gb/s, respectively. As such, the NB7L14 is ideal for SONET, GigE, Fiber Channel, Backplane and other Clock or Data distribution applications.

The differential inputs incorporate internal 50 Ω termination resistors that are accessed through the VT Pin. This feature allows the NB7L14 to accept various logic standards, such as LVPECL, CML, LVDS, LVCMOS or LVTTL logic levels. The V_{REFAC} reference output can be used to rebias capacitor-coupled differential or single-ended input signals. The 1:4 fanout design was optimized for low output skew applications.

The NB7L14 is a member of the GigaComm™ family of high performance clock products.

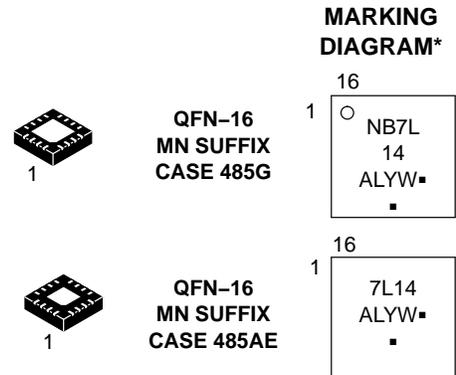
Features

- Input Data Rate > 10.7 Gb/s
- Input Clock Frequency > 7 GHz
- 165 ps Typical Propagation Delay
- 45 ps Typical Rise and Fall Times
- <15 ps max Output Skew
- <0.8 ps maximum RMS Clock Jitter
- <15 ps pp of Data Dependent Jitter
- Differential LVPECL Outputs, 720 mV peak-to-peak, typical
- LVPECL Operating Range: V_{CC} = 2.375 V to 3.6 V with GND = 0 V
- NECL Operating Range: V_{CC} = 0 V with GND = -2.375 V to -3.6 V
- Internal Input Termination Resistors, 50 Ω
- V_{REFAC} Reference Output
- Functionally Compatible with Existing 2.5 V / 3.3 V LVEL, LVEP, EP, and SG Devices
- -40°C to +85°C Ambient Operating Temperature
- These are Pb-Free Devices



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XXXX = Specific Device Code
 A = Assembly Location
 L = Wafer Lot
 Y = Year
 W = Work Week
 ■ = Pb-Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

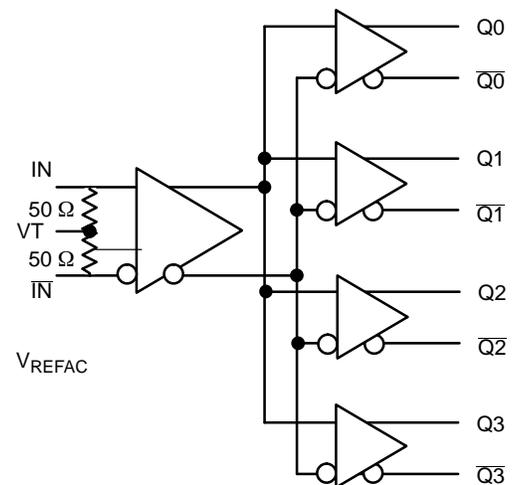


Figure 1. Logic Diagram

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 10 of this data sheet.

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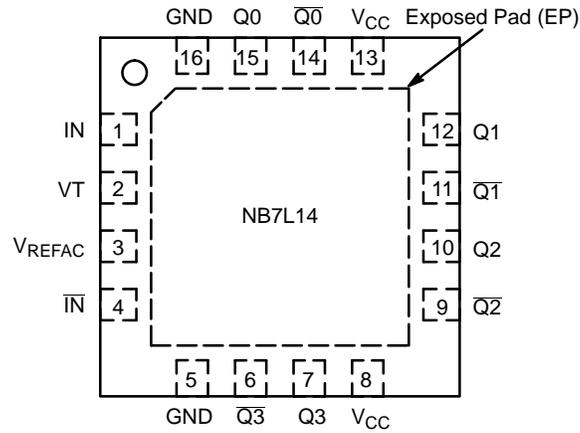


Figure 2. QFN-16 Pinout (Top View)

Table 1. PIN DESCRIPTION

| Pin | Name | I/O | Description |
|-----|------------------------|--------------------------------------|--|
| 1 | IN | ECL, CML, LVCMOS, LVDS, LVTTTL Input | Non-inverted Differential Input. Note 1. Internal 50 Ω Resistor to Termination Pin, VT |
| 2 | VT | - | Internal 50- Ω Termination Pin for IN/ $\overline{\text{IN}}$ inputs. |
| 3 | VREFAC | | Output Reference Voltage for capacitor-coupled inputs |
| 4 | $\overline{\text{IN}}$ | ECL, CML, LVCMOS, LVDS, LVTTTL Input | Inverted Differential Input. Note 1. Internal 50 Ω Resistor to Termination Pin, VT. |
| 5 | GND | - | Negative Supply Voltage |
| 6 | $\overline{\text{Q3}}$ | LVPECL Output | Inverted Differential Output. Typically Terminated with 50 Ω Resistor to $V_{\text{CC}} - 2.0 \text{ V}$. |
| 7 | Q3 | LVPECL Output | Non-inverted Differential Output. Typically Terminated with 50 Ω Resistor to $V_{\text{CC}} - 2.0 \text{ V}$. |
| 8 | VCC | - | Positive Supply Voltage |
| 9 | $\overline{\text{Q2}}$ | LVPECL Output | Inverted Differential Output. Typically Terminated with 50 Ω Resistor to $V_{\text{CC}} - 2.0 \text{ V}$. |
| 10 | Q2 | LVPECL Output | Non-inverted Differential Output. Typically Terminated with 50 Ω Resistor to $V_{\text{CC}} - 2.0 \text{ V}$. |
| 11 | $\overline{\text{Q1}}$ | LVPECL Output | Inverted Differential Output. Typically Terminated with 50 Ω Resistor to $V_{\text{CC}} - 2.0 \text{ V}$. |
| 12 | Q1 | LVPECL Output | Non-inverted Differential Output. Typically Terminated with 50 Ω Resistor to $V_{\text{CC}} - 2.0 \text{ V}$. |
| 13 | VCC | - | Positive Supply Voltage |
| 14 | $\overline{\text{Q0}}$ | LVPECL Output | Inverted Differential Output. Typically Terminated with 50 Ω Resistor to $V_{\text{CC}} - 2.0 \text{ V}$. |
| 15 | Q0 | LVPECL Output | Non-inverted Differential Output. Typically Terminated with 50 Ω Resistor to $V_{\text{CC}} - 2.0 \text{ V}$. |
| 16 | GND | - | Negative Supply Voltage |
| - | EP | - | The Exposed Pad (EP) on the QFN-16 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat-sinking conduit. The pad is electrically connected to the die, and must be electrically connected to device GND. |

1. In the differential configuration when the input termination pin (VT) is connected to a common termination voltage or left open, and if no signal is applied on IN/ $\overline{\text{IN}}$ input, then, the device will be susceptible to self-oscillation.
2. All VCC and GND pins must be externally connected to a power supply for proper operation.

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Table 2. ATTRIBUTES

| Characteristics | | Value |
|--|-----------------------------------|----------------------|
| ESD Protection | Human Body Model Machine Model | > 2000 V > 150 V |
| Moisture Sensitivity (Note 3) | QFN-16 | Level 1 |
| Flammability Rating | Oxygen Index: 28 to 34 | UL 94 V-0 @ 0.125 in |
| Transistor Count | | 173 |
| Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test | | |

3. For additional information, see Application Note AND8003/D.

Table 3. MAXIMUM RATINGS

| Symbol | Parameter | Condition 1 | Condition 2 | Rating | Unit |
|---------------------|--|---------------------|--|----------------|------|
| V _{CC} | Positive Power Supply | GND = 0 V | | -0.5 V to +4.0 | V |
| V _{IO} | Positive Input/Output Voltage | GND = 0 V | -0.5 ≤ V _{IO} ≤ V _{CC} + 0.5 | 4.0 | V |
| V _{INPP} | Differential Input Voltage D - \bar{D} | | | 2.8 | V |
| I _{IN} | Input Current Through R _T (50 Ω Resistor) | | | ±40 | mA |
| I _{OUT} | Output Current (LVPECL Output) | Continuous Surge | | 50 100 | mA |
| I _{VREFAC} | V _{REFAC} Sink/Source Current | | | ±1.5 | mA |
| T _A | Operating Temperature Range | QFN-16 | | -40 to +85 | °C |
| T _{stg} | Storage Temperature Range | | | -65 to +150 | °C |
| θ _{JA} | Thermal Resistance (Junction-to-Ambient) (Note 4) | 0 lfpm 500 lfpm | QFN-16 QFN-16 | 42 35 | °C/W |
| θ _{JC} | Thermal Resistance (Junction-to-Case) (Note 4) | | QFN-16 | 4 | °C/W |
| T _{sol} | Wave Solder Pb-Free | | | 265 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

4. JEDEC standard multilayer board – 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

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Table 4. DC CHARACTERISTICS, MULTI-LEVEL INPUTS $V_{CC} = 2.375\text{ V to }3.6\text{ V}$, $GND = 0\text{ V}$, $T_A = -40^\circ\text{C to }+85^\circ\text{C}$

| Symbol | Characteristic | Min | Typ | Max | Unit | |
|--|---|--|---------------------------------|--------------------------------|---------------------------------|---------------|
| POWER SUPPLY CURRENT | | | | | | |
| V_{CC} | Power Supply Voltage | $V_{CC} = 2.5\text{ V}$ $V_{CC} = 3.3\text{ V}$ | 2.375 3.0 | 2.5 3.3 | 2.625 3.6 | V |
| I_{CC} | Power Supply Current (Inputs and Outputs Open) | | | 85 | 105 | mA |
| LVPECL OUTPUTS (Notes 5 & 6) | | | | | | |
| V_{OH} | Output HIGH Voltage | $V_{CC} = 2.5\text{ V}$ $V_{CC} = 3.3\text{ V}$ | $V_{CC} - 1145$ 1355 2155 | $V_{CC} - 900$ 1600 2400 | $V_{CC} - 825$ 1675 2475 | mV |
| V_{OL} | Output LOW Voltage | $V_{CC} = 2.5\text{ V}$ $V_{CC} = 3.3\text{ V}$ | $V_{CC} - 2000$ 500 1300 | $V_{CC} - 1700$ 800 1600 | $V_{CC} - 1500$ 1000 1800 | mV |
| DIFFERENTIAL INPUT DRIVEN SINGLE-ENDED (see Figure 5 & 7) (Note 7) | | | | | | |
| V_{IH} | Single-ended Input HIGH Voltage | | $V_{th} + 75$ | | V_{CC} | mV |
| V_{IL} | Single-ended Input LOW Voltage | | GND | | $V_{th} - 75$ | mV |
| V_{th} | Input Threshold Reference Voltage Range (Note 8) | | 1125 | | $V_{CC} - 75$ | mV |
| V_{ISE} | Single-ended Input Voltage Amplitude ($V_{IH} - V_{IL}$) | | 150 | | 2800 | mV |
| VREFAC | | | | | | |
| V_{REFAC} | Output Reference Voltage (100 μA Load) | | $V_{CC} - 1400$ | $V_{CC} - 1300$ | $V_{CC} - 1000$ | mV |
| DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (see Figure 6 & 8) (Note 9) | | | | | | |
| V_{IHD} | Differential Input HIGH Voltage | | 1200 | | V_{CC} | mV |
| V_{ILD} | Differential Input LOW Voltage | | 0 | | $V_{IHD} - 50$ | mV |
| V_{ID} | Differential Input Voltage ($V_{IHD} - V_{ILD}$) | | 100 | | 2800 | mV |
| V_{CMR} | Input Common Mode Range (Differential Configuration) (Note 10) (Figure 9) | | 950 | | $V_{CC} - 50$ | mV |
| I_{IH} | Input HIGH Current $I_N / \overline{I_N}$, (VT Open) | | -150 | | 150 | μA |
| I_{IL} | Input LOW Current $I_N / \overline{I_N}$, (VT Open) | | -150 | | 150 | μA |
| TERMINATION RESISTORS | | | | | | |
| R_{TIN} | Internal Input Termination Resistor | | 45 | 50 | 55 | Ω |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- LVPECL outputs loaded with 50 Ω to $V_{CC} - 2.0\text{ V}$ for proper operation.
- Input and output parameters vary 1:1 with V_{CC} .
- V_{th} , V_{IH} , V_{IL} , and V_{ISE} parameters must be complied with simultaneously.
- V_{th} is applied to the complementary input when operating in single-ended mode.
- V_{IHD} , V_{ILD} , V_{ID} and V_{CMR} parameters must be complied with simultaneously.
- V_{MR} min varies 1:1 with V_{EE} , V_{CMR} max varies 1:1 with V_{CC} . The V_{CMR} range is referenced to the most positive side of the differential input signal.

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Table 5. AC CHARACTERISTICS $V_{CC} = 2.375\text{ V to }3.6\text{ V}$, $GND = 0\text{ V}$, $T_A = -40^\circ\text{C to }+85^\circ\text{C}$; (Note 11)

| Symbol | Characteristic | Min | Typ | Max | Unit | |
|--------------------------|--|--|------------|----------------|-----------|--------------------|
| f_{MAX} | Maximum Input Clock Frequency; $V_{OUT} \geq 400\text{ mV}$ | 7 | 8 | | GHz | |
| $f_{DATAMAX}$ | Maximum Operating Data Rate; NRZ, (PRBS23) | 10 | 11 | | Gbps | |
| V_{OUTPP} | Output Voltage Amplitude (Note 15) (See Figure 9) | $f_{in} \leq 5\text{ GHz}$ 400 | 720 450 | | mV | |
| t_{PLH} , t_{PHL} | Propagation Delay IN to Q | 125 | 165 | 200 | ps | |
| t_{SKEW} | Duty Cycle Skew (Note 12) Output – Output Within Device Skew Device to Device Skew | | 3 | 15 15 50 | ps | |
| t_{DC} | Output Clock Duty Cycle (Reference Duty Cycle = 50%) | $f_{in} \leq 7\text{ GHz}$ | 45 | 50 | 55 | % |
| t_{JITTER} | RMS Random Clock Jitter (Note 13) Peak-to-Peak Data Dependent Jitter (Note 14) | $f_{in} \leq 7\text{ GHz}$ $f_{in} \leq 10.7\text{ Gb/s}$ | | 0.5 5 | 0.8 15 | ps rms ps pk-pk |
| $t_{jit}(\phi)$ | Additive RMS Phase Jitter $f_c = 622.08\text{ MHz}$, Integration Range: 12 kHz to 20 MHz (See Figure 17) | | 24 | | fs | |
| V_{INPP} | Input Voltage Swing/Sensitivity (Differential Configuration) (Note 15) | 100 | | 1200 | mV | |
| t_r t_f | Output Rise/Fall Times @ 1.0 GHz (20% – 80%) | Qx, \overline{Qx} | 30 | 45 | 60 | ps |

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

11. Measured by forcing $V_{INPP}(\text{min})$ from a 50% duty cycle clock source. All loading with an external $R_L = 50\ \Omega$ to $V_{CC} - 2.0\text{ V}$. Input edge rates 40 ps (20% – 80%).
12. Skew is measured between outputs under identical transitions and conditions @ 0.5 GHz. Duty cycle skew is measured between differential outputs using the deviations of the sum of T_{pw-} and T_{pw+} @ 0.5 GHz.
13. Additive RMS jitter with 50% duty cycle clock signal.
14. Additive peak-to-peak data dependent jitter with input NRZ data at PRBS23.
15. Input and output voltage swing is a single-ended measurement operating in differential mode.

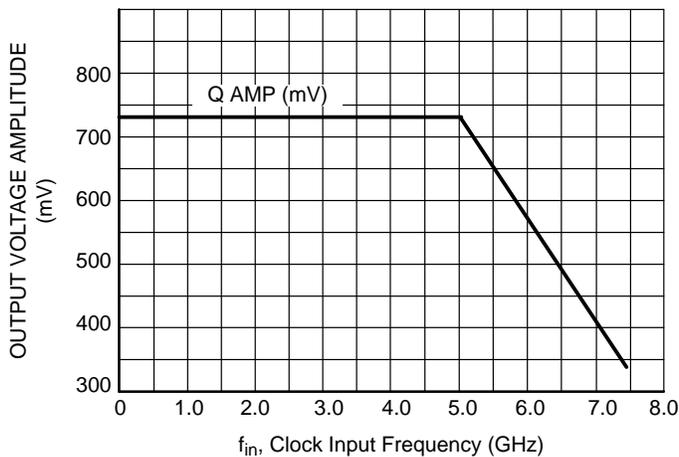


Figure 3. CLOCK Output Voltage Amplitude (V_{OUTPP}) vs. Input Frequency (f_{in}) at Ambient Temperature (Typ)

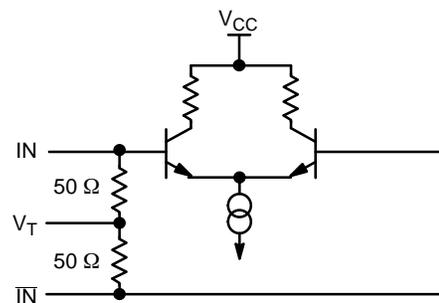


Figure 4. Input Structure

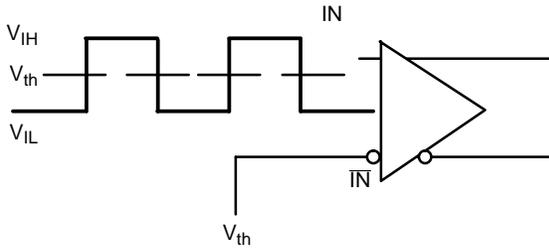


Figure 5. Differential Input Driven Single-Ended

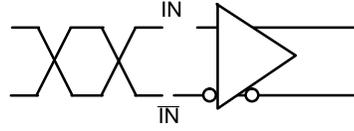


Figure 6. Differential Inputs Driven Differentially

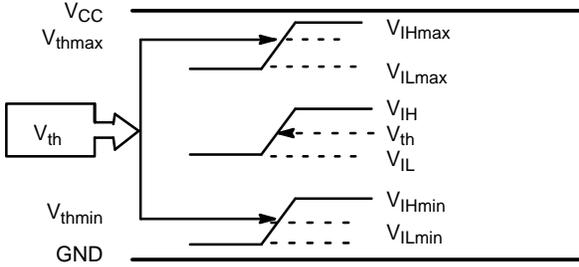


Figure 7. V_{th} Diagram

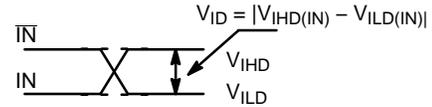


Figure 8. Differential Inputs Driven Differentially

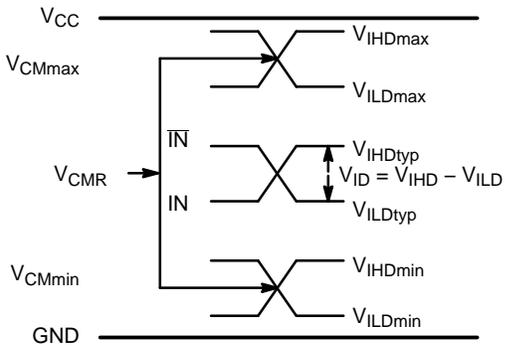


Figure 9. V_{CMR} Diagram

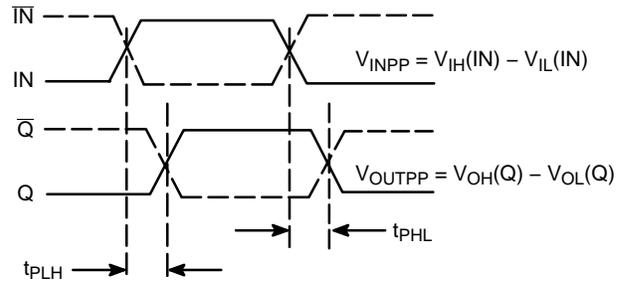


Figure 10. AC Reference Measurement

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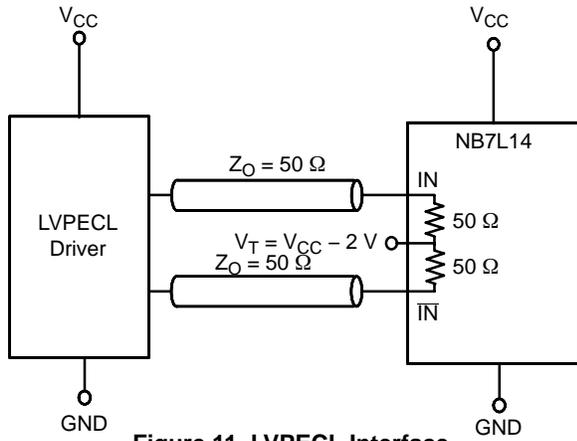


Figure 11. LVPECL Interface

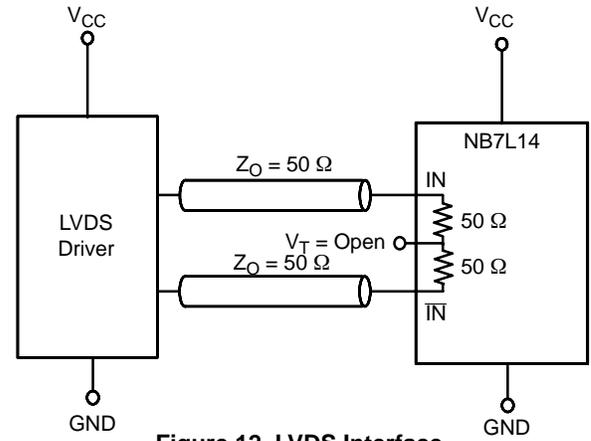


Figure 12. LVDS Interface

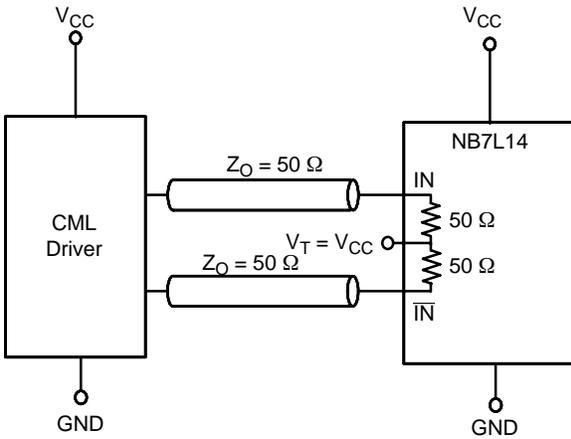


Figure 13. Standard 50 Ω Load CML Interface

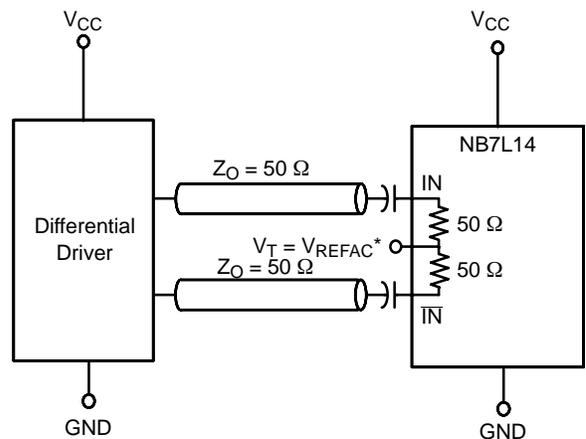


Figure 14. Capacitor-Coupled Differential Interface

(V_T Connected to External V_{REFAC})

* V_{REFAC} bypassed to ground with a 0.01 μF capacitor

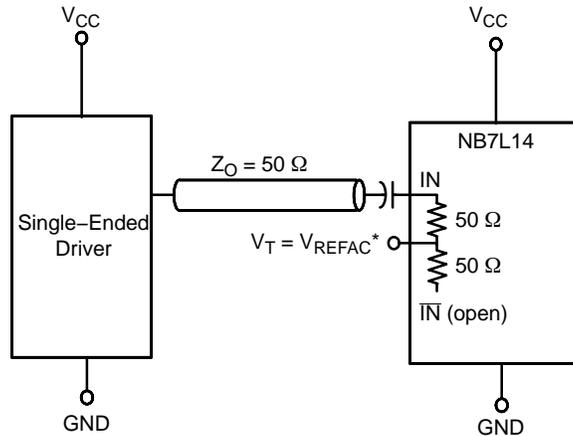
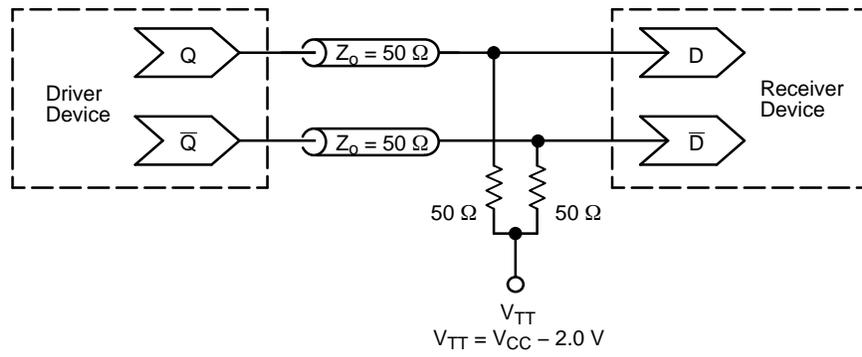


Figure 15. Capacitor-Coupled Differential Interface (V_T Connected to External V_{REFAC})

* V_{REFAC} bypassed to ground with a 0.01 μF capacitor

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**Figure 16. Typical Termination for Output Driver and Device Evaluation
(See Application Note AND8020/D – Termination of ECL Logic Devices.)**

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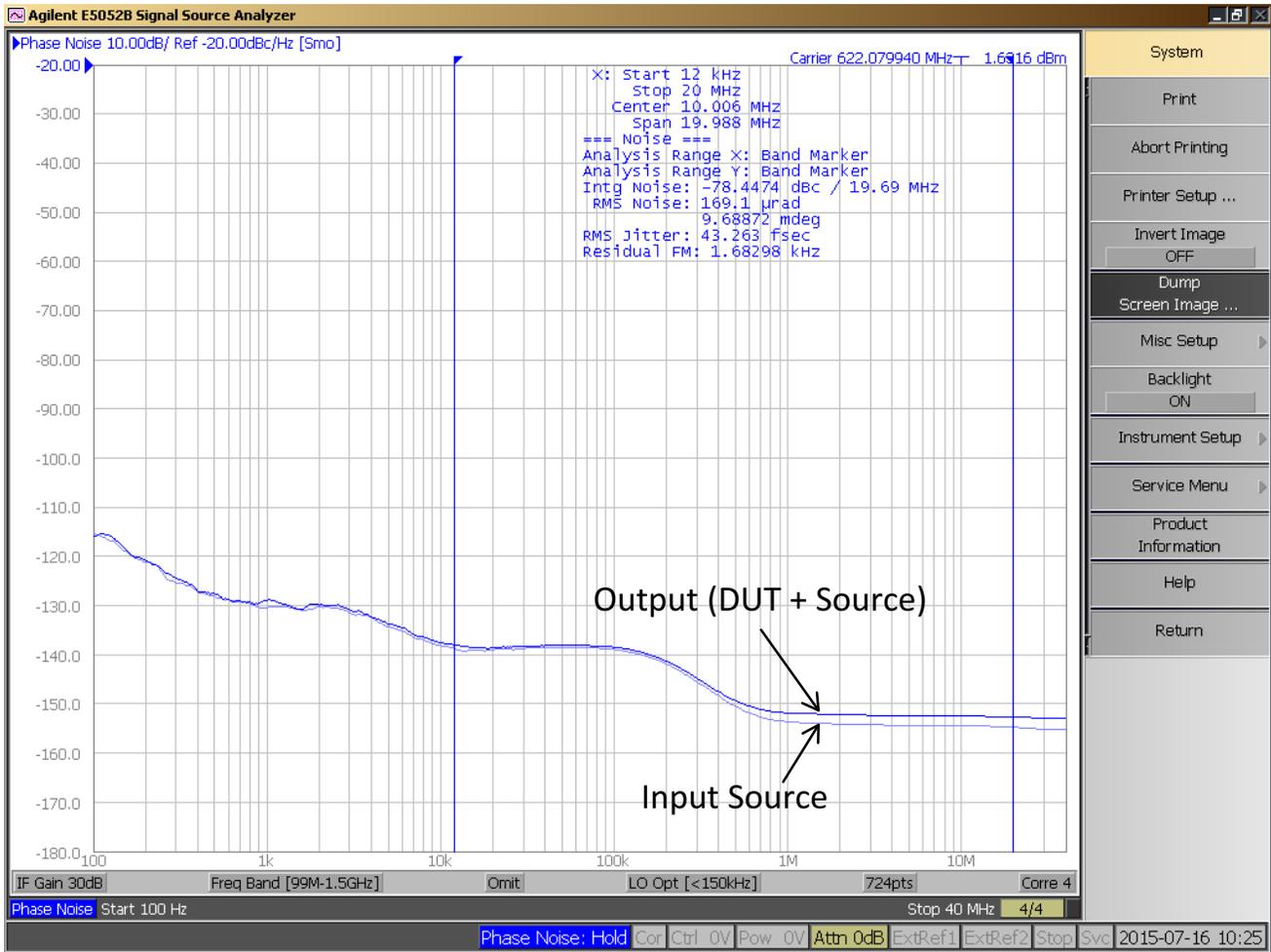


Figure 17. Typical NB7L14 Phase Noise Plot at $f_{\text{Carrier}} = 622.08 \text{ MHz}$, $V_{\text{CC}} = 3.3 \text{ V}$, 25°C

The above phase noise data was captured using Agilent E5052A/B. The data displays the input phase noise and output phase noise used to calculate the additive phase jitter at a specified integration range. The additive RMS phase jitter contributed by the device (integrated between 12 kHz and 20 MHz) is 24 fs. The additive RMS phase jitter performance of the translator is highly dependent on the phase noise of the input source.

To obtain the most precise additive phase noise measurement, it is vital that the source phase noise be

notably lower than that of the DUT. If the phase noise of the source is greater than the noise floor of the device under test, the source noise will dominate the additive phase jitter calculation and lead to an incorrect negative result for the additive phase noise within the integration range. The Figure above is a good example of the NB7L14 source generator phase noise having a significantly lower floor than the DUT and results in an additive phase jitter of 24 fs.

$$\text{Additive RMS phase jitter} = \sqrt{\text{RMS phase jitter of output}^2 - \text{RMS phase jitter of input}^2}$$

$$24 \text{ fs} = \sqrt{43.26 \text{ fs}^2 - 35.98 \text{ fs}^2}$$

To see the performance of NB7L14 beyond conditions outlined in this datasheet use our Phase Noise Explorer web tool located at ON Semiconductor [Green Point Design Tools](#)

homepage. This free application enables an interactive environment for advanced phase noise and jitter analysis of timing devices and clock tree designs.

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ORDERING INFORMATION

| Device | Package | Case | Shipping† |
|--------------|---------------------|-------|--------------------|
| NB7L14MNG | QFN-16 (Pb-Free) | 485G | 123 Units / Rail |
| NB7L14MNTXG | QFN-16 (Pb-Free) | 485G | 3000 / Tape & Reel |
| NB7L14MN1G | QFN-16 (Pb-Free) | 485AE | 123 Units / Rail |
| NB7L14MN1TXG | QFN-16 (Pb-Free) | 485AE | 3000 / Tape & Reel |
| NB7L14MN1TWG | QFN-16 (Pb-Free) | 485AE | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

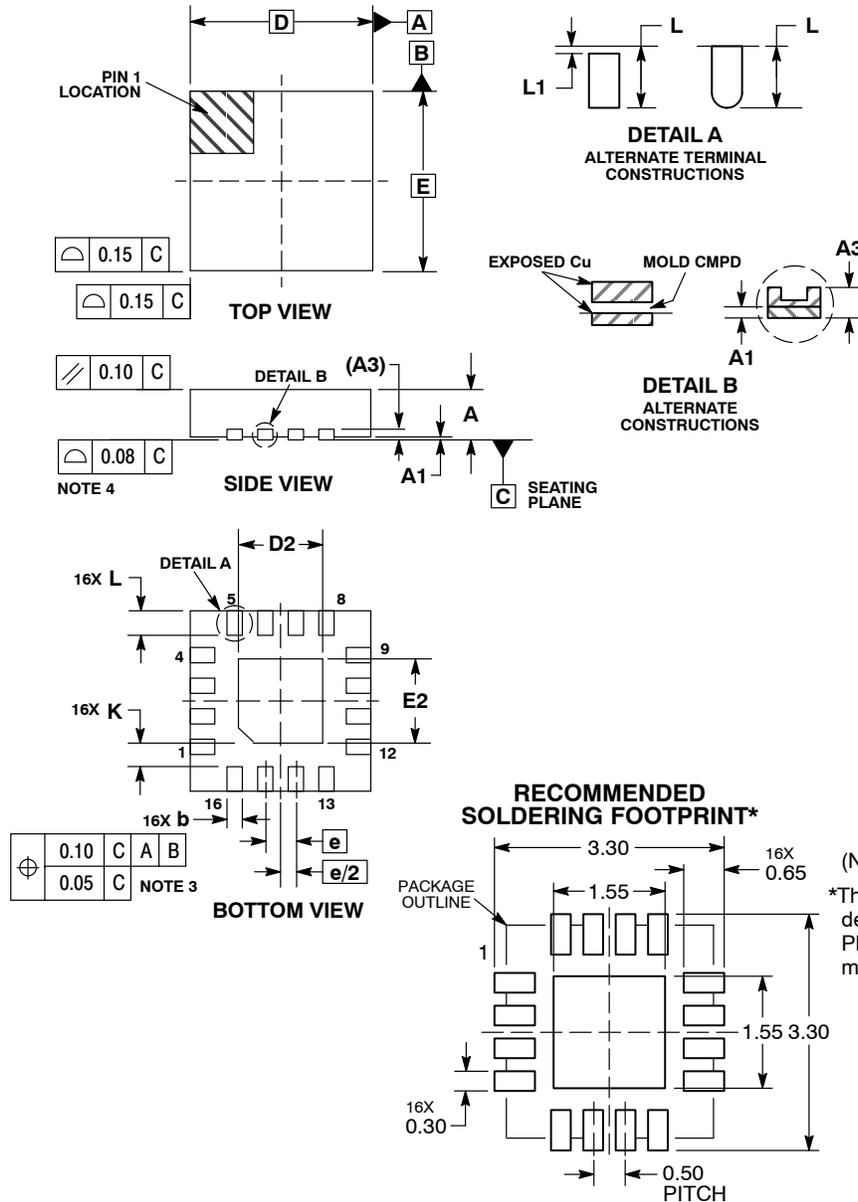
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1
SCALE 2:1

QFN16 3x3, 0.5P
CASE 485AE
ISSUE C

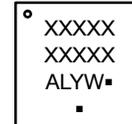
DATE 24 JUN 2016



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS.
 3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
 4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
 5. OUTLINE MEETS JEDEC DIMENSIONS PER MO-220, VARIATION VEED-6.

| DIM | MILLIMETERS | |
|-----|-------------|------|
| | MIN | MAX |
| A | 0.80 | 1.00 |
| A1 | 0.00 | 0.05 |
| A3 | 0.20 | REF |
| b | 0.18 | 0.30 |
| D | 3.00 | BSC |
| D2 | 1.25 | 1.55 |
| E | 3.00 | BSC |
| E2 | 1.25 | 1.55 |
| e | 0.50 | BSC |
| K | 0.20 | --- |
| L | 0.30 | 0.50 |
| L1 | 0.00 | 0.15 |

GENERIC MARKING DIAGRAM*



- A = Assembly Location
- L = Wafer Lot
- Y = Year
- W = Work Week
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present.

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

| | | |
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