

**Dual High-efficiency PWM Step-down DC-DC Converter with OVP**

**AUR9707**

### General Description

The AUR9707 is a high efficiency step-down DC-DC voltage converter. The chip operation is optimized using constant frequency, peak-current mode architecture with built-in synchronous power MOSFET switchers and internal compensators to reduce external part counts. It is automatically switching between the normal PWM mode and LDO mode to offer improved system power efficiency covering a wide range of loading conditions.

The oscillator and timing capacitors are all built-in providing an internal switching frequency of 1.5MHz that allows the use of small surface mount inductors and capacitors for portable product implementations. Additional features included Soft Start (SS), Under Voltage Lock Out (UVLO), Input Over Voltage Protection (IOVP) and Thermal Shutdown Detection (TSD) are integrated to provide reliable product applications.

The device is available in adjustable output voltage versions ranging from 1V to 3.3V, and is able to deliver up to 1A.

The AUR9707 is available in WDFN-3x3-12 package.

### Features

- Dual Channel High Efficiency Buck Power Converter
- Low Quiescent Current
- Output Current: 1A
- Adjustable Output Voltage from 1V to 3.3V
- Wide Operating Voltage Range: 2.5V to 5.5V
- Built-in Power Switches for Synchronous Rectification with High Efficiency
- Feedback Voltage: 600mV
- 1.5MHz Constant Frequency Operation
- Automatic PWM/LDO Mode Switching Control
- Thermal Shutdown Protection
- Low Drop-out Operation at 100% Duty Cycle
- No Schottky Diode Required
- Internal Input Over Voltage Protection

### Applications

- Mobile Phone, Digital Camera and MP3 Player
- Headset, Radio and Other Hand-held Instrument
- Post DC-DC Voltage Regulation
- PDA and Notebook Computer

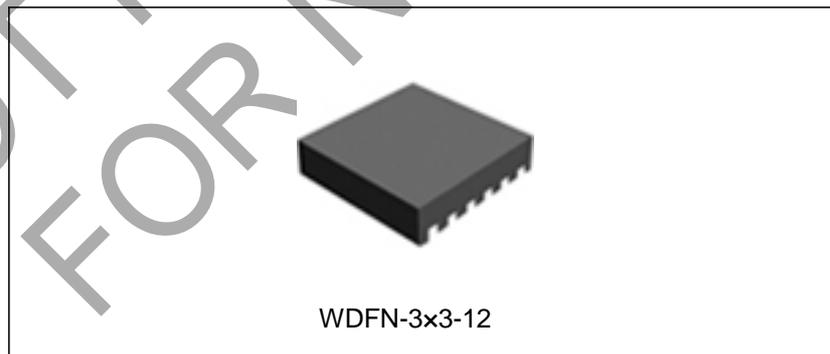


Figure 1. Package Type of AUR9707

## Pin Configuration

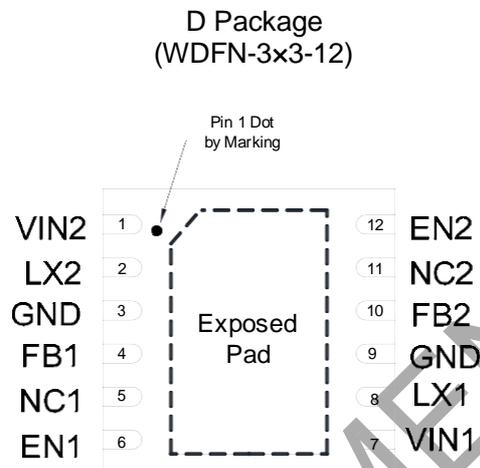


Figure 2. Pin Configuration of AUR9707 (Top View)

## Pin Description

Pin Number	Pin Name	Function
1	VIN2	Power supply input of channel 2
2	LX2	Connection from power MOSFET of channel 2 to inductor
3, 9	GND	This pin is the GND reference for the NMOSFET power stage. It must be connected to the system ground
4	FB1	Feedback voltage of channel 1
5, 11	NC1,NC2	No internal connection (floating or connecting to GND)
6	EN1	Enable signal input of channel 1, active high
7	VIN1	Power supply input of channel 1
8	LX1	Connection from power MOSFET of channel 1 to inductor
10	FB2	Feedback voltage of channel 2
12	EN2	Enable signal input of channel 2, active high

### Functional Block Diagram

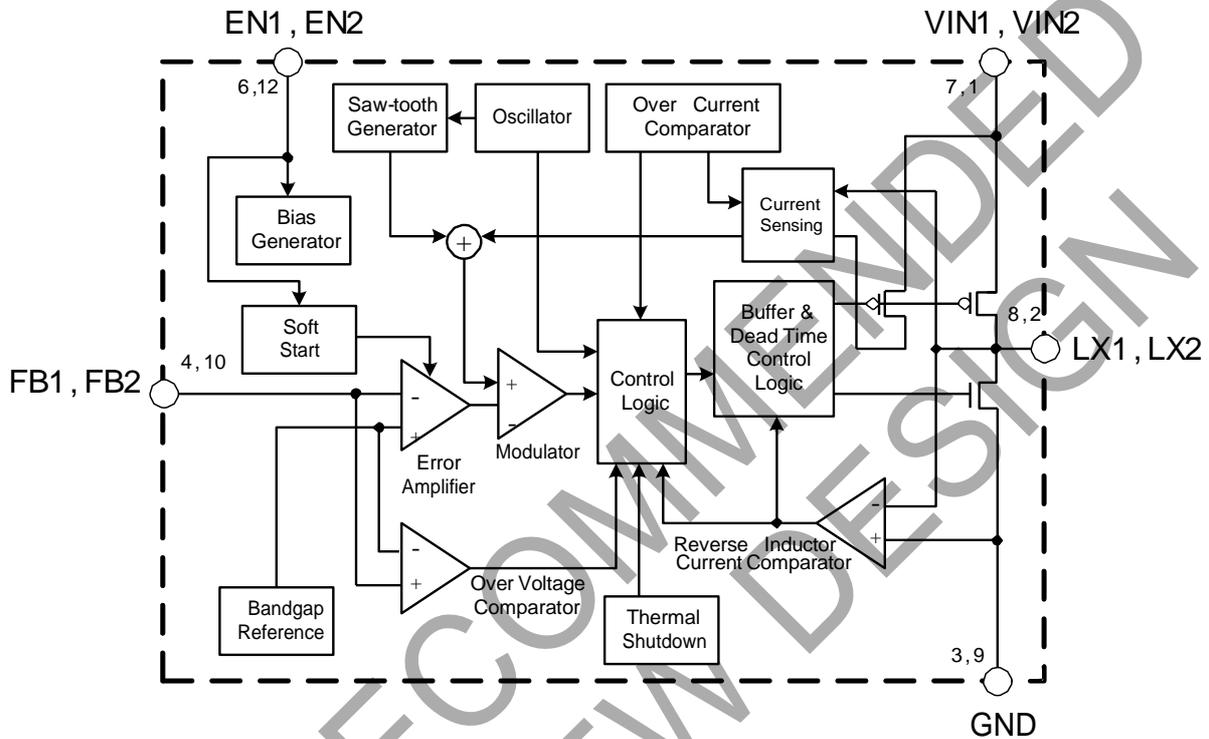
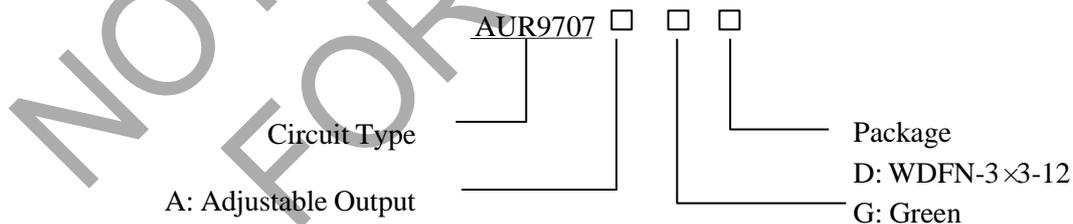


Figure 3. Functional Block Diagram of AUR9707

### Ordering Information



Package	Temperature Range	Part Number	Marking ID	Packing Type
WDFN-3x3-12	-40 to 80 °C	AUR9707AGD	9707A	Tape & Reel

BCD Semiconductor's Pb-free products, as designated with "G" in the part number, are RoHS compliant and green.

**Absolute Maximum Ratings (Note 1)**

Parameter	Symbol	Value	Unit
Supply Input Voltage	$V_{IN}$	0 to 6.5	V
Enable Input Voltage	$V_{EN}$	-0.3 to $V_{IN}+0.3$	V
Output Voltage	$V_{OUT}$	-0.3 to $V_{IN}+0.3$	V
$V_{IN1}-V_{IN2}$ Voltage (Note 2)	$V_{DF}$	-0.3 to 0.3	V
Power Dissipation (On PCB, $T_A=30\text{ }^\circ\text{C}$ )	$P_D$	2.31	W
Thermal Resistance (Junction to Ambient, Simulation)	$\theta_{JA}$	41	$^\circ\text{C/W}$
Thermal Resistance (Junction to Case, Simulation)	$\theta_{JC}$	4.2	$^\circ\text{C/W}$
Operating Junction Temperature	$T_J$	160	$^\circ\text{C}$
Operating Temperature	$T_O$	-40 to 85	$^\circ\text{C}$
Storage Temperature	$T_S$	-55 to 150	$^\circ\text{C}$
ESD (Human Body Model)	$V_{HBM}$	2000	V
ESD (Machine Model)	$V_{MM}$	200	V

Note 1: Stresses greater than those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to “Absolute Maximum Ratings” for extended periods may affect device reliability.

Note 2:  $|V_{IN1}-V_{IN2}|$  voltage difference can not exceed 0.3V, otherwise, the chip will be damaged.

**Recommended Operating Conditions**

Parameter	Symbol	Min	Max	Unit
Supply Input Voltage	$V_{IN}$	2.5	5.5	V
Junction Temperature Range	$T_J$	-20	125	$^\circ\text{C}$
Ambient Temperature Range	$T_A$	-40	80	$^\circ\text{C}$

**Dual High-efficiency PWM Step-down DC-DC Converter with OVP****AUR9707****Electrical Characteristics** $V_{IN}=3.6V$ ,  $V_{OUT}=2.5V$ ,  $V_{REF}=0.6V$ ,  $L=2.2\mu H$ ,  $C_{IN}=4.7\mu F$ ,  $C_{OUT}=10\mu F$ ,  $T_A=25^\circ C$ ,  $I_{MAX}=1A$ .

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input Voltage Range	$V_{IN}$		2.5		5.5	V
Shutdown Current	$I_{OFF}$	$V_{EN}=0$		0.1	1	$\mu A$
Regulated Feedback Voltage	$V_{FB}$	For Adjustable Output Voltage	0.585	0.6	0.615	V
Regulated Output Voltage Accuracy	$\Delta V_{OUT}/V_{OUT}$	$V_{IN}=2.5V$ to $5.5V$ ; $I_{OUT}=0$ to $1A$	-3		3	%
Peak Inductor Current	$I_{PK}$	$V_{IN}=3V$ , $V_{FB}=0.5V$		1.5		A
Oscillator Frequency	$f_{OSC}$	$V_{IN}=3.6V$	1.2	1.5	1.8	MHz
PMOSFET $R_{ON}$	$R_{ON(P)}$	$V_{IN}=3.6V$ , $I_{OUT}=200mA$		0.28		$\Omega$
NMOSFET $R_{ON}$	$R_{ON(N)}$	$V_{IN}=2.5V$ , $I_{OUT}=200mA$		0.38		$\Omega$
Input DC Bias Current	$I_S$	$V_{IN}=3.6V$ , $I_{OUT}=200mA$		0.25		$\mu A$
		$V_{IN}=2.5V$ , $I_{OUT}=200mA$		0.35		
LX Leakage Current	$I_{LX}$	$V_{IN}=5V$ , $V_{EN}=0V$ , $V_{LX}=0V$ or $5V$		0.01	0.1	$\mu A$
Feedback Current	$I_{FB}$				30	nA
Input Over Voltage Protection	$V_{LOVP}$			6		V
EN Leakage Current	$I_{EN}$			0.01	0.1	$\mu A$
EN High-level Input Voltage	$V_{EN\_H}$	$V_{IN}=2.5V$ to $5.5V$	1.5			V
EN Low-Level Input Voltage	$V_{EN\_L}$	$V_{IN}=2.5V$ to $5.5V$			0.6	V
Under Voltage Lock Out				1.8		V
Hysteresis				0.1		V
Thermal Shutdown	$T_{SD}$			150		$^\circ C$

Typical Performance Characteristics

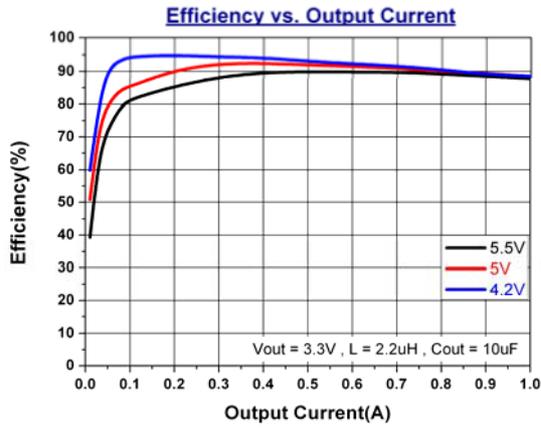


Figure 4. Efficiency vs. Output Current

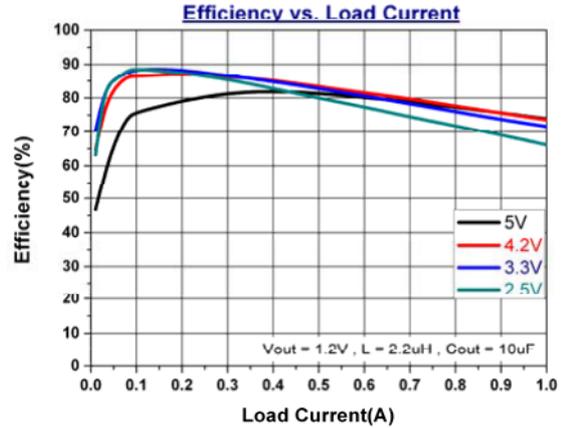


Figure 5. Efficiency vs. Load Current

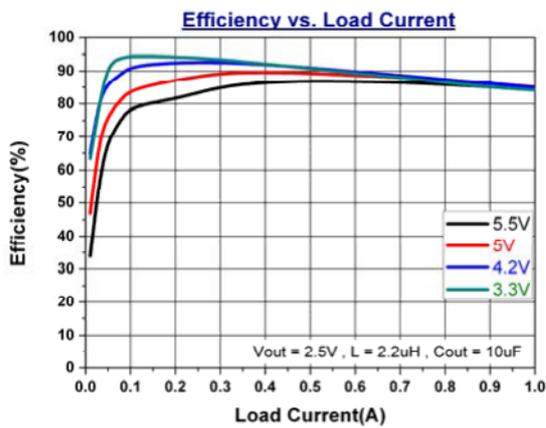


Figure 6. Efficiency vs. Load Current

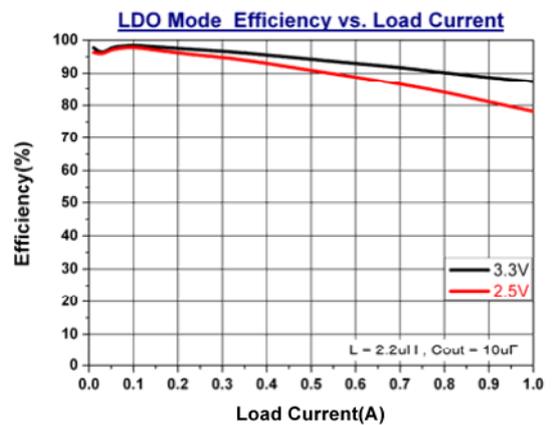


Figure 7. LDO Mode Efficiency vs. Load Current

Typical Performance Characteristics (Continued)

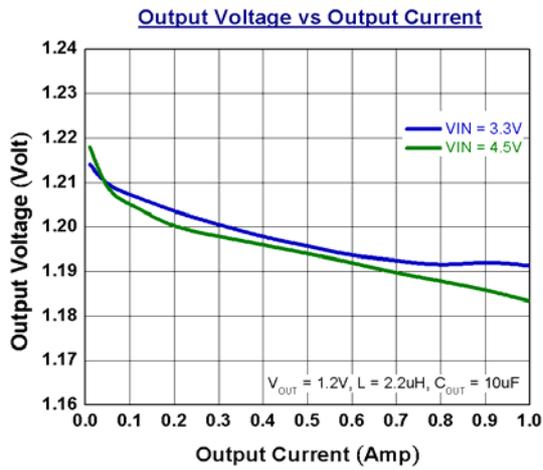


Figure 8. Output Voltage vs. Output Current

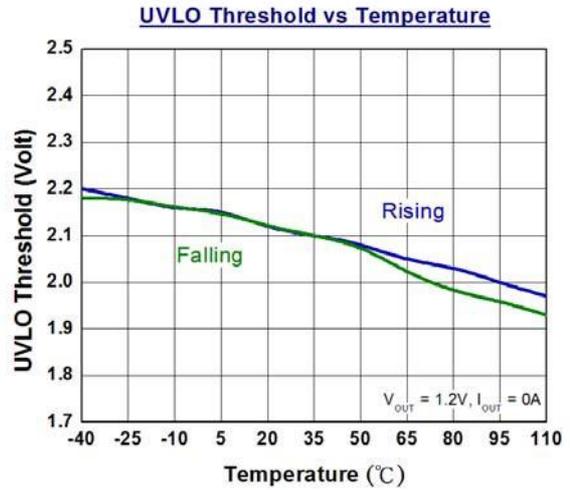


Figure 9. UVLO Threshold vs. Temperature

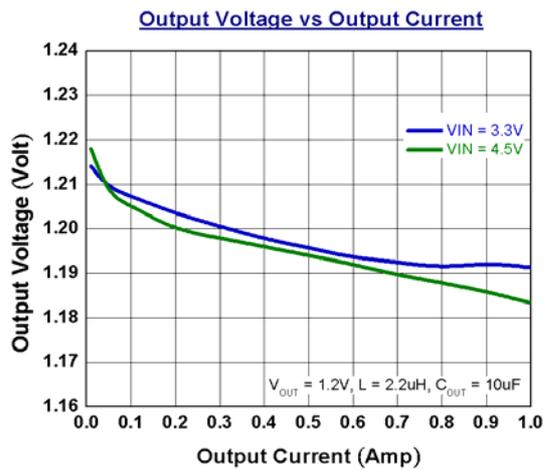


Figure 10. Output Voltage vs. Output Current

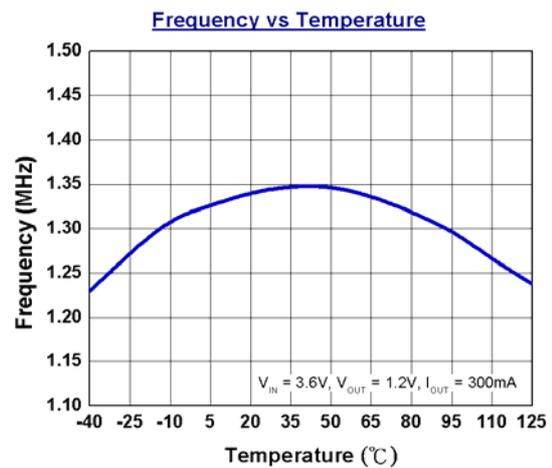


Figure 11. Frequency vs. Temperature

Typical Performance Characteristics (Continued)

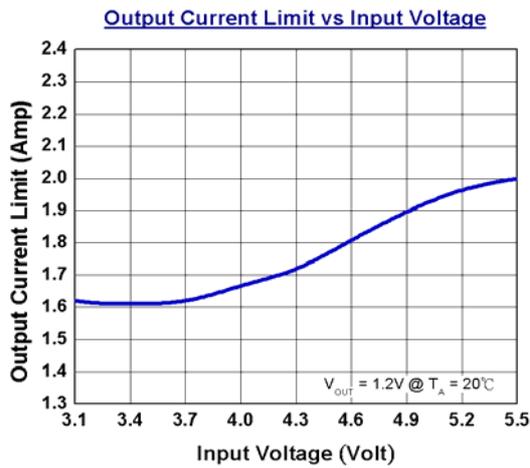


Figure 12. Output Current Limit vs. Input Voltage

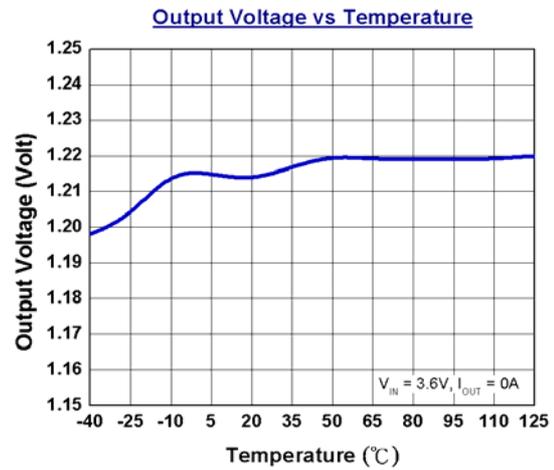


Figure 13. Output Voltage vs. Temperature

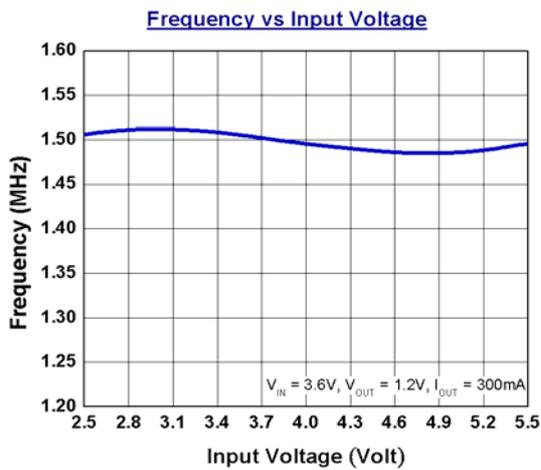


Figure 14. Frequency vs. Input Voltage

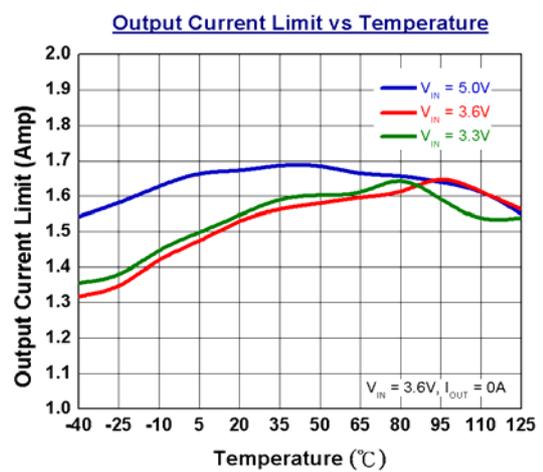


Figure 15. Output Current Limit vs. Temperature

Typical Performance Characteristics (Continued)

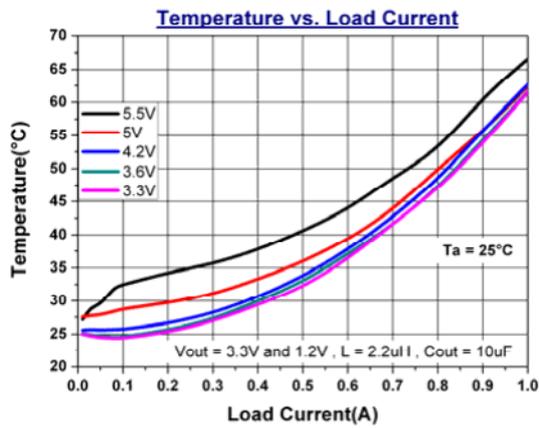


Figure 16. Temperature vs. Load Current

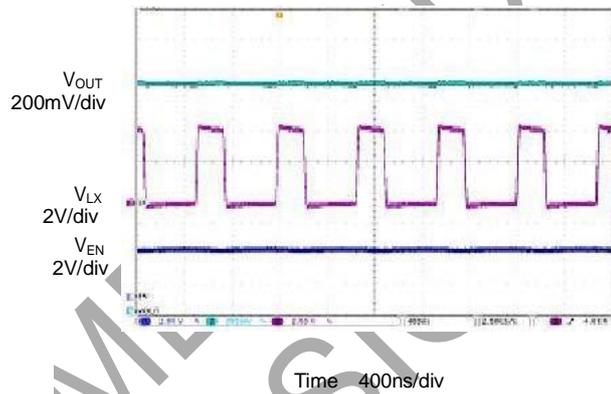


Figure 17. Waveform of  $V_{IN}=4.5V$ ,  $V_{OUT}=1.5V$ ,  $L=2.2\mu H$

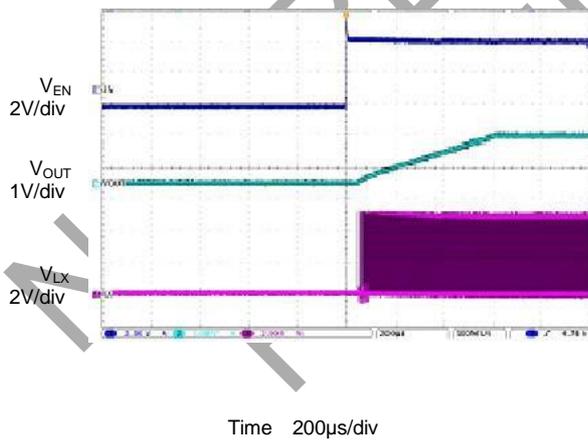


Figure 18. Soft Start

## Application Information

The basic AUR9707 application circuit is shown in Figure 23, external components selection is determined by the load current and is critical with the selection of inductor and capacitor values.

### 1. Inductor Selection

For most applications, the value of inductor is chosen based on the required ripple current with the range of 2.2μH to 4.7μH.

$$\Delta I_L = \frac{1}{f \times L} V_{OUT} \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

The largest ripple current occurs at the highest input voltage. Having a small ripple current reduces the ESR loss in the output capacitor and improves the efficiency. The highest efficiency is realized at low operating frequency with small ripple current. However, larger value inductors will be required. A reasonable starting point for ripple current setting is  $\Delta I_L = 40\% I_{MAX}$ . For a maximum ripple current stays below a specified value, the inductor should be chosen according to the following equation:

$$L = \left[ \frac{V_{OUT}}{f \times \Delta I_L (MAX)} \right] \left[ 1 - \frac{V_{OUT}}{V_{IN} (MAX)} \right]$$

The DC current rating of the inductor should be at least equal to the maximum output current plus half the highest ripple current to prevent inductor core saturation. For better efficiency, a lower DC-resistance inductor should be selected.

### 2. Capacitor Selection

The input capacitance,  $C_{IN}$ , is needed to filter the trapezoidal current at the source of the top MOSFET. To prevent large ripple voltage, a low ESR input capacitor sized for the maximum RMS current must be used. The maximum RMS capacitor current is given by:

$$I_{RMS} = I_{OMAX} \times \frac{[V_{OUT} (V_{IN} - V_{OUT})]^{\frac{1}{2}}}{V_{IN}}$$

It indicates a maximum value at  $V_{IN} = 2V_{OUT}$ , where  $I_{RMS} = I_{OUT}/2$ . This simple worst-case condition is commonly used for design because even significant

deviations do not much relieve. The selection of  $C_{OUT}$  is determined by the Effective Series Resistance (ESR) that is required to minimize output voltage ripple and load step transients, as well as the amount of bulk capacitor that is necessary to ensure that the control loop is stable. Loop stability can be also checked by viewing the load step transient response as described in the following section. The output ripple,  $\Delta V_{OUT}$ , is determined by:

$$\Delta V_{OUT} \leq \Delta I_L \left[ ESR + \frac{1}{8 \times f \times C_{OUT}} \right]$$

The output ripple is the highest at the maximum input voltage since  $\Delta I_L$  increases with input voltage.

### 3. Load Transient

A switching regulator typically takes several cycles to respond to the load current step. When a load step occurs,  $V_{OUT}$  immediately shifts by an amount equal to  $\Delta I_{LOAD} \times ESR$ , where ESR is the effective series resistance of output capacitor.  $\Delta I_{LOAD}$  also begins to charge or discharge  $C_{OUT}$  generating a feedback error signal used by the regulator to return  $V_{OUT}$  to its steady-state value. During the recovery time,  $V_{OUT}$  can be monitored for overshoot or ringing that would indicate a stability problem.

### 4. Output Voltage Setting

The output voltage of AUR9707 can be adjusted by a resistive divider according to the following formula:

$$V_{OUT} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right) = 0.6V \times \left(1 + \frac{R_1}{R_2}\right)$$

The resistive divider senses the fraction of the output voltage as shown in Figure 19.

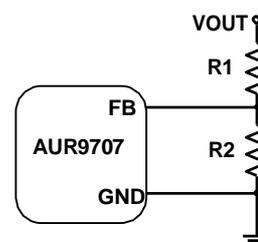


Figure 19. Setting the Output Voltage

## Application Information (Continued)

### 5. Efficiency Considerations

The efficiency of switching regulator is equal to the output power divided by the input power times 100%. It is usually useful to analyze the individual losses to determine what is limiting efficiency and which change could produce the largest improvement. Efficiency can be expressed as:

$$\text{Efficiency} = 100\% - L1 - L2 - \dots$$

Where L1, L2, etc. are the individual losses as a percentage of input power.

Although all dissipative elements in the regulator produce losses, two major sources usually account for most of the power losses:  $V_{IN}$  quiescent current and  $I^2R$  losses. The  $V_{IN}$  quiescent current loss dominates the efficiency loss at very light load currents and the  $I^2R$  loss dominates the efficiency loss at medium to heavy load currents.

**5.1** The  $V_{IN}$  quiescent current loss comprises two parts: the DC bias current as given in the electrical characteristics and the internal MOSFET switch gate charge currents. The gate charge current results from switching the gate capacitance of the internal power MOSFET switches. Each cycle the gate is switched from high to low, then to high again, and the packet of charge,  $dQ$  moves from  $V_{IN}$  to ground. The resulting  $dQ/dt$  is the current out of  $V_{IN}$  that is typically larger than the internal DC bias current. In continuous mode,

$$I_{GATE} = f \times (Q_P + Q_N)$$

Where  $Q_P$  and  $Q_N$  are the gate charge of power PMOSFET and NMOSFET switches. Both the DC bias current and gate charge losses are proportional to the  $V_{IN}$  and this effect will be more serious at higher input voltages.

**5.2**  $I^2R$  losses are calculated from internal switch resistance,  $R_{SW}$  and external inductor resistance  $R_L$ . In continuous mode, the average output current flowing through the inductor is chopped between power PMOSFET switch and NMOSFET switch. Then, the series resistance looking into the LX pin is a function of both PMOSFET  $R_{DS(ON)}$  and NMOSFET

$R_{DS(ON)}$  resistance and the duty cycle (D):

$$R_{SW} = R_{DS(ON)P} \times D + R_{DS(ON)N} \times (1 - D)$$

Therefore, to obtain the  $I^2R$  losses, simply add  $R_{SW}$  to  $R_L$  and multiply the result by the square of the average output current.

Other losses including  $C_{IN}$  and  $C_{OUT}$  ESR dissipative losses and inductor core losses generally account for less than 2 % of total additional loss.

### 6. Thermal Characteristics

In most applications, the part does not dissipate much heat due to its high efficiency. However, in some conditions when the part is operating in high ambient temperature with high  $R_{DS(ON)}$  resistance and high duty cycles, such as in LDO mode, the heat dissipated may exceed the maximum junction temperature. To avoid the part from exceeding maximum junction temperature, the user should do some thermal analysis. The maximum power dissipation depends on the layout of PCB, the thermal resistance of IC package, the rate of surrounding airflow and the temperature difference between junction and ambient.

### 7. PCB Layout Considerations

When laying out the printed circuit board, the following checklist should be used to optimize the performance of AUR9707.

- 1) The power traces, including the GND trace, the LX trace and the VIN trace should be kept direct, short and wide.
- 2) Put the input capacitor as close as possible to the VIN and GND pins.
- 3) The FB pin should be connected directly to the feedback resistor divider.
- 4) Keep the switching node, LX, away from the sensitive FB pin and the node should be kept small area.
- 5) The following is an example of 2-layer PCB layout as shown in Figure 21 and Figure 22 for reference.

Application Information (Continued)

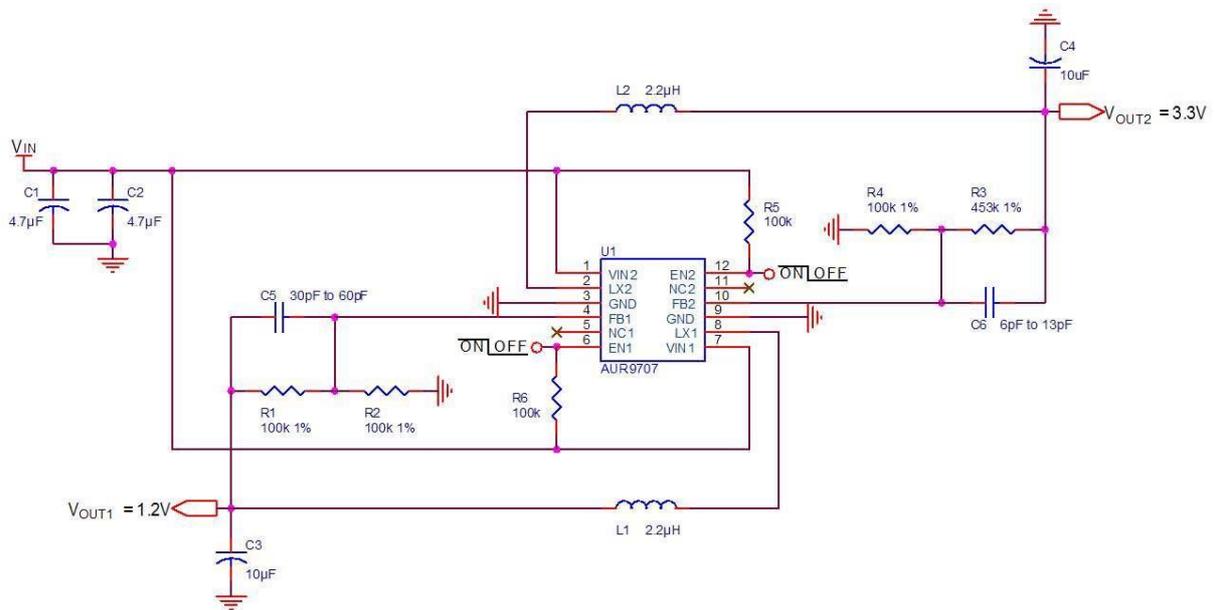


Figure 20. The Evaluation Board Schematic

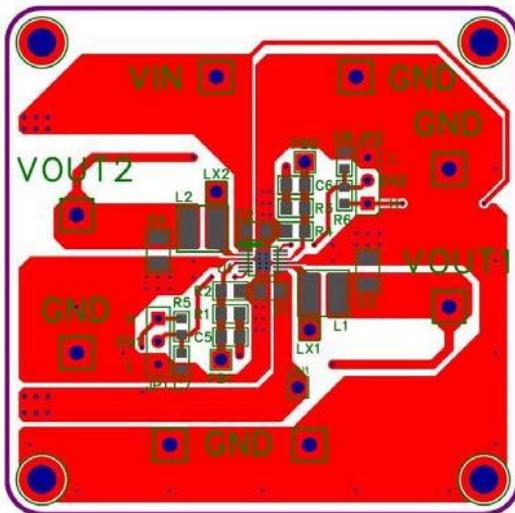


Figure 21. Top Layer Layout

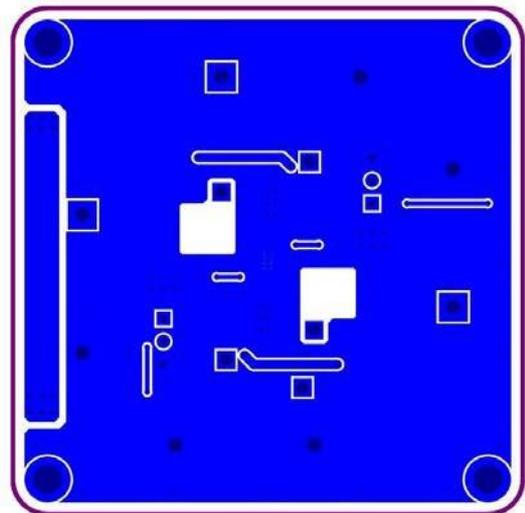
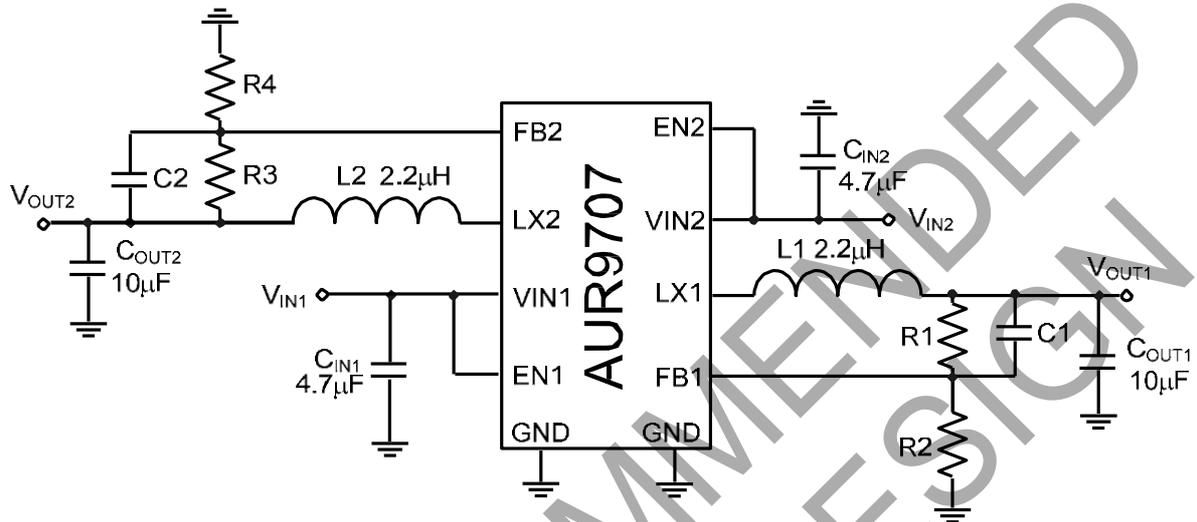


Figure 22. Bottom Layer Layout

## Typical Application



Note 3:  $V_{OUT1} = V_{REF} \times \left(1 + \frac{R_1}{R_2}\right)$  ;  $V_{OUT2} = V_{REF} \times \left(1 + \frac{R_3}{R_4}\right)$

When R2 or R4=300kΩ to 60 kΩ, the I<sub>R2</sub> or I<sub>R3</sub>=2µA to 10µA, and R1×C1 or R3×C2 should be in the range between 3×10<sup>-6</sup> and 6×10<sup>-6</sup> for component selection.

Figure 23. Typical Application Circuit of AUR9707

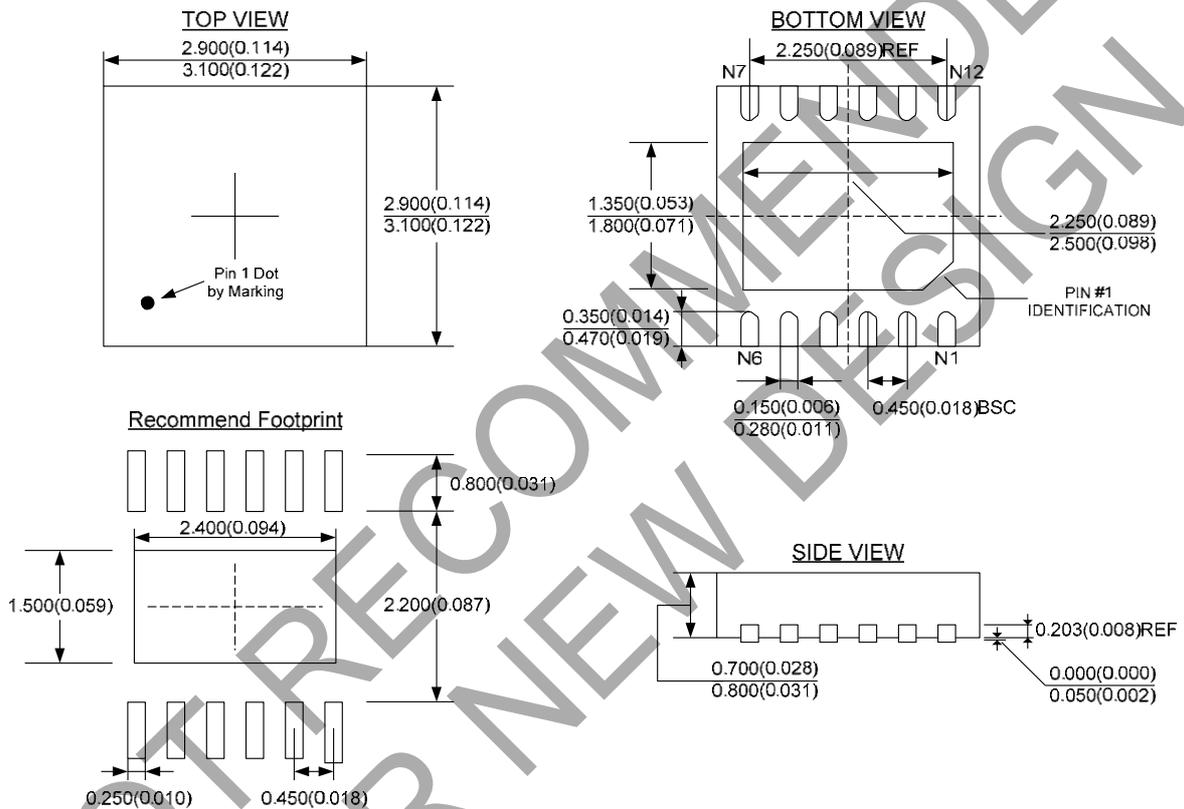
V <sub>OUT1</sub> or V <sub>OUT2</sub> (V)	R1 or R3(kΩ)	R2 or R4(kΩ)	C1 or C2(pF)	L1 or L2(µH)
3.3	240	53	20	2.2
2.5	240	75	20	2.2
1.8	240	120	20	2.2
1.5	240	160	20	2.2
1.2	240	240	20	2.2
1.0	240	300	20	2.2

Table 1. Component Guide

Mechanical Dimensions

WDFN-3x3-12

Unit: mm(inch)



**NOT RECOMMENDED FOR NEW DESIGN**  
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**BCD Semiconductor Manufacturing Limited**

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#### **MAIN SITE**

- Headquarters

**BCD Semiconductor Manufacturing Limited**

No. 1600, Zi Xing Road, Shanghai Zizhu Science-based Industrial Park, 200241, China  
Tel: +86-21-24162266, Fax: +86-21-24162277

- Wafer Fab

**Shanghai SIM-BCD Semiconductor Manufacturing Co., Ltd.**

800 Yi Shan Road, Shanghai 200233, China Tel:  
+86-21-6485 1491, Fax: +86-21-5450 0008

#### **REGIONAL SALES OFFICE**

**Shenzhen Office**

**Shanghai SIM-BCD Semiconductor Manufacturing Co., Ltd., Shenzhen Office**

Unit A Room 1203, Skyworth Bldg., Gaoxin Ave. I.S., Nanshan District, Shenzhen,  
China

Tel: +86-755-8826 7951  
Fax: +86-755-8826 7865

**Taiwan Office**

**BCD Semiconductor (Taiwan) Company Limited**

4F, 298-1, Rui Guang Road, Nei-Hu District, Taipei,  
Taiwan

Tel: +886-2-2656 2808  
Fax: +886-2-2656 2806

**USA Office**

**BCD Semiconductor Corp.**

30920 Huntwood Ave. Hayward,  
CA 94544, USA

Tel: +1-510-324-2988  
Fax: +1-510-324-2788