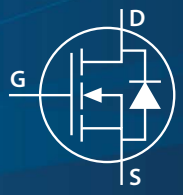
EPC2059 – Enhancement Mode Power Transistor

V_{DS}, 170 V
$R_{DS(on)}$, 9 mΩ
I_D, 24 A



EFFICIENT POWER CONVERSION

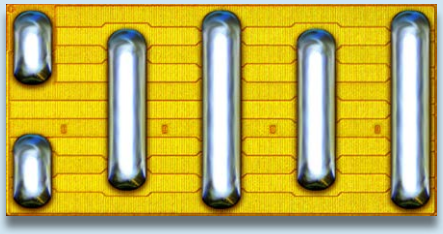
RoHS Halogen-Free

Gallium Nitride's exceptionally high electron mobility and low temperature coefficient allows very low $R_{DS(on)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and zero Q_{RR}. The end result is a device that can handle tasks where very high switching frequency, and low on-time are beneficial as well as those where on-state losses dominate.

Maximum Ratings			
PARAMETER		VALUE	UNIT
V_{DS}	Drain-to-Source Voltage (Continuous)	170	V
I_D	Continuous (T_A = 25°C)	24	A
	Pulsed (25°C, T_{PULSE} = 300 µs)	102	
V_{GS}	Gate-to-Source Voltage	6	V
	Gate-to-Source Voltage	-4	
T_J	Operating Temperature	-40 to 150	°C
T_{STG}	Storage Temperature	-40 to 150	

Thermal Characteristics			
PARAMETER		TYP	UNIT
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	0.9	°C/W
$R_{\theta JB}$	Thermal Resistance, Junction-to-Board	3	
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient (Note 1)	63	

Note 1: $R_{\theta JA}$ is determined with the device mounted on one square inch of copper pad, single layer 2 oz copper on FR4 board.
See https://epc-co.com/epc/documents/product-training/Appnote_Thermal_Performance_of_eGaN_FETs.pdf for details.



EPC2059 eGaN® FETs are supplied only in passivated die form with solder bars.
Die Size: 2.8 mm x 1.4 mm

Applications

- DC-DC Converters
- Sync rectification for AC/DC & DC-DC
- USB-C PD Quick Chargers & Adaptors
- BLDC Motor Drives
- Lidar
- Class-D Audio

Benefits

- Ultra High Efficiency
- No Reverse Recovery
- Ultra Low Q_G
- Small Footprint

Static Characteristics (T_J = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BV_{DSS}	Drain-to-Source Voltage	V_{GS} = 0 V, I_D = 0.15 mA	170			V
I_{DSS}	Drain-Source Leakage	V_{GS} = 0 V, V_{DS} = 136 V		0.03	0.1	mA
I_{GSS}	Gate-to-Source Forward Leakage	V_{GS} = 5 V		0.01	2.4	
	Gate-to-Source Forward Leakage#	V_{GS} = 5 V, T_J = 125°C		0.13	5.5	
	Gate-to-Source Reverse Leakage	V_{GS} = -4 V		0.03	0.2	
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 3 mA	0.7	1	2.5	V
$R_{DS(on)}$	Drain-Source On Resistance	V_{GS} = 5 V, I_D = 10 A		6.8	9	mΩ
V_{SD}	Source-Drain Forward Voltage	I_S = 0.5 A, V_{GS} = 0 V		1.6		V

Defined by design. Not subject to production test.

Dynamic Characteristics (T_J = 25°C unless otherwise stated)						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
C_{ISS}	Input Capacitance#	V_{DS} = 85 V, V_{GS} = 0 V		633	836	pF
C_{RSS}	Reverse Transfer Capacitance			1.6		
C_{OSS}	Output Capacitance#			267	401	
$C_{OSS(ER)}$	Effective Output Capacitance, Energy Related (Note 2)	V_{DS} = 0 to 85 V, V_{GS} = 0 V		332		
$C_{OSS(TR)}$	Effective Output Capacitance, Time Related (Note 3)			414		
R_G	Gate Resistance			0.5		Ω
Q_G	Total Gate Charge#	V_{DS} = 85 V, V_{GS} = 5 V, I_D = 10 A		5.7	7.4	nC
Q_{GS}	Gate-to-Source Charge	V_{DS} = 85 V, I_D = 10 A		1.3		
Q_{GD}	Gate-to-Drain Charge			0.9		
$Q_{G(TH)}$	Gate Charge at Threshold			1.0		
Q_{OSS}	Output Charge#	V_{DS} = 85 V, V_{GS} = 0 V		35	53	
Q_{RR}	Source-Drain Recovery Charge			0		

Defined by design. Not subject to production test.
Note 2: $C_{OSS(ER)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.
Note 3: $C_{OSS(TR)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 50% BV_{DSS}.

Figure 1: Typical Output Characteristics at 25°C

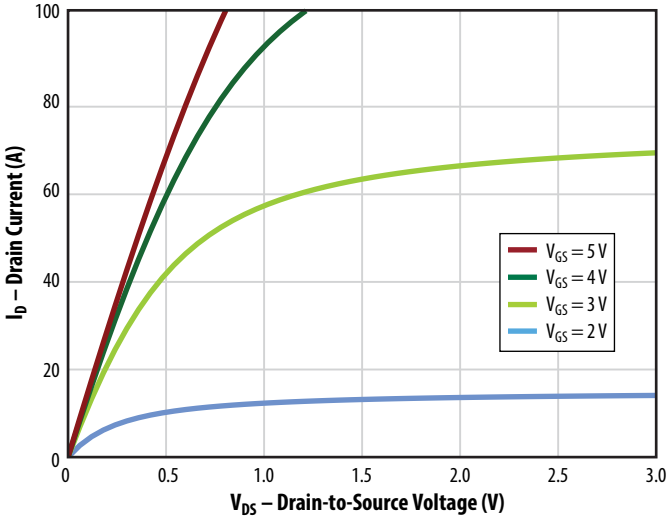


Figure 2: Transfer Characteristics

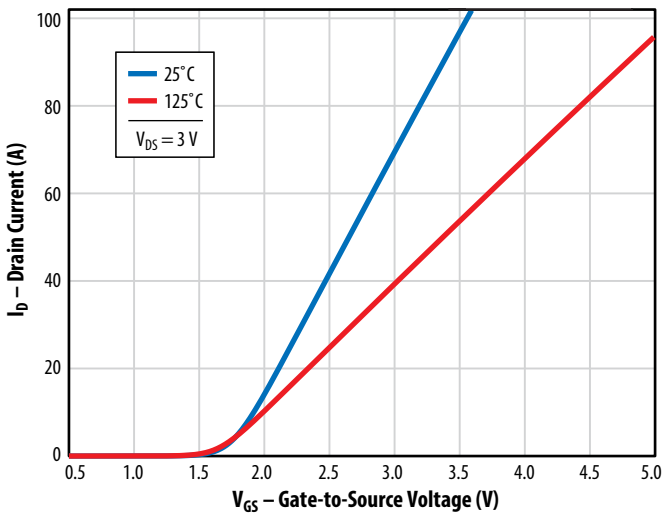


Figure 3: $R_{DS(on)}$ vs. V_{GS} for Various Drain Currents

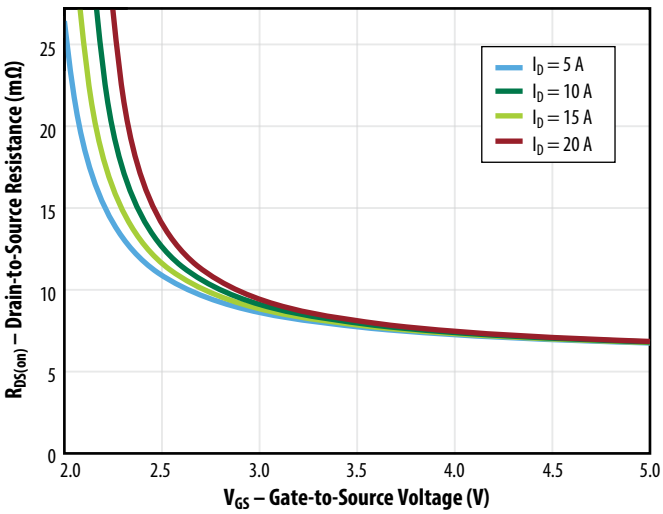


Figure 4: $R_{DS(on)}$ vs. V_{GS} for Various Temperatures

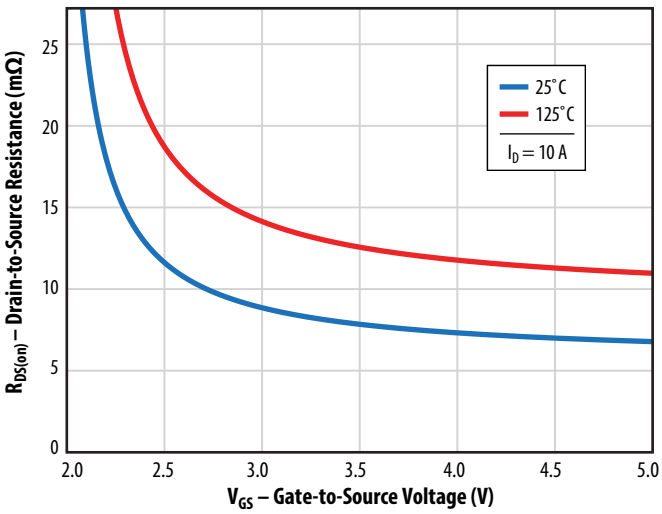


Figure 5a: Capacitance (Linear Scale)

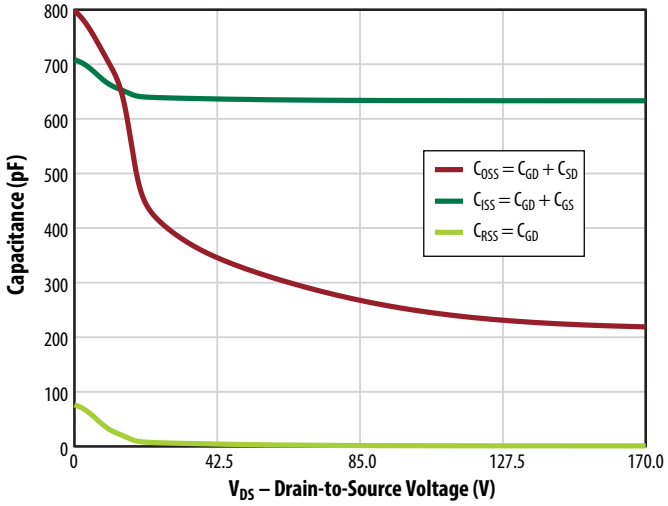


Figure 5b: Capacitance (Log Scale)

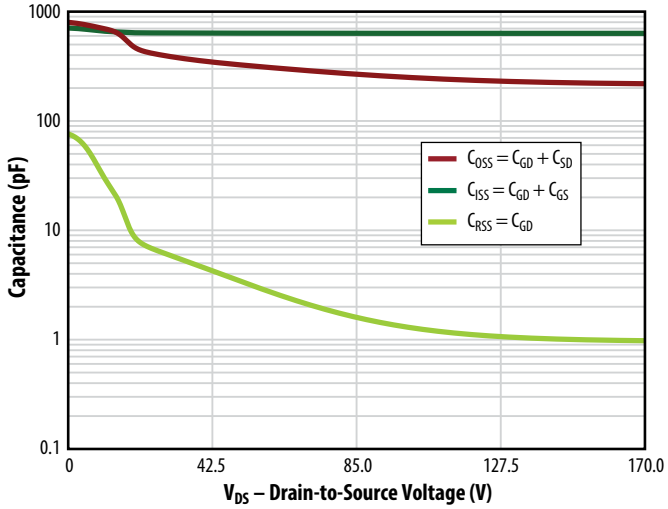


Figure 6: Output Charge and C_{OSS} Stored Energy

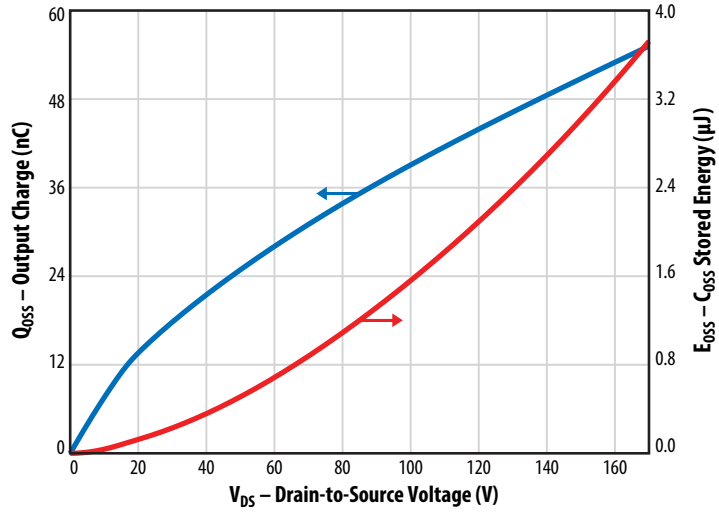


Figure 7: Gate Charge

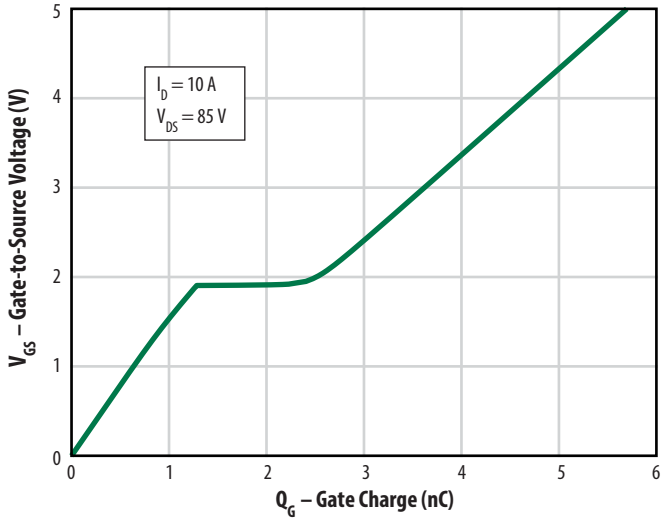


Figure 8: Reverse Drain-Source Characteristics

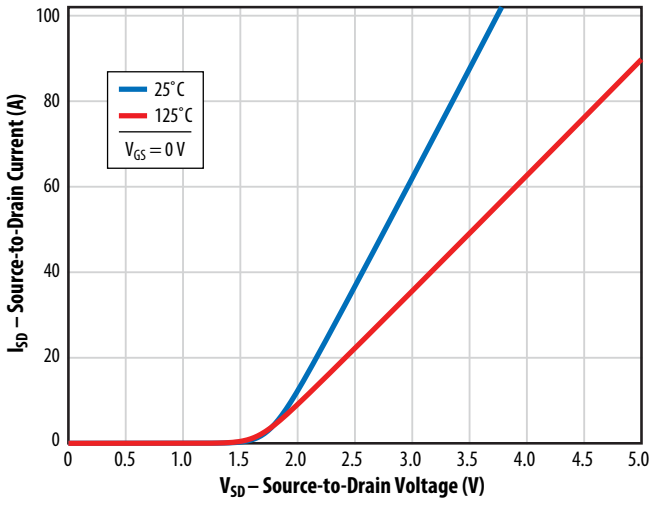


Figure 9: Normalized On-State Resistance vs. Temperature

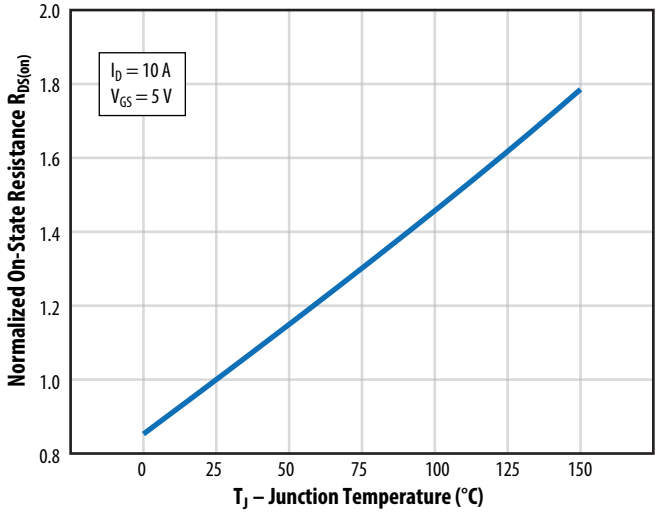


Figure 10: Normalized Threshold Voltage vs. Temperature

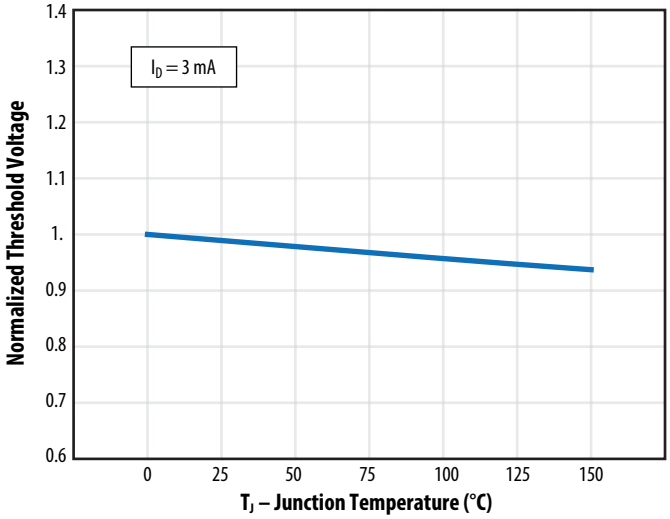
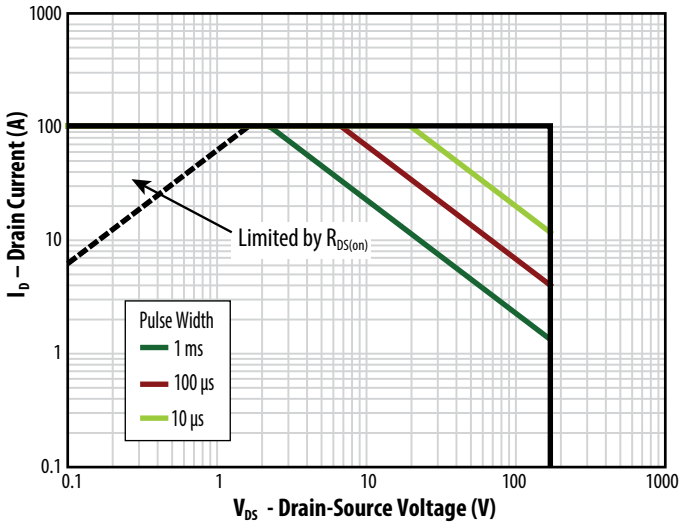
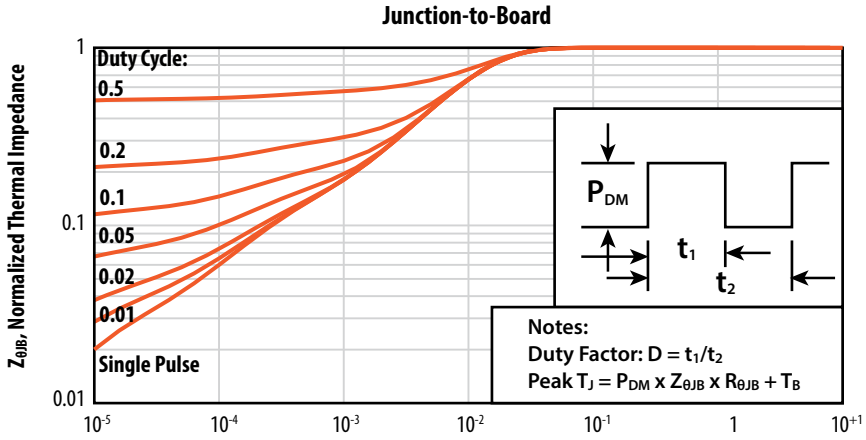


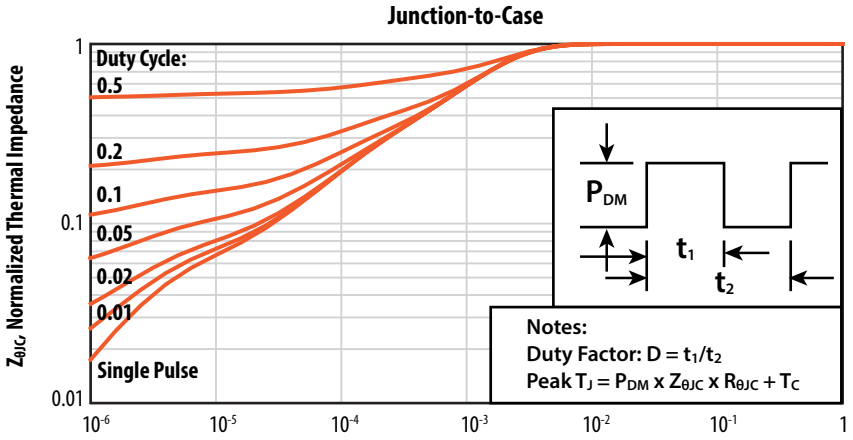
Figure 11: Safe Operating Area



T_J = Max Rated, T_C = +25°C, Single Pulse

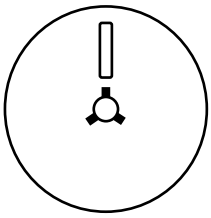
Figure 12: Transient Thermal Response Curves

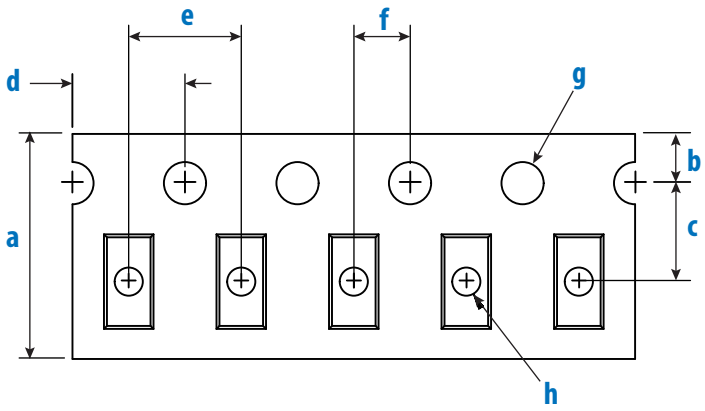


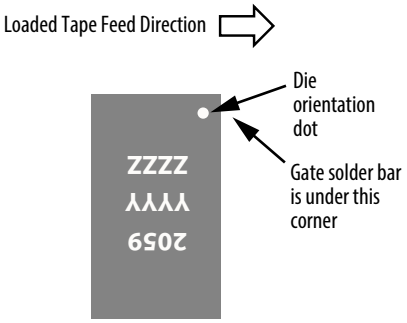


TAPE AND REEL CONFIGURATION

4 mm pitch, 8 mm wide tape on 7" reel







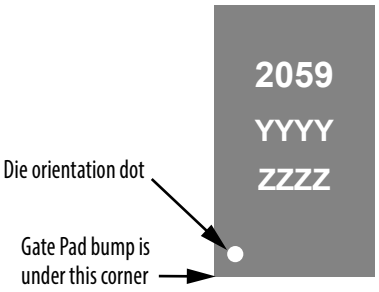
Die is placed into pocket solder bump side down (face side down)

	Dimension (mm)		
EPC2059 (Note 1)	Target	MIN	MAX
a	8.00	7.90	8.30
b	1.75	1.65	1.85
c (Note 2)	3.50	3.45	3.55
d	4.00	3.90	4.10
e	4.00	3.90	4.10
f (Note 2)	2.00	1.95	2.05
g	1.50	1.50	1.60
h	1.00	0.95	1.05

Note 1: MSL 1 (moisture sensitivity level 1) classified according to IPC/JEDEC industry standard.

Note 2: Pocket position is relative to the sprocket hole measured as true position of the pocket, not the pocket hole.

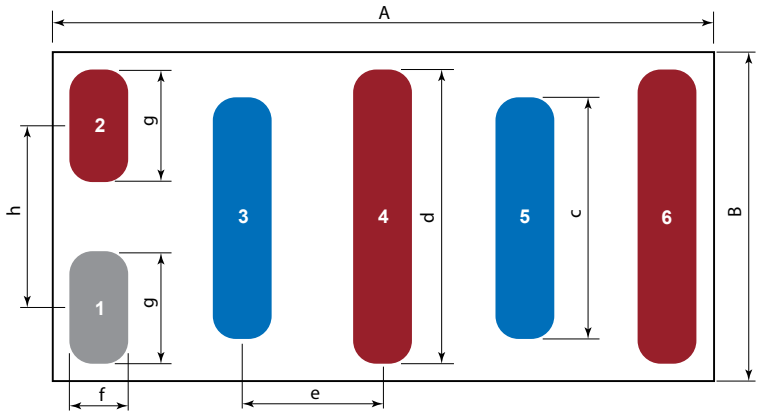
DIE MARKINGS



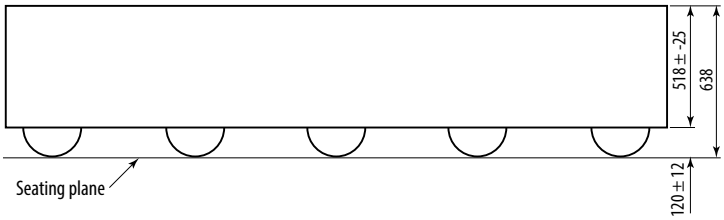
Part Number	Laser Markings		
	Part # Marking Line 1	Lot_Date Code Marking Line 2	Lot_Date Code Marking Line 3
EPC2059	2059	YYYY	ZZZZ

DIE OUTLINE

Solder Bump View



Side View



DIM	Micrometers		
	MIN	Nominal	MAX
A	2770	2800	2830
B	1370	1400	1430
c		1010	
d		1250	
e		600	
f		250	
g		475	
h		775	

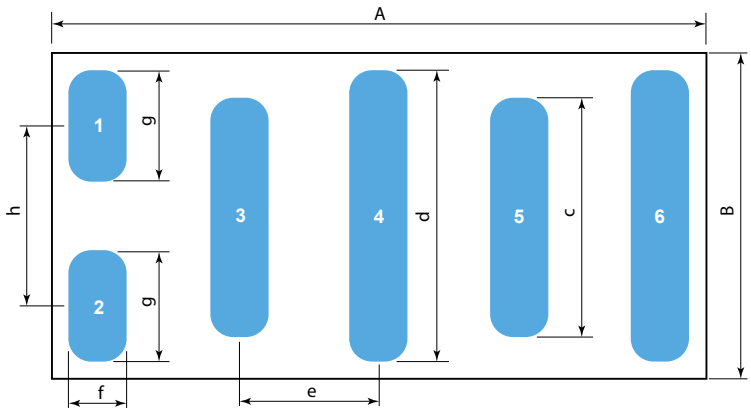
Pad 1 is Gate;

Pads 2 ,4, 6 are Source;

Pads 3, 5 are Drain

RECOMMENDED LAND PATTERN

(units in µm)



Land pattern is solder mask defined.

Solder mask is same as bump.

It is recommended to have on-Cu trace PCB vias,

Pad 1 is Gate;

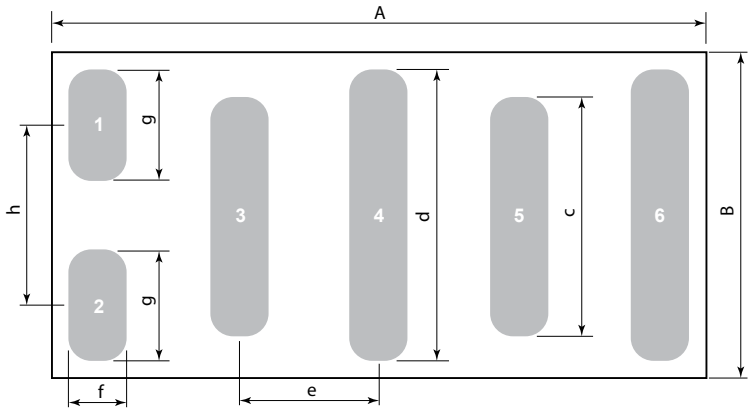
Pads 2 ,4, 6 are Source;

Pads 3, 5 are Drain

DIM	Nominal
A	2800
B	1400
c	1010
d	1250
e	600
f	250
g	475
h	775

RECOMMENDED STENCIL DRAWING

(units in µm)



DIM	Nominal
A	2800
B	1400
c	1010
d	1250
e	600
f	250
g	475
h	775

Recommended stencil should be 4 mil (100 µm) thick, must be laser cut, openings per drawing.

The corner has a radius of R60.

Intended for use with SAC305 Type 3 solder, reference 88.5% metals content.

Split stencil design can be provided upon request, but EPC has tested this stencil design and not found any scooping issues.

Additional assembly resources available at https://epc-co.com/epc/DesignSupport/AssemblyBasics.aspx