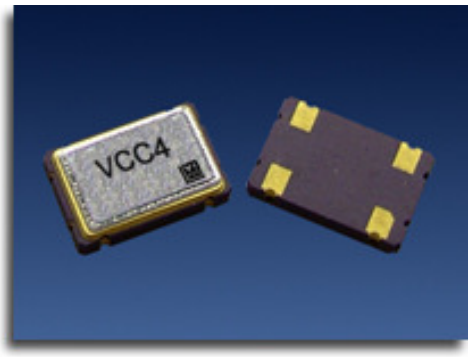
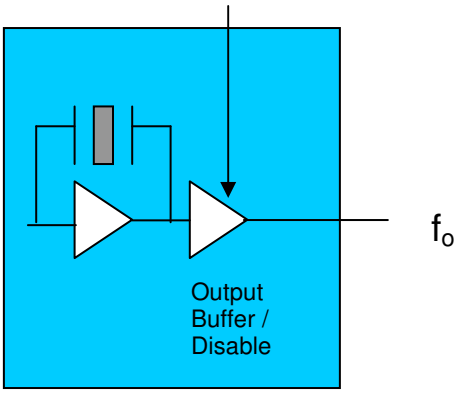
VCC4 series
1.8, 2.5, 3.3, 5.0 volt CMOS Oscillator



The VCC4 Crystal Oscillator



Features

- CMOS output
- Output frequencies to 125 MHz
- Low jitter, Fundamental or 3rd OT Crystal
- Tristate output for board test and debug
- -10/70 or –40/85°C operating temperature
- Gold over nickel contact pads
- Hermetically sealed ceramic SMD package
- Product is compliant to RoHS directive and fully compatible with lead free assembly

Applications

- SONET/SDH/DWDM
- Ethernet, Gigabit Ethernet
- Storage Area Network
- Digital Video
- Broadband Access
- Microprocessors/DSP/FPGA

Description

Vectron's VCC4 Crystal Oscillator (XO) is quartz stabilized square wave generator with a CMOS output, operating off a 1.8, 2.5, 3.3 or 5.0 volt supply.

The VCC4 uses fundamental or 3rd overtone crystals for output frequencies > 50MHz resulting in low jitter performance. VCC4 is hermetically sealed and also uses a monolithic IC, which improves reliability and reduces cost.

Performance Characteristics

Table 1. Electrical Performance, 5V option

Parameter	Symbol	Min	Typical	Maximum	Units
Frequency	f_O	1.544		75.000	MHz
Operating Supply Voltage [1]	V_{DD}	4.5		5.5	V
Absolute Maximum Supply Voltage		-0.7		7.0	V
Supply Current, Output Enabled	I_{DD}				mA
< 1.50 MHz				7	
1.500 to 20 MHz				10	
20.01 to 50 MHz				30	
50.01 to 75 MHz				40	
Supply Current, Out disabled	I_{DD}			30	uA
Output Logic Levels					
Output Logic High [2]	V_{OH}	0.9*V_{DD}			V
Output Logic Low [2]	V_{OL}			0.1*V_{DD}	V
Output Logic High Drive	I_{OH}	16			mA
Output Logic Low Drive	I_{OL}	16			mA
Output Rise/Fall Time [2]	t_R/t_F				ns
< 20.00 MHz				8	
20.01 to 50.00 MHz				5	
50.01 to 75.00 MHz				2	
Duty Cycle [3] *(ordering option)*	SYM		45/55		%
Operating temperature (*ordering option*)			-10/70 or -40/85		°C
Stability [4] (*ordering option)*			±25, ±50, ±100		ppm
RMS Jitter, 12kHz to 20 MHz			0.5	1	ps
Period Jitter					ps
RMS			3.0		
Peak to Peak			21		
Output Enable/Disable [5]					V
Output Enabled		4.0			
Output Disabled				0.8	
Internal Enable Pull-Up resistor [5]			100		Kohm
Start-up time				8	ms

1. Recommend a 0.01uF and a 0.1uF capacitor between power supply and ground (close to supply).
2. Parameter is defined in Figure 1 and tested as shown in Figure 2.
3. Symmetry is defined as On Time/Period (Figure 1).
4. Includes calibration tolerance, operating temperature, supply voltage variations, and shock and vibration (not under operation). Aging is included for ±50 and ±100ppm options.
5. Output will be enabled if enable/disable is left open.

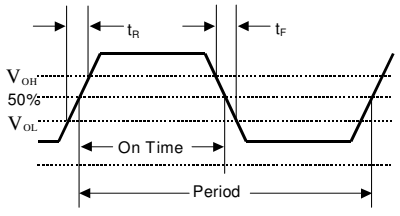


Figure 1: Output Waveform

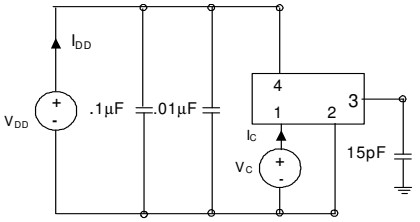


Figure 2: Typical Output Test Conditions (25±5°C)

Table 2. Electrical Performance, 3.3V option					
Parameter	**Symbol**	**Min**	**Typical**	**Maximum**	**Units**
Frequency	f_O	1.544		125.000	MHz
Operating Supply Voltage [1]	V_{DD}	2.97	3.3	3.63	V
Absolute Maximum Operating Voltage		-0.5		5.0	V
Supply Current, Output Enabled	I_{DD}				mA
< 1.500 MHz				5	
1.5 to 20 MHz				7	
20.01 to 50 MHz				20	
50.01 to 75 MHz				30	
75.01 to 100 MHz				40	
100.01 to 125 MHz				46	
Supply Current, Output disabled	I_{DD}			30	uA
Output Logic Levels					
Output Logic High [2]	V_{OH}	0.9*V_{DD}			V
Output Logic Low [2]	V_{OL}			0.1*V_{DD}	V
Output Logic High Drive	I_{OH}	8			mA
Output Logic Low Drive	I_{OL}	8			mA
Output Rise/Fall Time [2]	t_R/t_F				ns
< 20.00 MHz				10	
20.01 to 50.00 MHz				6	
50.01 to 125.00 MHz				3	
Duty Cycle [3] *(ordering option)*	SYM		45/55		%
Operating temperature (*ordering option*)			-10/70 or –40/85		°C
Stability [4] (*ordering option)*			±25, ±50, ±100		ppm
RMS Jitter, 12kHz to 20 MHz			0.5	1	ps
Period Jitter					ps
RMS			3.0		
Peak to Peak			21		
Output Enable/Disable [5]					V
Output Enabled		2.0			
Output Disabled				0.5	
Internal Enable Pull-Up resistor [5]			100		Kohm
Start-up time				8	ms

1. Recommend a 0.01uF and a 0.1uF capacitor between power supply and ground (close to supply).
2. Parameter is defined in Figure 3 and tested as shown in Figure 4. For fo > 90MHz, rise and fall time is measured 20 to 80%.
3. Symmetry is defined as On Time/Period (Figure 3).
4. Includes calibration tolerance, operating temperature, supply voltage variations, and shock and vibration (not under operation). ±50 and ±100ppm options include aging.
5. Output will be enabled if enable/disable is left open.

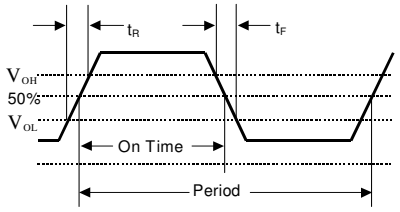


Figure 3: Output Waveform

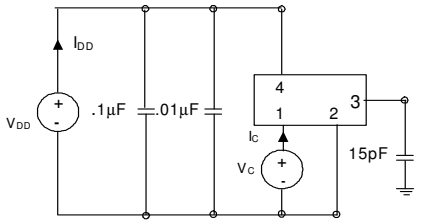


Figure 4: Typical Output Test Conditions (25±5°C)

Table 3. Electrical Performance, 2.5V option					
Parameter	**Symbol**	**Min**	**Typical**	**Maximum**	**Units**
Frequency	f_O	1.544		125.000	MHz
Operating Supply Voltage [1]	V_{DD}	2.25	2.5	2.75	V
Absolute Maximum Voltage		-0.5		5.0	V
Supply Current, Output Enabled	I_{DD}				mA
< 1.5 MHz				5	
1.500 to 20 MHz				7	
20.01 to 50 MHz				15	
50.01 to 75 MHz				20	
75.01 to 100 MHz				26	
100.01 to 125 MHz				36	
Supply Current, Out disabled	I_{DD}			30	uA
Output Logic Levels					
Output Logic High[2]	V_{OH}	0.9*V_{DD}			V
Output Logic Low[2]	V_{OL}			0.1*V_{DD}	V
Output Logic High Drive	I_{OH}	4			mA
Output Logic Low Drive	I_{OL}	4			mA
Output Logic High Drive[3]	I_{OH}	8			mA
Output Logic Low Drive[3]	I_{OL}	8			mA
Output Rise/Fall Time[2]	t_R/t_F				ns
< 20.000 MHz				10	
20.01 to 50.00 MHz				6	
50.01 to 125.00 MHz				3	
Duty Cycle[4] *(ordering option)*	SYM		45/55		%
Operating temperature (*ordering option*)			-10/70 or –40/85		°C
Stability[5] (*ordering option)*			±25, ±50, ±100		ppm
RMS Jitter, 12kHz to 20 MHz			0.5	1	ps
Period Jitter					ps
RMS			3.0		
Peak to Peak			21		
Output Enable/Disable[6]					V
Output Enabled		1.75			
Output Disabled				0.5	
Internal Enable Pull-Up resistor[6]			100		Kohm
Start-up time				8	ms

1. Recommend a 0.01uF and a 0.1uF capacitor between power supply and ground (close to supply).
2. Parameter is defined in Figure 5 and tested as shown in Figure 6.
3. Overtone designs, output frequencies > 35MHz.
4. Symmetry is defined as On Time/Period (Figure 5).
5. Includes calibration tolerance, operating temperature, supply voltage variations, and shock and vibration (not under operation). ±50 and ±100ppm options include aging.
6. Output will be enabled if enable/disable is left open.

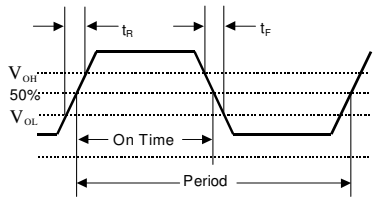


Figure 5: Output Waveform

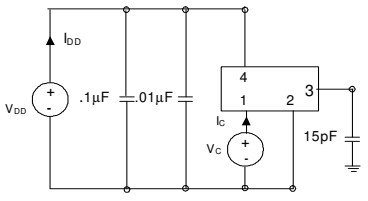


Figure 6: Typical Output Test Conditions (25±5°C)

Table 4. Electrical Performance, 1.8V option					
Parameter	**Symbol**	**Min**	**Typical**	**Maximum**	**Units**
Frequency	f_O	1.544		75.000	MHz
Operating Supply Voltage [1]	V_{DD}	1.71	1.8	1.89	V
Absolute Maximum Voltage		-0.5		3.6	V
Supply Current, Output Enabled < 20 MHz 20.01 to 70 MHz	I_{DD}			 5 15	mA
Supply Current, Out disabled	I_{DD}			30	uA
Output Logic Levels Output Logic High[2] Output Logic Low[2] Output Logic High Drive Output Logic Low Drive Output Logic High Drive[3] Output Logic Low Drive[3]	 V_{OH} V_{OL} I_{OH} I_{OL} I_{OH} I_{OL}	 0.9*V_{DD} 2.8 2.8 8 8		 0.1*V_{DD}	 V V mA mA mA mA
Output Rise/Fall Time[2] < 20.000 MHz 20.01 to 50.00 MHz 50.01 to 70.00 MHz	t_R/t_F			 10 6 3	ns
Duty Cycle[4] (*ordering option*)	SYM	45/55			%
Operating temperature (*ordering option*)		-10/70 or –40/85			°C
Stability[5] (*ordering option)*		±25, ±50, ±100			ppm
RMS Jitter, 12kHz to 20 MHz			0.5	1	ps
Period Jitter RMS Peak to Peak			 3.0 21		ps
Output Enable/Disable[6] Output Enabled Output Disabled		 1.26		 0.5	V
Internal Enable Pull-Up resistor[6]			1		Mohm
Start-up time				8	ms

1. Recommend a 0.01uF and a 0.1uF capacitor between power supply and ground (close to supply).
2. Parameter is defined in Figure 7 and tested as shown in Figure 8.
3. Overtone designs, output frequencies > 50MHz.
4. Symmetry is defined as On Time/Period (Figure 7).
5. Includes calibration tolerance, operating temperature, supply voltage variations, and shock and vibration (not under operation). ±50 and ±100 ppm options include aging.
6. Output will be enabled if enable/disable is left open.

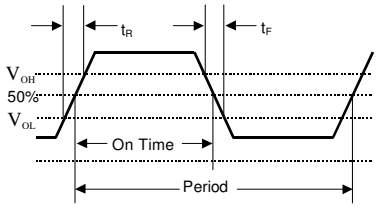


Figure 7: Output Waveform

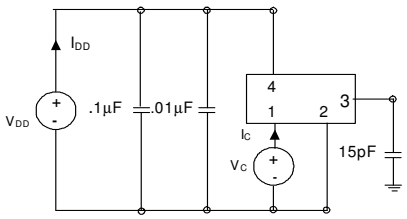


Figure 8: Typical Output Test Conditions (25±5°C)

Enable/Disable Functional Description

Under normal operation the Enable/Disable is left open, or set to a logic high state, and the VCC4 is oscillating. When the E/D is set to a logic low, the oscillator stops and the output is in a high impedance state. This helps reduce power consumption as well as facilitating board testing and troubleshooting.

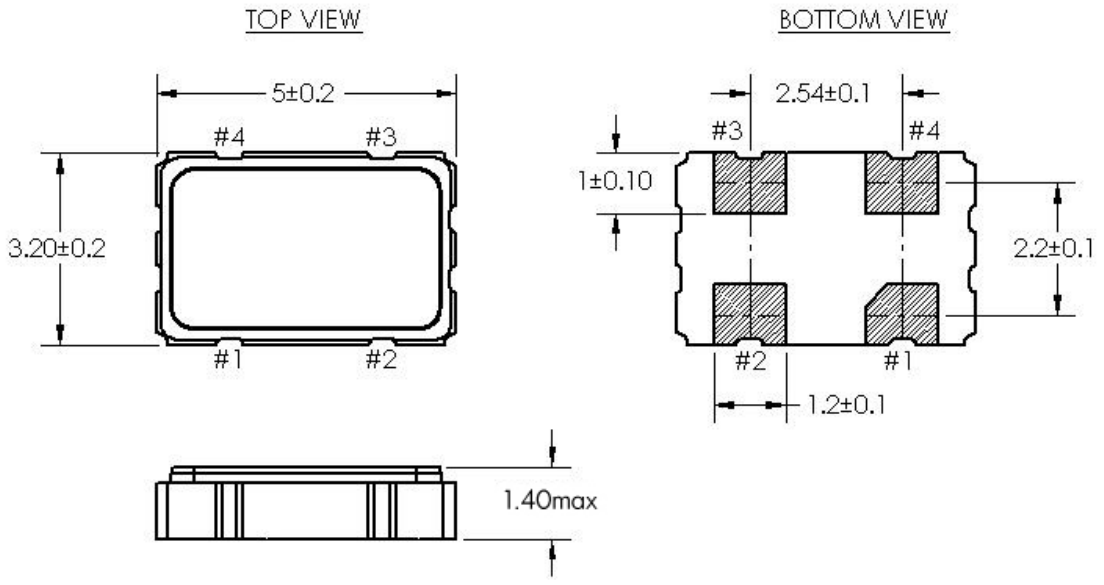
TriState Functional Description

Under normal operation the Tristate is left open or set to a logic high state. When the Tri-State is set to a logic low, the oscillator remains active but the output buffer is in a high impedance state. This helps facilitate board testing and troubleshooting.

Outline Diagrams, Pad Layout and Pin Out

Table 5. Pin out

Pin #	Symbol	Function
1	E/D or NC	Tristate, Enable/Disable or NC
2	GND	Electrical and Case Ground
3	f_O	Output Frequency
4	V_{DD}	Supply Voltage

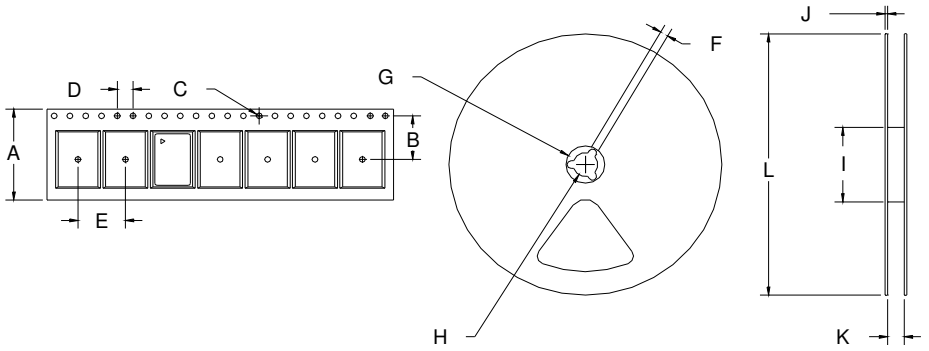


All dimensions in mm.
Contact Pads are gold over nickel

Figure 9: Package drawing

Tape and Reel

Table 6: Tape and Reel Dimensions (mm)													
Tape Dimensions						Reel Dimensions							# Per
Product	A	B	C	D	E	F	G	H	I	J	K	L	Reel
VCC4	16	7.5	1.5	4	8	2	21	13	60	2	17	180	1000



Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can permanently damage the device. Functional operation is not implied at these or any other conditions in excess of conditions represented in the operational sections of this data sheet. Exposure to absolute maximum ratings for extended periods may adversely affect device reliability.

Table 7. Absolute Maximum Ratings			
Parameter	Symbol	Ratings	Unit
Storage Temperature	Tstorage	-55/125	°C

Reliability

The VCC4 qualification tests include:

Table 8. Environmental Compliance	
Parameter	Conditions
Mechanical Shock	MIL-STD-883 Method 2022
Mechanical Vibration	MIL-STD-883 Method 2007
Temperature Cycle	MIL-STD-883 Method 1010
Solderability	MIL-STD-883 Method 2003
Gross and Fine Leak	MIL-STD-883 Method 1014
Resistance to Solvents	MIL-STD-883 Method 2015

Handling Precautions

Although ESD protection circuitry has been designed into the the VCC4, proper precautions should be taken when handling and mounting. VI employs a Human Body Model and a Charged-Device Model (CDM) for ESD susceptibility testing and design protection evaluation. ESD thresholds are dependent on the circuit parameters used to define the model. Although no industry wide standard has been adopted for the CDM, a standard HBM of resistance = 1.5kohms and capacitance = 100pF is widely used and therefore can be used for comparison purposes.

Table 9. ESD Ratings

Model	Minimum	Conditions
Human Body Model	1000	MIL-STD-883 Method 3115
Charged Device Model	1500	JESD 22-C101

Suggested IR profile

Devices are built using lead free epoxy and can also be subjected to standard lead free IR reflow conditions, Table 9 shows max temperatures and lower temperatures can also be used e.g. peak temperature of 220C.

Table 10. Reflow Profile (IPC/JEDEC J-STD-020B)

Parameter	Symbol	Value
PreHeat Time	t_S	150 sec Min, 200 sec Max
Ramp Up	R_{UP}	3 °C /sec Max
Time Above 217 °C	t_L	60 sec Min, 150 sec Max
Time To Peak Temperature	t_{AMB-P}	480 sec Max
Time At 260 °C (max)	t_P	30 sec Max
Time At 240 °C (max)	t_{p2}	60 sec Max
Ramp Down	R_{DN}	6 °C /sec Max

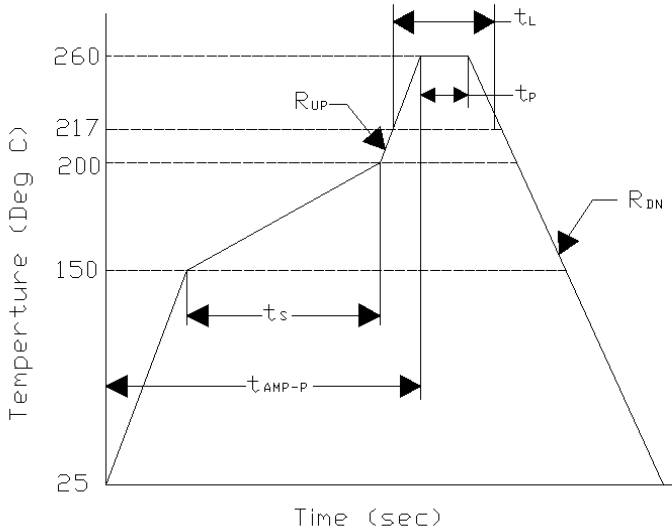


Table 11. Standard Frequency List							
9.8304	10.000	11.0596	11.0590	11.2896	12.000	12.272	12.288
12.353	13.000	13.500	13.560	14.318	14.745	16.000	16.376
16.384	16.777216	16.800	17.734	17.734475	18.432	19.440	19.660
19.800	20.000	20.480	22.000	22.5792	24.000	24.5453	24.576
25.000	26.000	27.000	27.120	28.636	28.375	30.000	32.000
32.768	33.000	33.333	34.368	36.000	37.056	37.500	40.000
44.000	44.736	48.000	49.090	50.000	54.000	60.000	66.000
75.000	100.00	106.250	125.000				

Ordering Information

VCC4 - [B] [3] [B] - [50M000]

Product Family

Crystal Oscillator

Output Frequency

In MHZ

Voltage Options

A: +5.0 Vdc ± 10%, 15pF
B: +3.3 Vdc ± 10%, 15pF
C: +3.0 Vdc ± 10%, 15pF
E: +5.0 Vdc ± 10%, 50pF
F: +3.3 Vdc ± 10%, 50pF
G: +2.5 Vdc ± 10%, 15pF
H: +1.8 Vdc ± 10%, 15pF

Electrical Options

3: Tristate, 45/55 % Duty Cycle

Following Codes are not recommended for new designs.
0: No Tristate, 40/60% Duty Cycle
1: Tristate, 40/60% Duty Cycle
2: No Tristate, 45/55% Duty Cycle
5: Enable, 40/60% Duty Cycle
6: Enable, 45/55% Duty Cycle

Stability Options

A: ±100ppm, -10 ºC to 70 ºC
C: ±100ppm, -40 ºC to 85 ºC
B: ±50ppm, -10 ºC to 70 ºC
D: ±50ppm, -40 ºC to 85 ºC
E: ±25ppm, -10 ºC to 70 ºC
F: ±25ppm, -40 ºC to 85 ºC

Note: Not all combinations are available.

Tristate with a 45/55% is the most common Electrical code and is recommended for most applications.

For Additional Information, Please Contact:

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Rev: Oct 16, 2014 VN

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Revision History

Revision Date	Approved	Description
Oct 16, 2014	VN	Modified package drawing to reflect 1.40mm maximum height. Added Revision History Table.