San Technology, Inc.

SPECIFICATION
FOR
LCD MODULE

Customer P/N:
Santek P/N: ST0500A2WCYOL-RSLW-C
DOC. Revision: RS02

Customer Approval:

	SIGNATURE	DATE
PREPARED BY	Vivian Huang	2016.09.08
CHECKED BY	Sam Liu	2016.09.08
APPROVED BY	Natty Lee	2016-Sep-12

Document Revision History

Revision	Date	Description	Changed by
RS01	2016.05.24	FIRST ISSUE	Vivian Huang
RS02	2016.09.08	Add Power Consumption (Page 4) Add Packing drawing (Page 61)	Vivian Huang

Table of Contents

1. General Specifications

1.1 Description

ST0500A2WCYOL-RSLW-C is a one cell CTP product of 5.0" color TFT-LCD(Thin Film Transistor Liquid Crystal Display),which is 9:16 aspect ratio panels for the high end Mobile application.

The 5.0" screen produces a high resolution image that is composed of 921,600(720x1280) pixel elements in a stripe arrangement. The sensor trace of touch sensor is 10x18 and the transmission interface is I2C.

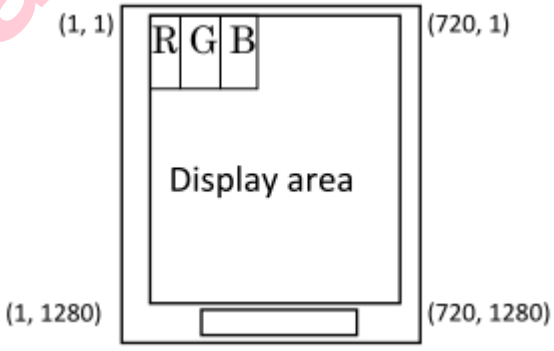
1.2 Functions & Features

Table 1. Module Functions and Features

Parameter	Value	Unit
Size	5.0	inch
Resolution	720x3(H) *1280(V)	Pixel
Display Signal Interface	MIPI 4 Lanes	-
Pixel Pitch	0.02875 (W)*0.08625 (H)	mm
NTSC	70%(typ)	-
Pixel Configuration Display Mode	R.G.B Vertical Stripe TM with Normal Black	-
Cover Lens Surface Treatment	6H	-
Viewing Direction	80/80/80/80	-
Touch Sensor Type	Capacitance	-
Touch Sensor Numbers	10TX+18RX	-
Sensor Pitch	6.28x6.23	mm
Sensor Electrical Interface	I2C	-
Power consumption	1.0 TYP, 1.2 MAX	Watt Note1

Note1: Include TFT panel, backlight and CTP.

1.3 Pixel Configuration



2. Mechanical Units

2.1 Mechanical Specification

Table 2. Module Mechanical Specification

Parameter	Value	Unit
LCM(WxHxD)	128*70*3.04(Thickness without FPC)	mm
Active Area	62.1(H)*110.4(V)	mm
With/Without CTP	With CTP	-
Weight	TBD	g
LED Numbers	14 LEDs	-
LCD Driver IC	NT35592(w/o RAM)	-
TP Sensor Driver IC	FT5346	-

3. Input / Output Terminals

NO	Symbol	I/O/P	Description	Remarks
1	NC		No Connection	
2	GND	P	Ground	
3	LED_AN		LED power	
4	NC(RSVD1)		No Connection (Future Reserved for LED Ground	
5	LED_CA2		LED Cathode 2	
6	LED_CA1		LED Cathode 1	
7	GND	P	Ground	
8	VDDI	P	Power Supply to the I/O (1.8V)	
9	GND	P	Ground	
10	FTE1	O	This signal is used for noise sensing of TP	
11	FTE	O	Frame head pulse signal	
12	LEDPWM	O	This PIN is used to connect to the external LED driver of panel backlight control	
13	RESX	I	Reset signal active low.	
14	GND	P	Ground	
15	D2P	I/O	MIPI-DSI data Lane 2 positive-end I/O	
16	D2N	I/O	MIPI-DSI data Lane 2 negative-end I/O	

17	GND	P	Ground	
18	D1P	I/O	MIPI-DSI data Lane 1 positive-end I/O	
19	D1N	I/O	MIPI-DSI data Lane 1 negative-end I/O	
20	GND	P	Ground	
21	CLKP	I	MIPI clock lane positive end	
22	CLKN	I	MIPI data lane 1 negative end	
23	GND	P	Ground	
24	D0P	I/O	MIPI-DSI data Lane 0 positive-end I/O	
25	D0N	I/O	MIPI-DSI data Lane 0 negative-end I/O	
26	GND	P	Ground	
27	D3P	I/O	MIPI-DSI data Lane 3 positive-end I/O	
28	D3N	I/O	MIPI-DSI data Lane 3 negative-end I/O	
29	GND	P	Ground	
30	VCI		Power supply to the liquid crystal power supply analog circuit (3.0V)	
31	NC(RSVD2)		No Connection (Camera Record LED)	
32	NC		No Connection	
33	ALS_INT	I	Ambient Light Sensor Interrupt	
34	GND	P	Ground	
35	NC		No Connection	
36	NC		No Connection	
37	NC		No Connection	
38	NC		No Connection	
39	NC		No Connection	
40	NC		No Connection	

Note: I/O definition: I----Input O----Output P----Power/Ground

4. CTP Specification

4.1 Construction

Construction	Materials Used	Comment
Glass LENS	Glass	Thickness：0.55mm
OCA	Adhesive	Thickness：0.15mm
ITO Sensor	ITO Sensor	Thickness：0.40 mm

4.2 Mechanical Characteristics

Item	Description	Unit
Outside Dimension	128.00*70.00（±0.1）	mm
View Area	111.10*62.80（±0.2）	mm
Active Area	112.10*63.80	mm
Thickness	1.10±0.15	mm
Input Method	Finger Or Conductive Pen	
Hardness Of Surface	≥6H	
Accuracy	+/-1mm@10mm	mm
Support Operation	Finger	
Channel	10*18	
Interface	I^2C	
Supported Operating Systems	Android2.0-5.0Windce	

4.3 Electrical Characteristics

Item	Description	Unit
Operating Voltage	DC 3.3 V	V
Insulation Resistance	＞20MΩ At DC 25V	MΩ
Insulation Ability	≥60sec. At DC 25V	sec
Chatting Times	<5ms	ms

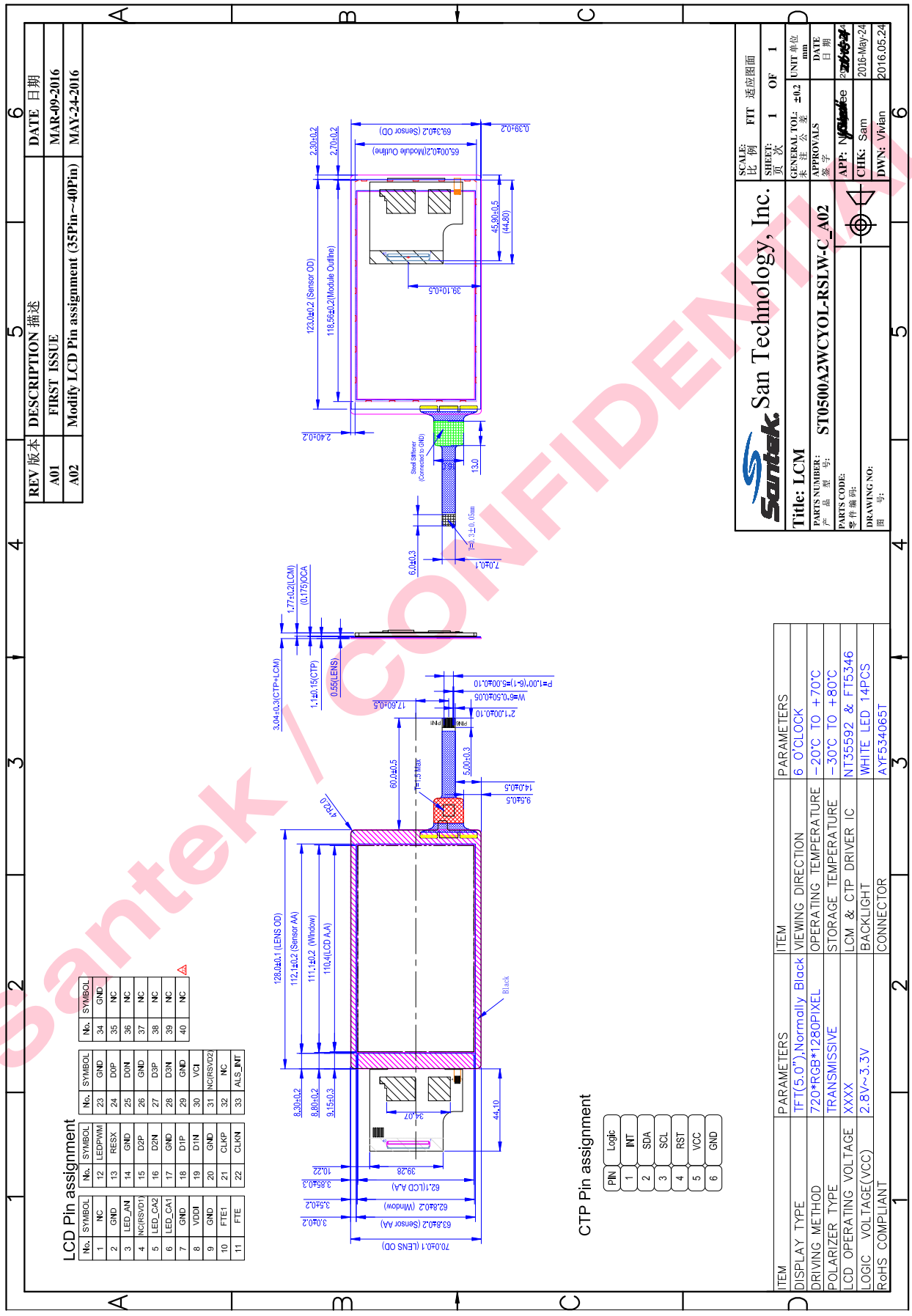
4.4 Optical Characteristics

Item	Description
Total Transmittance	≥85% [JISK7105]
Total Haze	<3% [JISK7105]

4.5 Processing Environment

Item	Description
Operating Temperature	-20℃～+70℃
Operating Humidity	≤90%RH
Storage Temperature	-30℃～+80℃
Storage Humidity	<90%RH

5. Mechanical Drawing



6. Absolute Maximum Ratings

Table 6-1

Parameter	Symbol	Rated value	Unit	Note
Driver IC(Digital) Power Supply Voltage	VDDI - GND	0 to +5.5	V	Note6-1
Driver IC(Positive Analog) Power Supply Voltage	AVDD – AGND	0 to +6.5	V	Note6-1
Driver IC(Negative Analog) Power Supply Voltage	AVEE – AGND	-6.5 to 0	V	Note6-1
Driver IC(Analog) Power Supply Voltage	VCI - AGND	0 to +5.5	V	Note6-1
Logic Input voltage range	VIN	0 to +4	V	Note6-1
Logic Output voltage rage	VO	-4 to 0	V	Note6-1
Power Supply voltage for MTP programming	MTP_PWR – GND	7.8	V	Note6-1
Temperature for storage	Tstg	-30 to +80	°C	Note6-2
Temperature for operation	Topr	-20 to +70	°C	Note6-2

GND=0V

Note6-1: Voltage applied to GND pins. GND pin conditions are based on all the same voltage (0V). Always connect all GND externally and use at the same voltage.

Note6-2: Humidity: 95%RHMax.(at Ta≤40°C). Maximum wet-bulb temperature is less than 39°C(at Ta>40°C). Condensation of dew must be avoided.

7. Electrical Characteristics

7-1. TFT-LCD Panel Driving Section

Table 7-1 GND=0V

Parameter	Symbol	Min.	Typ.	Max.	Unit	Remarks
- 2Power Mode						
DriverIC(Digital) Power Supply Voltage	VDDI	1.75	1.80	1.95	V	Note7-1
Driver IC(Analog) Power Supply Voltage	VCI	2.7	2.8	3.1	V	Note7-1
- 3Power Mode						
DriverIC(Digital) Power Supply Voltage	VDDI	1.75	1.80	1.95	V	Note7-1
Driver IC(Positive Analog) Power Supply Voltage	AVDD	4.9	5.0	5.6	V	Note7-1
Driver IC(Negative Analog) Power Supply Voltage	AVEE	-5.6	-5.0	-4.9	V	Note7-1
Input power for MTP programming	MTP_PWR	7.4	7.5	7.6	V	
Logic Input voltage (High)	V_{IH}	0.7VDDI	-	VDDI	V	Note7-2
Logic Input voltage (Low)	V_{IL}	0	-	0.3VDDI	V	Note7-2
Logic Output voltage (High)	V_{OH}	0.8VDDI	-	-	V	I_{OH}=-0.1mA
Logic Output voltage (Low)	V_{OL}	0	-	0.2IOVCC	V	I_{OL}=+0.1mA
Logic High level leakage (Except MIPI)	ILIH1			1	uA	V_{IN}=0 to VDDI
Logic Low Level Leakage (Except MIPI)	ILIL1	-1			uA	V_{IN}=0 to VDDI
Logic High level leakage MIPI	ILIH2			10	uA	V_{IN}=0 to 1.3V
Logic Low level leakage MIPI	ILIH2	-10			uA	VI_N=0 to 1.3V
Current consumption	I_{VCI}	-	21.5	35	mA	Note7-3
	I_{IOVDD1}	-	20	30	mA	Note7-3

Note7-1: Include Ripple Noise

Note7-2: Applied overshoot

Note7-3: Measurement Conditions:

Image Pattern : Full screen white pattern(V255)

Power Supply : VCI=2.8V, IOVCC=1.8V, Ta = 25°C

Video Timing : HS=4,HBP=6,HFP=6,VS=2,VBP=2,VFP=6, Frame refresh ratio 60Hz

MIPI transfer ratio : 472Mbps/lane,

MIPI Data lane number : 4lane

8. Timing Characteristics Of Input Signals

8-1.MIPI DC Characteristics

<DC characteristics>

Table 8-1 Ta=+25°C, GND=0V

Symbol	Parameter	Min	Typ	Max	Unit
Power and Operation Voltage for MIPI Receiver					
VDDAM	Power supply voltage for MIPI RX	1.7	1.8	4.8	V
VLPH	Low power mode operating voltage	1.1	1.2	1.3	V
MIPI Characteristics for High Speed Receiver					
VILHS	Single-ended input low voltage	-40	-	-	mV
VIHHS	Single-ended input high voltage	-	-	460	mV
VCMRXDC	Common-mode voltage	70	-	330	mV
ZID	Differential input impedance	80	100	125	ohm
|VOD|	HS transmit differential voltage (VOD=VDP-VDN)	140	200	250	mV
MIPI Characteristics for Low Power Mode					
VI	Pad signal voltage range	-50	-	1350	mV
VGNDSH	Ground shift	-50	-	50	mV
VIL	Logic 0 input threshold	0	-	550	mV
VIH	Logic 1 input threshold	880	-	VDDAM	mV
VHYST	Input hysteresis	25	-	-	mV
VOL	Output low level	-50	-	50	mV
VOH	Output high level	1.1	1.2	1.3	V
ZOLP	Output impedance of Low Power Transmitter	80	100	125	ohm
VIHCD_MAX	Logic 0 contention threshold	0	-	200	mV
VILCD_MIN	Logic 1 contention threshold	450	-	VDDAM	mV

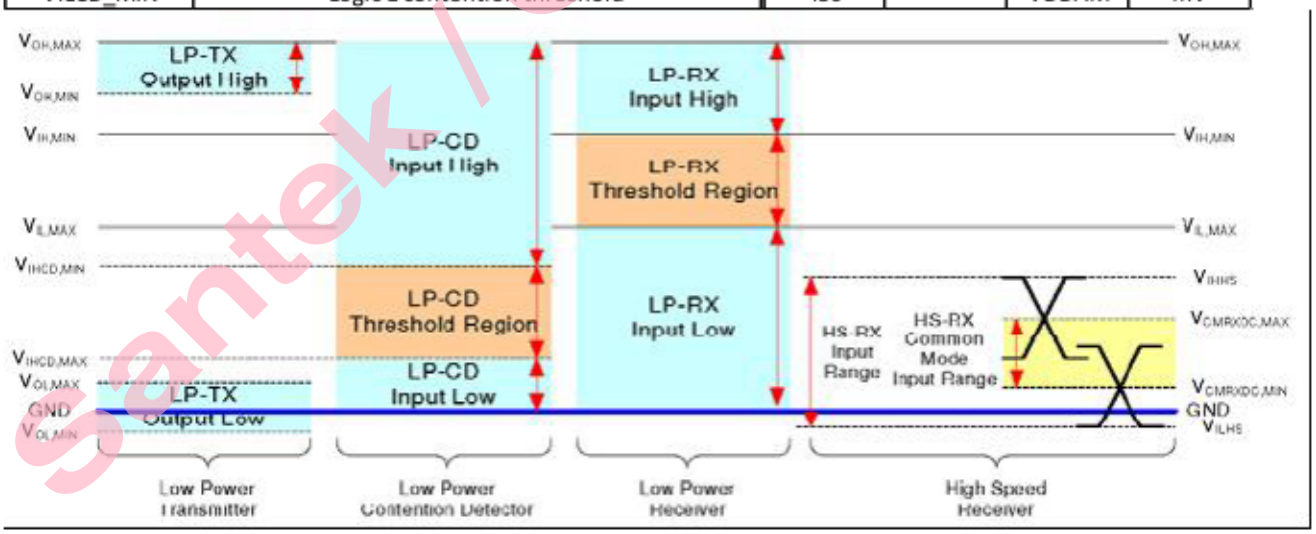


Fig. 8-1

8-2 AC Characteristics

8-2-1 High-Speed Data Transmission : Data-Clock Timing

Table 8-2-1 Ta=+25°C,GND=0V

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
UI instantaneous	UI_{INST}	1.176	-	12.5	ns	1,2,5
Data to Clock Skew [measured at transmitter]	$T_{SKEW[TX]}$	-0.15	-	0.15	UI_{INST}	3
Data to Clock Setup Time [measured at receiver]	$T_{SETUP[RX]}$	0.15			UI_{INST}	4
Data to Clock Hold Time [measured at receiver]	$T_{HOLD[RX]}$	0.15			UI_{INST}	4
20% - 80% rise time and fall time	Tr/Tf	150	-	-	ps	
		-	-	0.3	UI_{INST}	

(Note1) This value corresponds to minimum 80Mbps data rate.

(Note2) The minimum UI shall not violated for any single bit period.

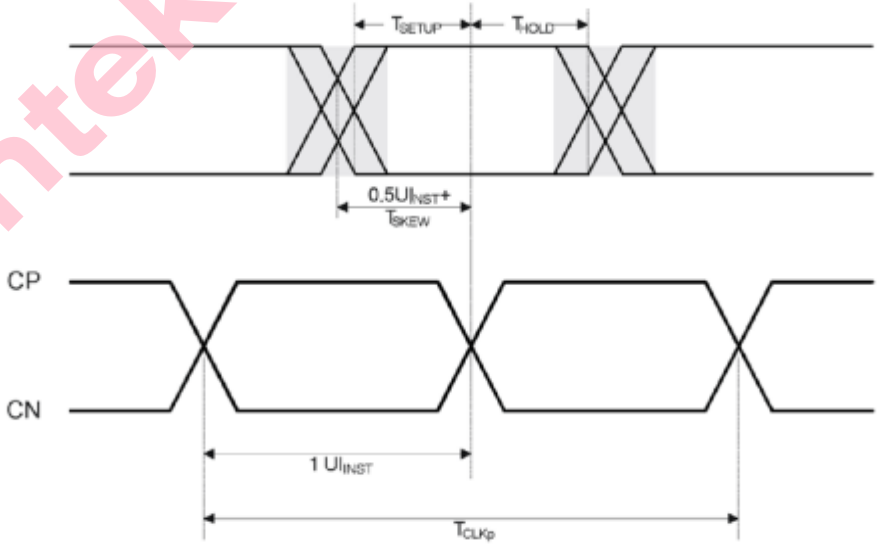
(Note3) Total delay budget of 0.3 UIINST.

(Note4) Total setup and hold window for receiver of 0.3 UIINST.

(Note5) For MIPI Speed Limitation:

[1] Per lane bandwidth is 850Mbps,

[2] Total Bit Rate : 2Gpbs for 8-8-8; 1.5Gbps for 6-6-6; 1.3Gbps for 5-6-5



8-2-2 LP Transmission AC Specification

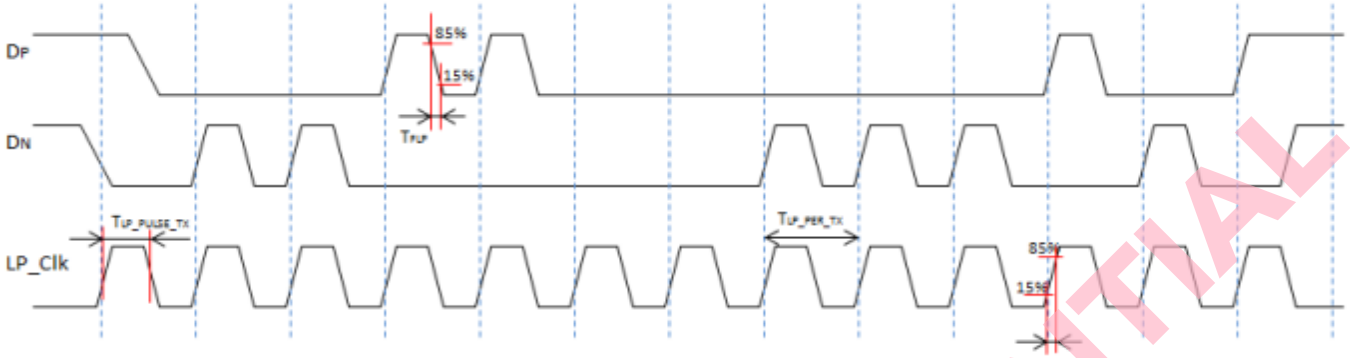


Table 8-2-2

Parameter		Symbol	Min	Typ	Max	Unit	Remarks
15%-85% rise time and fall time		T_{RLP} / T_{FLP}	-	-	25	ns	1
30%-85% rise time and fall time		T_{REO}	-	-	35	ns	1,5,6
Pulse width of the LP exclusive-OR clock	First LP exclusive-OR clock pulse after STOP state or last pulse before stop state	$T_{LP-PULSE-TX}$	40	-	-	ns	4
	All other pulses		20	--	-	ns	4
Period of the LP exclusive-OR clock		$T_{LP-PER-TX}$	90	-	-	Ns	
Slew Rate@C_{LOAD} = 0pF		$\delta V/\delta t_{SR}$	30	-	500	mV/ns	1,2,3,7
Slew Rate@ C_{LOAD} = 5pF		$\delta V/\delta t_{SR}$	30	-	200	mV/ns	1,2,3,7
Slew Rate@C_{LOAD} = 20pF		$\delta V/\delta t_{SR}$	30	-	150	mV/ns	1,2,3,7
Slow Rate@C_{LOAD} = 70pF		$\delta V/\delta t_{SR}$	30	-	100	mV/ns	1,2,3,7
Load Capacitance		C_{LOAD}	-	-	70	pF	1

(Note1) CLOAD includes the low-frequency equivalent transmission line capacitance. The capacitance of TX and RX are assumed to always be <10pF. The distributed line capacitance can be up to 50pF for a transmission line with 2ns delay.

(Note2) When the outpout voltage is between 15% and below 85% of the fully settled LP signal levels.

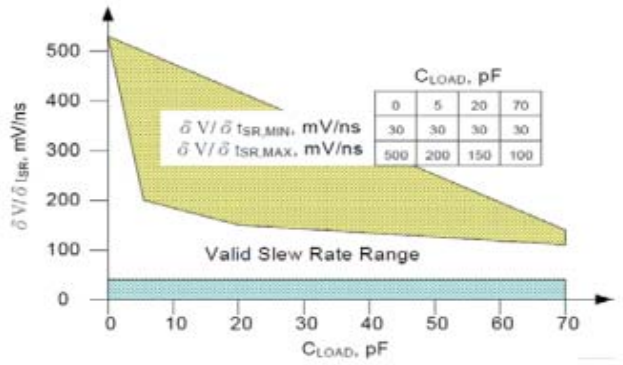
(Note3) Measured as average across any 50mV segment of the output signal transition.

(Note4) This parameter value can be lower than TLPX due to differences in rise vs. fall signal slopes and trip levels and mismatches between Dp and Dn Lp transmitters. Any Lp exclusive-OR pulse observed during HS EoT (transition from HS level LP-11) is glitch behavior.

(Note5) The rise-time of TREOT strts from the HS common-level at the moment the differential amplitude drops below 70mV, due to stopping the differential drive.

(Note6) With an additional load capacitance CCM between 0-60pF on the terminationcenter tap at RX side of the Lane.

(Note7) This value represents a corner point in a piecewise linear curve as bellowed.



8-2-3 High-Speed Data Transmission In Bursts

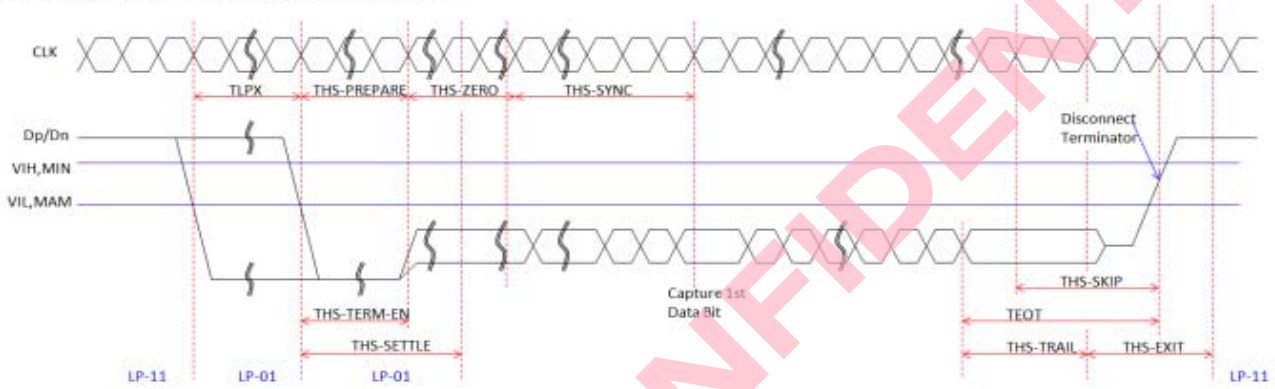


Table 8-2-3

Parameter	Symbol	Min	Typ	Max	Unit
Time to drive LP-00 to prepare for HS transmission	$T_{HS-PREPARE}$	40+4UI	-	85+6UI	ns
Time from start of tHS-TRAIL or tCLK-TRAIL period to start of LP-11 state	T_{EOT}	-	-	105+12UI	ns
Time to enable Data Lane receiver line termination measured from when Dn cross VIL,MAX	$T_{HS-TERM-EN}$	-	-	35+4UI	ns
Time to drive flipped differential state after last payload data bit of a HS transmission burst	$T_{HS-TRAIL}$	60+4UI	-	-	ns
Time-out at RX to ignore transition period of EoT	$T_{HS-SKIP}$	40	-	55+4UI	ns
Time to drive LP-11 agter HS burst	$T_{HS-EXIT}$	100	-	-	ns
Length of any Low-Power state period	T_{LPX}	50	-	-	ns
Sync sequence period	$T_{HS-SYNC}$	-	8UI	-	ns
Minimum lead HS-0 drive period before the Sync sequence	$T_{HS-ZERO}$	105+6UI	-	-	ns

(Note1) The minimum value depends on the bit rate. Implementations should ensure proper operation for all the supported bit rates.

(Note2) UI means Unit Interval, equal to one half HS the clock period on the Clock lane.

(Note3) TLPX is an internal state machine timing reference. Externally measured values may differ slightly from the specified values due to asymmetrical rise and fall times.

8-2-4 Turnaround Procedure

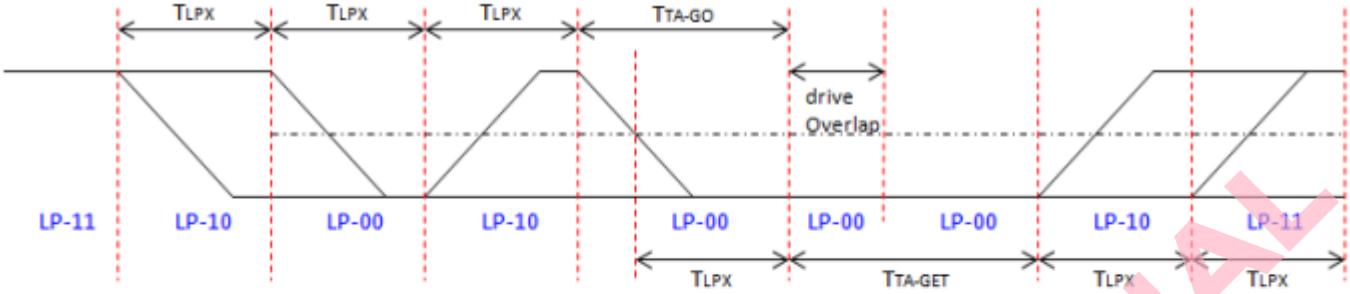


Table 8-2-4

Parameter	Symbol	Min	Typ	Max	Unit
Length of any Low-Power state period : Master side	T_{LPX}	50	-	75	ns
Length of any Low-Power state period : Slave side	T_{LPX}	50	-	75	ns
Ratio of TLPX(MASTER)/TLPX(SLAVE) between Master and Slave side	Ratio T_{LPX}	2/3	-	3/2	-
Time-out before new TX side start driving	$T_{TA-SURE}$	T_{LPX}	-	2_{TLPX}	ns
Time to drive LP-00 by new Tx	T_{TA-GET}	-	$5T_{LPX}$	-	ns
Time to drive LP-00 after turnaround Request	T_{TA-GO}	-	$4T_{LPX}$	-	ns

8-2-5 Switching the Clock Lane between Clock Transmission and Low-Power Mode

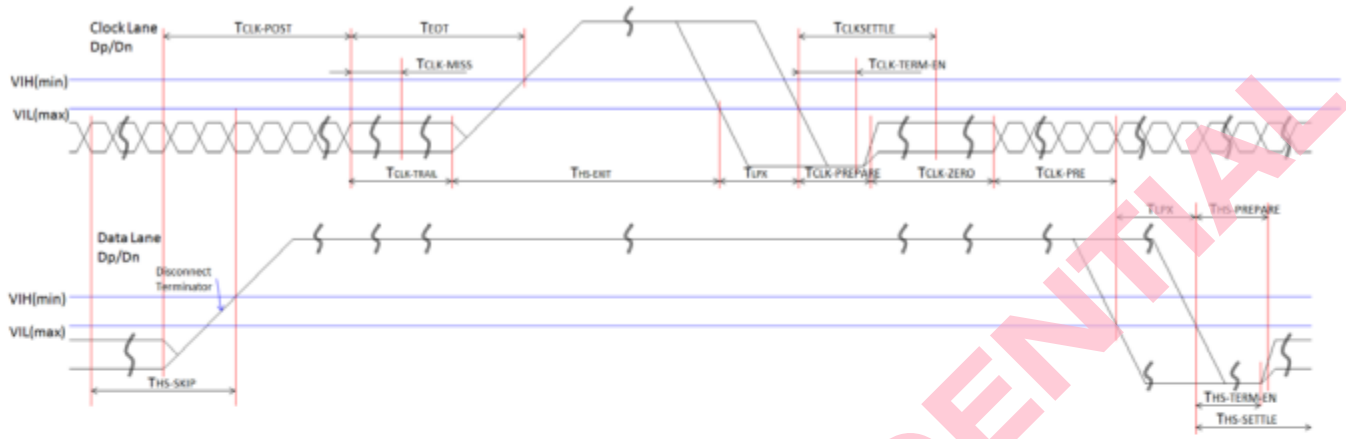


Table 8-2-5

Parameter	Symbol	Min	Typ	Max	Unit
Time that the transmitter shall continue sending HS clock after the last associated Data Lane has transitioned to LP mode	$T_{CLK-POST}$	60+152UI	-	-	ns
Detection time that the clock has stopped toggling	$T_{CLK-MISS}$	-	-	60	ns
Time to drive LP-oo to prepare for HS clock transmission	$T_{CLK-PREPARE}$	38	-	95	ns
Minimum lead HS-0 drive period before starting Clock	$T_{CLK-PREPARE}+T_{CLK-ZERO}$	300	-	-	ns
Time to enable Clock Lane receiver line termination measured from when Dn cross VIL,MAX	$T_{HS-TERM-EN}$	-	-	38	ns
Minimum time that the HS clock must be set prior to any associated date lane beginning the transmission from LP to HS mode	$T_{CLK-PRE}$	8	-	-	UI
Time to drive HS differential state after last payload clock bit of a HS transmission burst	$T_{CLK-TRAIL}$	60	-	-	ns

8-3.Reset Timing Characteristics

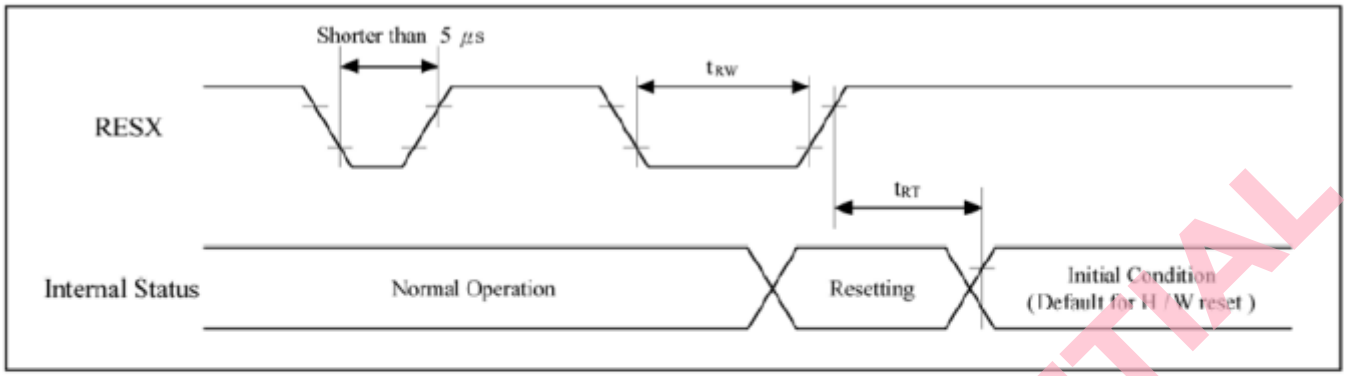


Table 8-3 Ta=-10 to 60°C, VDDI =1.75 to 1.95V, VSP=5.4V, VSN=-5.4V, GND=0V

Signal	Symbol	Parameter	Min.	Max.	Unit
RESX	t_{RW}	Reset pulse duration	10(Note)	-	us
	t_{RT}	Reset cancel	-	10(Note)	ms
			-	120(Note)	ms

Note :

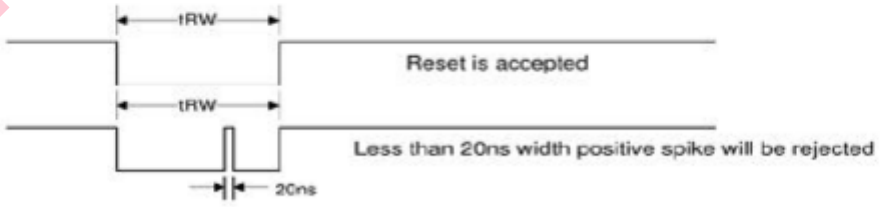
-The reset cancel also includes required time for loading ID bytes, VCOM setting and other settings from EEPROM (or similar device) to registers. This loading is done every time when there is HW reset cancel time (tRT) within 5 ms after a rising edge of RESX.

-Spike due to an electrostatic discharge on RESX line does not cause irregular system reset according to the table below :

RESX	Pulse Action
Shorter than 5us	Reset Rejected
Longer than 9us	Reset
Between 5us and 9us	Reset Starts

-During the Resetting period, the display will be blanked(The display is entering blanking sequence, which maximum time is 120 ms, when Reset Starts in Sleep-Out mode. The display remains the blank state in Sleep-In mode). Then return to Default condition for Hardware Reset.

-Spike Rejection also applies during a valid reset pulse as shown below :



-When Reset applied during Sleep-In Mode.

-When Reset applied during Sleep-Out Mode.

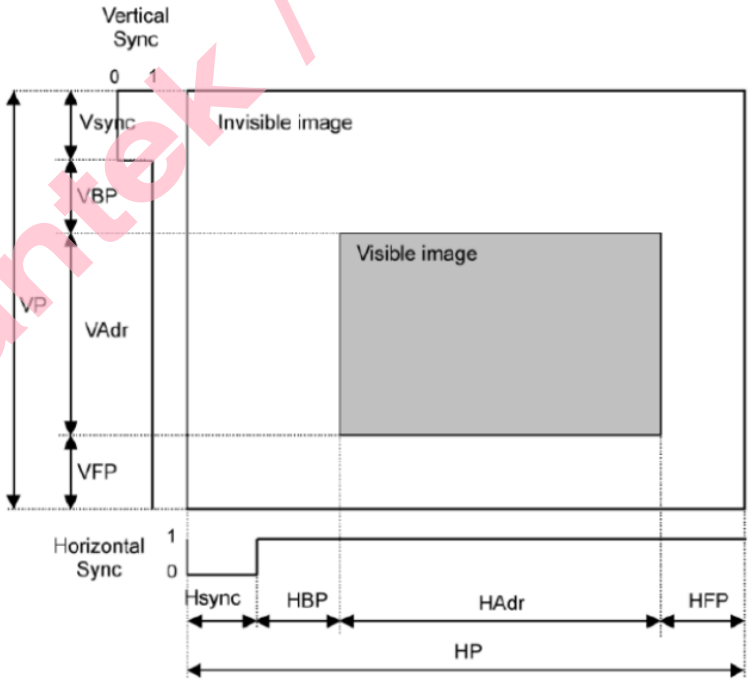
-It is necessary to wait 5ms after releasing RESX before sending commands. Also Sleep Out command cannot be sent for 120 ms.

9. Power Sequence

9-1 Video Timing

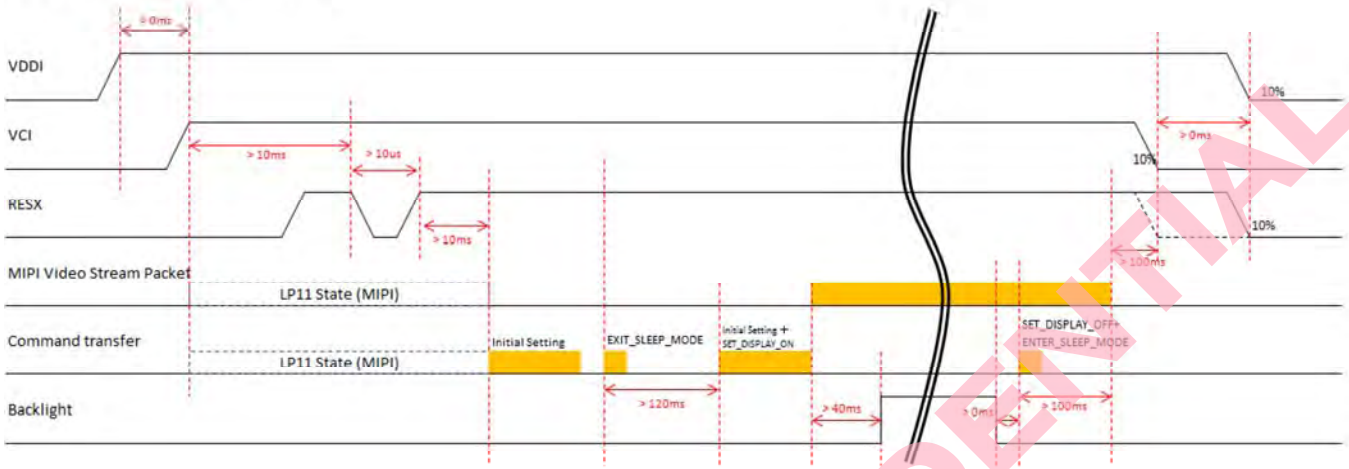
Table 9-1

Contents	Symbol	Condition	Min	Typ	Max	Unit
HS cycle	HP	HDISP+HBLK		736		PCLK
horizontal period	-		12.54	12.9	13.3	us
HS low Pulse width	HS			4		PCLK
Horizontal back porch	HBP			6		PCLK
Horizontal front porch	HFP			6		PCLK
Horizontal data start point		HS+HBP		10		PCLK
Horizontal blanking period	HBLK	HS+HBP+HFP		16		PCLK
Horizontal active area	HDISP			720		PCLK
Pixel clock frequency	PCLK		55.3	57.0	58.7	MHz
Verticle cycle	VP	VDISP+VBLK		1290		Lines
Verticle low pulse width	VS			2		Lines
Vertical front porch	VFP			6		Lines
Vertical back porch	VBP			2		Lines
Vertical data start point		VS+VBP		4		Lines
Vertical blanking period	VBLK	VS+VBP+VFP		10		Lines
Vertical active area	VDISP			1280		Lines
Vertical Refresh rate	VRR		58.2	60	61.8	Hz
MIPI Data transfer ratio (4lane)	-	-	424	472	TBD	Mbps/lane
MIPI Data transfer ratio (3lane)	-	-	528	576	TBD	Mbps/lane

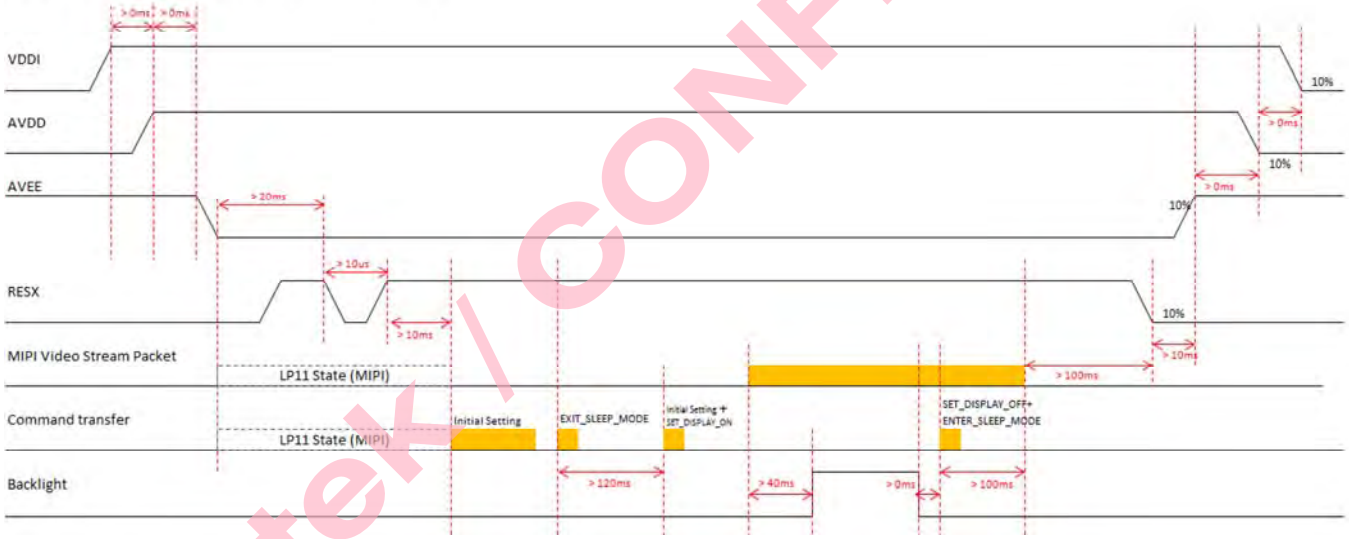


9-2 Power Supply On/Off Setting Sequence

9-2-1 2-input Power (VDDI/VCI)

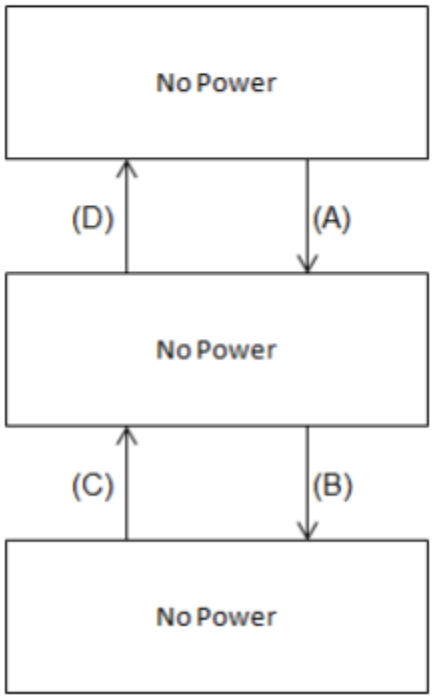


9-2-2 3-Input Power (VDDI/AVDD/AVEE)



9-3 Power On/Off Sequence

The power supply On/Off setting for No Power, Display On/Off, and Sleep mode Set/Exit sequence is illustrated in figure below.



9-3-1 2-Power (VDDI/VCI) Mode

- (A) No Power

Item	Address	Parameter	Delay	MIPI State	Data ID	Comment
<< No Power >>						
↓						
- Initial Condition	RESX = 'Low'			LP00 State		
- Power Supply VDDI	VDDI On			↓		Logic Power (Typ.1.8V)
- Wait	-		Min. 0ms	↓		Wait until Power stable
- Power Supply VCI	VCI On			LP11 State		Analog(Posi) Power (Typ.2.8V)
- Wait	-		Min. 20ms	↓		Wait until Power Stable
- Reset Release	RESX = 'High'			↓		
- Wait	-		Min. 1ms	↓		
- Reset Active	RESX = 'Low'			↓		
- Wait	-		Min. 10us	↓		
- Reset Release	RESX = 'High'			↓		
- Wait	-		Min. 20ms	LP11 State		
↓						
<< Sleep In >>						

- (B) Sleep Out

Item	Address	Parameter	Delay	MIPI State	Data ID	Comment
<< Sleep In >>						
↓						
--- *Initial Sequence for MIPI Data lane number selection*				LP State		Note : Required only for the sample of MTP Non-programming - Refer to "9-3-3 MIPI Data lane number selection"
--- *Initial Sequence for 3Power Mode*				HS State		Note : Required only for the sample of MTP Non-programming - Refer to "9-3-4 Initial Sequence "
- Host Display Data Transfer	START			HS State		Image Write (Send Video Stream Packet)
EXIT_SLEEP_MODE	0x11	-		↓	0x05	Sleep out
- Wait	-		Min. 120ms	↓		
SET_DISPLAY_ON	0x29	-		↓	0x05	Display On
↓						
<< Display On >>						

- (C) Sleep in

Item	Address	Parameter	Delay	MIPI State	Data ID	Comment
<< Display On >>						
↓						
(Normal Operation)	-	-		HS State		
SET_DISPLAY_OFF	0x28	-		↓	0x05	Display Off

ENTER_SLEEP_Mode	0x10	-		↓	0x05	Sleep in
- Wait	-		Min.100ms	↓		
- Host Display Data Transfer	STOP			LP11 State		Image Write (Send Video Stream Packet) Stop
- Wait	-	-	Min. 100ms	LP11 State		
↓						
<< Sleep In >>						

- (D) Power Off

Item	Address	Parameter	Delay	MIPI State	Data ID	Comment
<< Sleep In >>						
↓						
- Reset Active	RESX = 'Low'			LP11 State		
- Wait			Min. 10ms	↓		
- Power Supply VCI	VCI OFF			↓		
- Wait	-	-	Min. 0ms	↓		
- Power Supply VDDI	VDDI OFF			LP00 State		
↓						
<< No Power >>						

9-3-2 3-Power (VDDI/AVDD/AVEE) Mod

- (A) No Power

Item	Address	Parameter	Delay	MIPI State	Data ID	Comment
<< No Power >>						
↓						
- Initial Condition	RESX = 'Low'			LP00 State		
- Power Supply VDDI	VDDI On			↓		Logic Power (Typ.1.8V)
- Wait	-		Min. 0ms	↓		Wait until Power stable
- Power Supply AVDD	AVDD On			LP11 State		Analog(Posi) Power (Typ.5.0V)
- Wait	-		Min. 0ms	↓		Wait until Power Stable
- Power Supply AVEE	AVEE On			LP11 State		Analog(Nega) Power (Typ.-5.0V)
- Wait	-		Min. 20ms	↓		Wait until Power Stable
- Reset Release	RESX = 'High'			↓		
- Wait	-		Min. 1ms	↓		
- Reset Active	RESX = 'Low'			↓		
- Wait	-		Min. 10us	↓		
- Reset Release	RESX = 'High'			↓		
- Wait	-		Min. 20ms	LP11 State		
↓						
<< Sleep In >>						

- (B) Sleep Out

Item	Address	Parameter	Delay	MIPI State	Data ID	Comment
<< Sleep In >>						
↓						
--- Initial Sequence for MIPI Data lane number selection				LP State		Note : Required only for the sample of MTP Non-programming - Refer to "9-3-3 MIPI Data lane number selection"
--- Initial Sequence for 3Power Mode				HS State		Note : Required only for the sample of MTP Non-programming - Refer to "9-3-4 Initial Sequence "
- Host Display Data Transfer	START			HS State		Image Write (Send Video Stream Packet)
EXIT_SLEEP_MODE	0x11	-		↓	0x05	Sleep out
- Wait	-		Min. 120ms	↓		
SET_DISPLAY_ON	0x29	-		↓	0x05	Display On
↓						
<< Display On >>						

- (C) Sleep in

Item	Address	Parameter	Delay	MIPI State	Data ID	Comment
<< Display On >>						

↓						
(Normal Operation)	-	-		HS State		
SET_DISPLAY_OFF	0x28	-		↓	0x05	Display Off
ENTER_SLEEP_Mode	0x10	-		↓	0x05	Sleep in
- Wait	-		Min.100ms	↓		
- Host Display Data Transfer	STOP			LP11 State		Image Write (Send Video Stream Packet) Stop
- Wait	-	-	Min. 100ms	LP11 State		
↓						
<< Sleep In >>						

- (D) Power Off

Item	Address	Parameter	Delay	MIPI State	Data ID	Comment
<< Sleep In >>						
↓						
- Reset Active	RESX = 'Low'			LP11 State		
- Wait			Min. 10ms	↓		
- Power Supply AVEE	AVEE OFF			↓		
- Wait	-	-	Min. 0ms	↓		
- Power Supply AVDD	AVDD OFF			↓		
- Wait	-	-	Min. 0ms	↓		
- Power Supply VDDI	VDDI OFF			LP00 State		
↓						
<< No Power >>						

9-3-3 MIPI Data Lane number selection

MIPI Data Lane number selection can be MTP one time. When Customer MTP the register first time, the setting value will be programmed. So, The Sequence of the following is unnecessary, if the sample which carried out “MTP Programming” once does not need to change MIPI Data Lane number.

<< MIPI Data Lane = 4 Lane >>

Item	2Power Mode		3Power Mode		Data ID
	Address	Parameter	Address	Parameter	
CMD Page select	0xFF	0x00	0xFF	0x00	0x15
Reload CMD	0xFB	0x01	0xFB	0x01	0x15
SET_MIPI_LANE	0xBA	0x03	0xBA	**0x03**	0x15

<< MIPI Data Lane = 3 Lane >>

Item	2Power Mode		3Power Mode		Data ID
	Address	Parameter	Address	Parameter	
CMD Page select	0xFF	0x00	0xFF	0x00	0x15
Reload CMD	0xFB	0x01	0xFB	0x01	0x15
SET_MIPI_LANE	0xBA	0x02	0xBA	**0x02**	0x15

9-3-4 Initial Sequence

The Initial Sequence can be MTP on time (except VCOMDC, ID1, ID2, ID3, DDB). When Customer MTP the register first time, the setting value will be programmed. So, the sequence of the following is unnecessary, if the sample which carried out “MTP Programming” once does not need to change each setting values.

Item	Address	2Power Mode	3Power Mode	Data ID	Comment
		Parameter	Parameter		
Page Select	0xFF	0x01	<--	0x15	**- CMD2, Page0 -**
Reload CMD	0xFB	0x01	<--	0x15	Don't reload MTP
Panel CTRL 1	0x00	0x2A	<--	0x15	Normally black, HD720
PWR CTRL1	0x01	0x33	<--	0x15	AVDD/AVEE setting
PWR CTRL2	0x02	0x53	<--	0x15	VGH/VGL setting
PWR CTRL3	0x03	0x55	<--	0x15	-
PWR CTRL4	0x04	0x55	<--	0x15	-
PWR CTRL5	0x05	0x00	<--	0x15	AVDD/AVEE setting
PWR CTRL6	0x06	0x3B	<--	0x15	AVDD/AVEE setting
PWR CTRL 8	0x08	0x26	<--	0x15	VGH/VGL setting
PWR CTRL 9	0x09	0x09	<--	0x15	VGL setting
REG CTRL 1	0x0B	0xCA	<--	0x15	GVDDP setting
REG CTRL 2	0x0C	0xCA	<--	0x15	GVDDN setting
REG CTRL 3	0x0D	0x24	<--	0x15	VCI1 setting
REG CTRL 4	0x0E	0x2B	<--	0x15	VGH setting
REG_CTRL 5	0x0F	0x96	<--	0x15	VGLO setting
REG_CTRL 6	0x10	0x0F	<--	0x15	-
REG CTRL 7	0x11	***adjusted value***	***adjusted value***	0x15	**VCOMDC voltage setting ※ Refer to "9-3-5 VCOMDC adjustment "**
REG CTRL 8	0x12	0x03	<--	0x15	-
Driver & Panel CTRL	0x14	0x01	**0x0C**	0x15	Enginner Setting
DDB CTRL1	0x23	***user setting***	***user setting***	0x15	***- SID[7:0] MIPI member ID number***
DDB CTRL2	0x24	***user setting***	***user setting***	0x15	***- SID[15:8] MIPI menber ID number***
DDB CTRL3	0x25	***user setting***	***user setting***	0x15	***- MID[7:0] Module ID***
DDB CTRL4	0x26	***user setting***	***user setting***	0x15	***- MID[15:8] Module ID***

DDB CTRL5	0x27	***user setting***	***user setting***	0x15	***- RID[7:0] Revision ID***
DDB CTRL6	0x28	***user setting***	***user setting***	0x15	***- RID[15:8] Revision ID***
Gate CTRL A	0x36	0x73	<--	0x15	gate setting
no description	0x37	0x02	<--	0x15	VGLO pulldonw (GND) in Sleep In
WID_CTRL1	0x44	***user setting***	***user setting***	0x15	***- This read byte identifies the display module's manufacturer.***
WID_CTRL2	0x45	***user setting***	***user setting***	0x15	***- This read byte is used to track the display module/driver version.***
WID_CTRL3	0x46	***user setting***	***user setting***	0x15	***- This read byte identifies the display module/dirver.***
Auto-detect VBP and VFP	0x4C	0x01	<--	0x15	enable
Gate CTRL B	0x6F	0x00	<--	0x15	gate setting
MIPI CTRL 1	0x71	0x2C	<--	0x15	TA_GO & TA-GET period
Page Leave	FF h	0x00	<--	0x15	CMD1 is Selected.
RELOAD CMD	FB h	0x01	<--	0x15	Don't reload MTP
Gamma Setting	-	-	-		Refer to "9-5 Gamma table"
Page Select	0xFF	0x04	<--	0x15	**- CMD2, Page3 - * "CABC function"**
Reload CMD	0xFB	0x01	<--	0x15	Don't reload MTP
Page Leave	FF h	0x00	<--	0x15	CMD1 is Selected.
RELOAD CMD	FB h	0x01	<--	0x15	Don't reload MTP
Page Select	0xFF	0x05	<--	0x15	**- CMD2, Page4 -**
Reload CMD	0xFB	0x01	<--	0x15	Don't reload MTP
CGS CTRL 1	0x01	0x00	<--	0x15	panel timing setting
CGS CTRL 2	0x02	0x7F	<--	0x15	panel timing setting
CGS CTRL 3	0x03	0x7F	<--	0x15	-
CGS CTRL 4	0x04	0x7F	<--	0x15	-
CGS CTRL 5	0x05	0x00	<--	0x15	panel timing setting
CGS CTRL 6	0x06	0x00	<--	0x15	-
CGS CTRL 7	0x07	0x00	<--	0x15	panel timing setting
CGS CTRL 8	0x08	0x00	<--	0x15	-
CGS CTRL 9	0x09	0x02	<--	0x15	panel timing setting
CGS CTRL 10	0x0A	0x01	<--	0x15	panel timing setting
CGS CTRL 11	0x0B	0x75	<--	0x15	panel timing setting
CGS CTRL 12	0x0D	0x0E	<--	0x15	panel timing setting
CGS CTRL 13	0x0E	0x1A	<--	0x15	panel timing setting
CGS CTRL 14	0x0F	0x09	<--	0x15	panel timing setting
CGS CTRL 15	0x10	0x80	<--	0x15	panel timing setting
CGS CTRL 18	0x14	0x04	<--	0x15	panel timing setting
CGS CTRL 19	0x16	0x08	<--	0x15	panel timing setting
CGS CTRL 20	0x17	0x00	<--	0x15	panel timing setting
CGS CTRL 21	0x19	0x1F	<--	0x15	panel timing setting
CGS CTRL 22	0x1A	0x00	<--	0x15	panel timing setting
CGS CTRL 23	0x1B	0xFC	<--	0x15	panel timing setting
CGS CTRL 24	0x1C	0x00	<--	0x15	panel timing setting
CGS CTRL 25	0x1D	0x00	<--	0x15	panel timing setting
CGS CTRL 26	0x1E	0x00	<--	0x15	panel timing setting
CGS CTRL 27	0x1F	0x80	<--	0x15	panel timing setting
Driver & Panel CTRL	0x21	**0x00**	<--	0x15	panel timing setting **(Scanning direction ; Forward='0x00', Backward='0x07')**

In CMD2,Page3 , these register is used for "CABC function".
Please set up after carrying out sufficient evaluation.

					※ Refer to "9-3-6 Panel Scanning direction "
Driver & panel CTRL	0x24	0x45	<--	0x15	engineer setting
Driver & panel CTRL	0x27	0x05	<--	0x15	engineer setting
Driver & panel CTRL	0x28	0x00	<--	0x15	engineer setting
Driver & panel CTRL	0x29	0x52	<--	0x15	engineer setting
Driver & panel CTRL	0x2A	0xA9	<--	0x15	engineer setting
Display CTRL 4	0x2D	0x02	<--	0x15	panel timing setting
Driver & panel CTRL	0x2F	0x00	<--	0x15	engineer setting
Driver & panel CTRL	0x30	0x30	<--	0x15	engineer setting
Driver & panel CTRL	0x35	0x16	<--	0x15	engineer setting
GATE CTRL 1	0x36	0x01	<--	0x15	panel timing setting
GATE CTRL 2	0x37	0x00	<--	0x15	panel timing setting
GATE CTRL 3	0x38	0x02	<--	0x15	panel timing setting
GATE CTRL 4	0x39	0x01	<--	0x15	panel timing setting
INIT CTRL 1	0x3F	0x00	<--	0x15	panel timing setting
INIT CTRL 2	0x40	0x00	<--	0x15	panel timing setting
INIT CTRL 3	0x41	0x00	<--	0x15	panel timing setting
INIT CTRL 4	0x42	0x00	<--	0x15	panel timing setting
Driver & panel CTRL	0x4A	0x01	<--	0x15	engineer setting
SWAP CTRL	0x6F	0x25	<--	0x15	Driving setting
Driver & panel CTRL	0x7E	0xE9	<--	0x15	engineer setting
Driver & panel CTRL	0x82	0x18	<--	0x15	engineer setting
Driver & panel CTRL	0x89	0xC1	<--	0x15	engineer setting
Driver & panel CTRL	0xA4	0x05	<--	0x15	Driving setting
PORCH CTRL 1	0xBB	0x06	<--	0x15	FP=6
PORCH CTRL 2	0xBC	0x02	<--	0x15	BP=2
Page Leave	0xFF	0x00	<--	0x15	CMD1 is Selected.
RELOAD CMD2 , PAGE0	0xFB	0x01	<--	0x15	Don't reload MTP

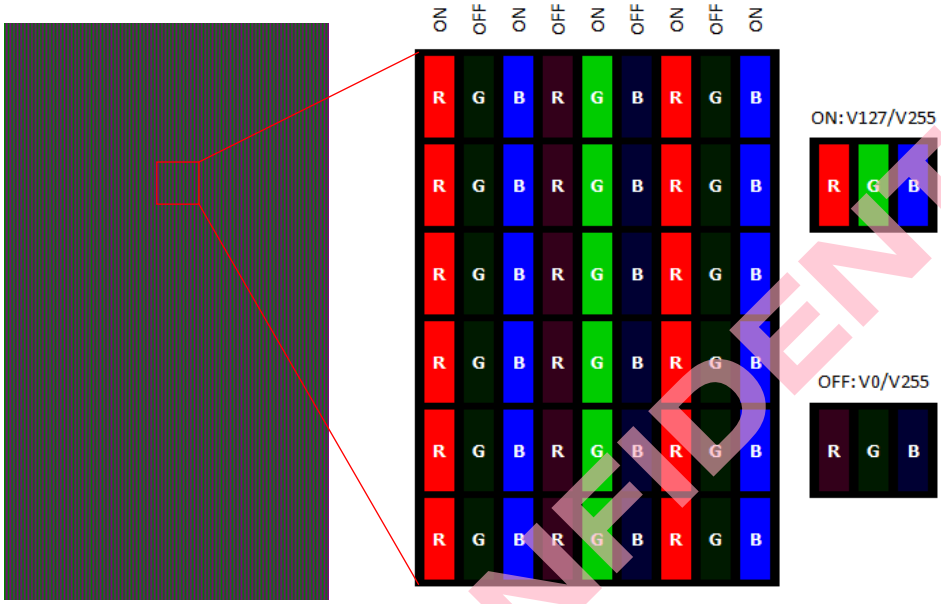
9-3-5 VCOMDC adjustment

The method for minimizing “Flicker display” is explained.

<Step1>

Please display on a LCD module “Image Pattern (Flicker Pattern)” which shows in the following figure.

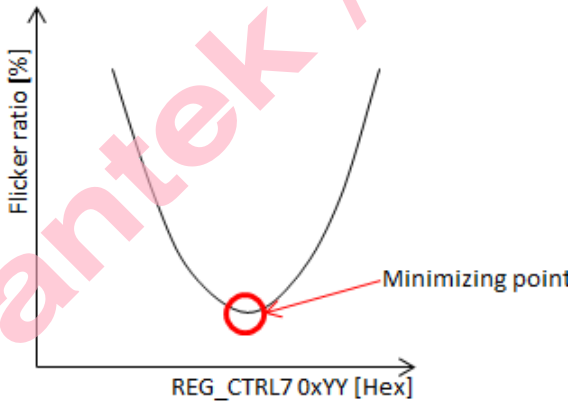
- Image Pattern (Flicker Pattern)



Note) Resolution : 720RGB x 1,280, Color depth : 24bits

<Step2>

In order that Flicker may look for the value used as the minimum, please carry out variable of he value of the Driver register “REG CTRL 7 (0x11)”. The following figure shows the relation between the Driver register “REG_CTRL7” Setting value[Hex] and Flicker ratio[%], and point by which flicker is minimized.



Note) the point with which Flicker raito is minimized will be only one point.

<Step3>

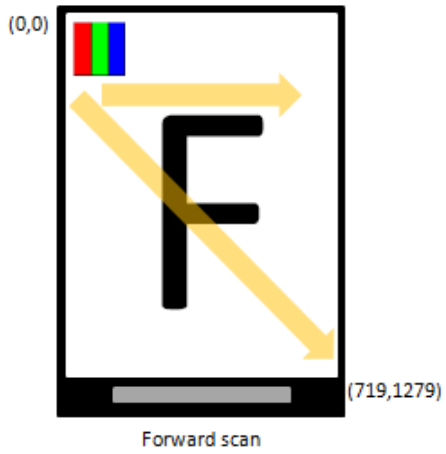
Please perform the value looked for in Initial Sequence, and carry out “MTP Programming Sequence”

<Step4>

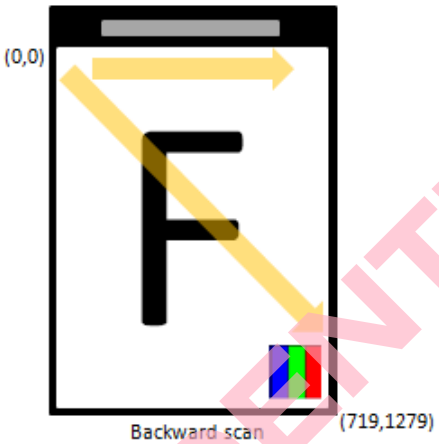
Without carrying out Initial Sequence, please carry out Power On Sequence and check whether Flicker is adjusted appropriately.

9-3-6 Panel Scanning direction

This LCD module can change the scanning direction Panel. Please set up according to the specification of customer's application.



Forward scan



Backward scan

- Forward Scanning direction setting value

Item	Address	Parameter	Data ID	Comment
<< **Forward** Scan >>				
Page Select	0xFF	0x05	0x15	CMD2, Page0 is selected.
Driver & Panel CTRL	0x21	**0x00**	0x15	forward scanning direction
Page leave	0xFF	0x00	0x15	CMD1 is selected.

- Backward Scanning direction setting value

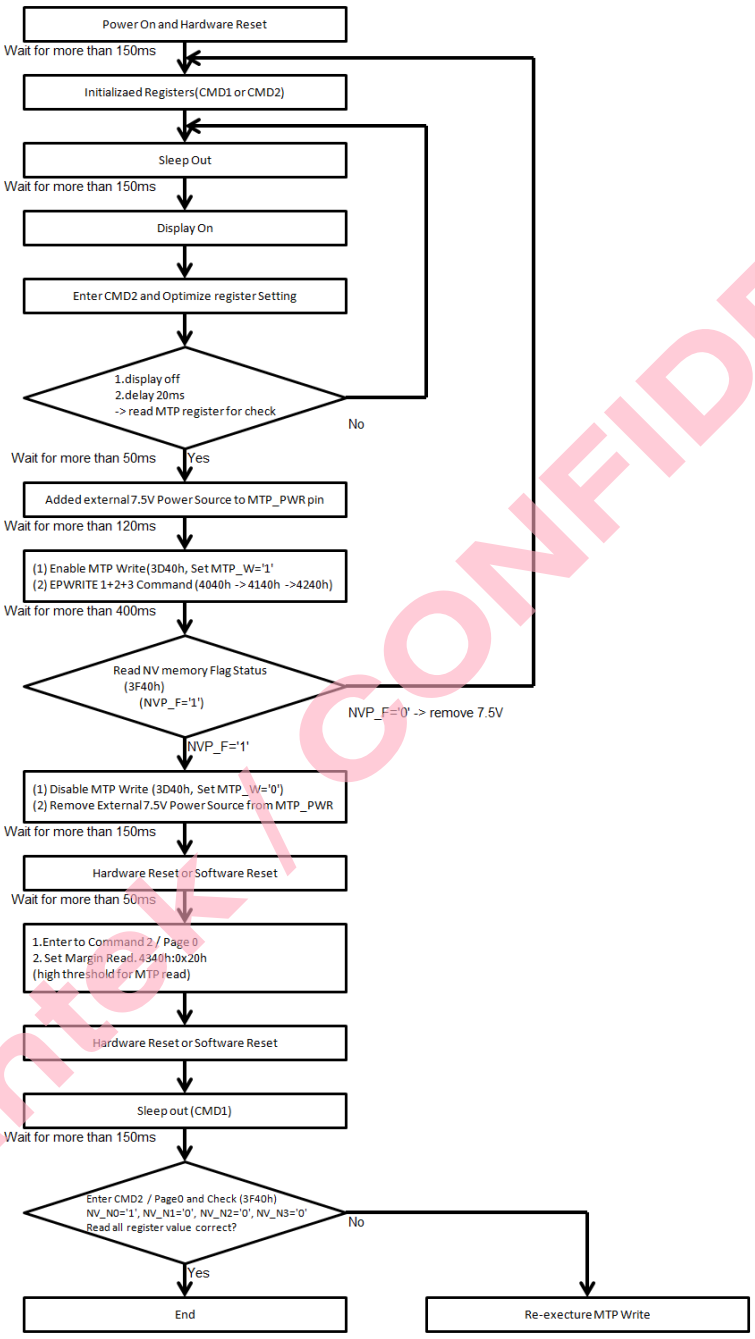
Item	Address	Parameter	Data ID	Comment
<< **Backward** Scan >>				
Page Select	0xFF	0x05	0x15	CMD2, Page0 is selected.
Driver & Panel CTRL	0x21	**0x07**	0x15	backward scanning direction
Page leave	0xFF	0x00	0x15	CMD1 is selected.

9-4 MTP programming Sequence

Input power for NV memory programming

MTP_PWR input voltage range: 7.4～7.6(Typical=7.5V). When not under programming, MTP_PWR pin can be floating or tied to ground. The worse current of MTP_PWR is 20mA

9-4-1 First time MTP Programming



sequence

Note :

1. During this step, user have to ensure that all registers are optimal for display, because most registers “only” have one MTP programming chance.

Sequence of each 2Power mode/3Power mode is shown below.

9-4-1-1 2Power(VDDI/VCI) Mode (1st time MTP Programming)

<< 2 Power Mode >>

Item	Address	Parameter	Delay	MIPI State	Data ID	Comment
- Initial Condition	RESX = 'Low'			LP00 State		
- Power Supply VDDI	VDDI ON			↓		Logic Power (Typ.1.8V)
- Wait	-		Min. 0ms	↓		Wait until Power stable
- Power Supply VCI	VCI ON			LP11 State		Analog Power (Typ.2.8V)
- Wait	-		Min. 20ms	↓		Wait until Power Stable
- Reset Release	RESX = 'High'			↓		
- Wait	-		Min. 1ms	↓		
- Reset Active	RESX = 'Low'			↓		
- Wait	-		Min. 10us	↓		
- Reset Release	RESX = 'High'			↓		
- Wait	-		Min. 150ms	↓		
--- Initial Sequence for MIPI Data lane number selection				LP State		Refer to "9-3-3 MIPI Data lane number selection"
Page select	0xFF	0x01		↓	0x15	CMD2, Page0 is selected
Reload CMD	0xFB	0x01		↓	0x15	Don't reload MTP
RD_CMDSTATUS	0xFE	Read value		↓	0x06	- Expected return value = '0x02'
MTP_CTRL	0x3F	Read value		↓	0x06	- Expected return value = '0x00'
Page Leave	0xFF	0x00		↓	0x15	CMD1 is selected.
Reload CMD	0xFB	0x01		↓	0x15	Don't reload MTP
--- Initial Sequence for 2Power Mode				HS State		Refer to " 9-3-4 Initial Sequence for 2power mode"
EXIT_SLEEP_MODE	0x11	-		↓	0x05	Sleep out
- Wait	-		Min. 150ms	↓		
SET_DISPLAY_ON	0x29	-		↓	0x05	Display On
-- Host Display Data Transfer	START			↓		Image : Flicker Pattern
Page select	0xFF	0x01		↓	0x15	CMD2, Page0 is selected
Reload CMD	0xFB	0x01		↓	0x15	Don't reload MTP
RD_CMDSTATUS	0xFE	Read value		↓	0x06	- Expected return value = '0x02'
Page Leave	0xFF	0x00		↓	0x15	CMD1 is selected.
Reload CMD	0xFB	0x01		↓	0x15	Don't reload MTP
RD_CMDSTATUS	0xFE	Read value		↓	0x06	- Expected return value = '0x01'
REG CTRL 7	0x11	*0xYY*		↓	0x15	*Set VCOMDC3_REG[7:0], YY:Optimize value setting*
SET_DISPLAY_OFF	0x28	-		↓	0x05	Display Off
- Wait	-		Min. 20ms	↓		
- Host Display Data Transfer	STOP / Continue			LP State / HS State		
(Read each register value for check)						※ If all data is not good, re-execute MTP Write
- Wait	-		Min. 50ms	↓		

- Added external 7.5V(typ.) Power Source to MTP_PWR_pin				↓		
- Wait	-		Min. 120ms	↓		
Page select	0xFF	0x01		↓	0x15	CMD2, Page0 is selected.
Reload CMD	0xFB	0x01		↓	0x15	Don't reload MTP
RD_CMDSTATUS	0xFE	Read value		↓	0x06	- Expected return value = '0x02'
MTP_CTRL1	0x3D	0x01		↓		Enable MTP Write (MTP_W[0]='1')
MTP_CTRL3	0x40	0x55		↓	0x15	EPWRITE1 (4040h=0055h)
MTP_CTRL4	0x41	0xAA		↓	0x15	EPWRITE2 (4140h=00AAh)
MTP_CTRL5	0x42	0x66		↓	0x15	EPWRITE3 (4240h=0066h)
- Wait	-		Min. 400ms	↓		
MTP_CTRL2	0x3F	Read value		↓	0x06	- Expected return value = '0x01'
MTP_CTRL1	0x3D	0x00		↓	0x15	Disable MTP Write (MTP_W[0]='0')
- Removed external 7.5V(Typ.) Power Source from MTP_PWR_pin				↓		
- Wait	-		Min .150ms	↓		
Page Leave	0xFF	0x00		↓	0x15	CMD1 is selected.
Reload CMD	0xFB	0x01		↓	0x15	Don't reload MTP
RD_CMDSTATUS	0xFE	Read value		↓		- Expected return value = '0x01'
ENTER_SLEEP_MODE	0x10	-		↓	0x15	
- Wait			Min. 100ms	↓		
- Reset Active	RESX = 'Low'			↓		
- Wait	-		Min. 10us	↓		
- Reset Release	RESX = 'High'			↓		
- Wait	-		Min. 150ms	↓		
Page Select	0xFF	0x01		↓	0x15	CMD2, Page0 is selected.
Reload CMD	0xFB	0x01		↓	0x15	Don't reload MTP
RD_CMDSTATUS	0xFE	Read value		↓	0x06	- Expected Return value = '0x02'
MTP_CTRL6	0x43	0x20		↓	0x15	Set Margin Read
(Read each register value for check)				↓		※ If all data is not good, re-executer MTP Write
- Reset Active	RESX = 'Low'			↓		
- Wait	-		Min. 10us	↓		
- Reset Release	RESX = 'High'			↓		
- Wait	-		Min. 20ms	↓		
EXIT_SLEEP_MODE	0x11	-		↓	0x05	Sleep out
- Wait			Min. 120ms	↓		
Page Select	0xFF	0x01		↓	0x15	CMD2, Page0 is selected.
MTP_CTRL2	0x3F	Read value		↓	0x15	- Expected return value = '0x10'
(Read each register value for check)				↓		※ If all data is not good, re- execute MTP Write
Page leave	0xFF	0x00		↓	0x15	CMD1 is selected.
ENTER_SLEEP_MODE	0x10		Min. 100ms	↓	0x05	Sleep in

- Host Display Data Transfer	STOP			LP11 State		Image Write Stop (Send Video Stream Packet)
- Wait	-	-	Min. 100ms	↓		
- Reset Active	RESX = 'Low'			LP00 State		
- Wait			Min. 10ms	↓		
- Power Supply VCI	VCI OFF			↓		
- Wait	-	-	Min. 0ms	↓		
- Power Supply VDDI	VDDI OFF			LP00 State		

9-4-1-2 3Power(VDDI/AVDD/AVEE) Mode (1st time MTP Programming)

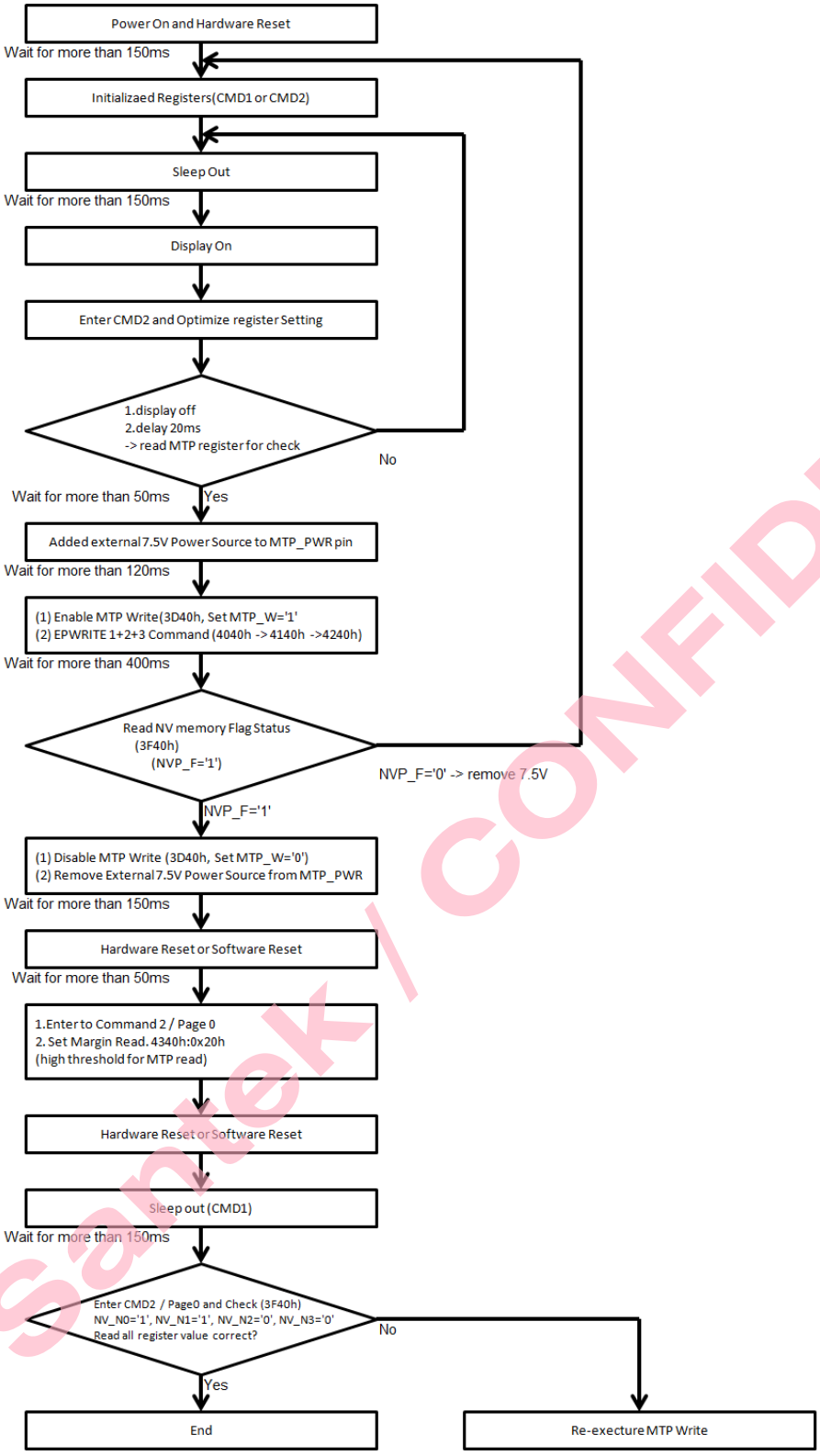
<< 3 Power Mode >>

Item	Address	Parameter	Delay	MIPI State	Data ID	Comment
- Initial Condition	RESX = 'Low'			LP00 State		
- Power Supply VDDI	VDDI ON			↓		Logic Power (Typ.1.8V)
- Wait	-		Min. 0ms	↓		Wait until Power stable
- Power Supply AVDD	AVDD ON			LP11 State		Analog(Posi) Power (Typ.5.0V)
- Wait	-		Min. 0ms	↓		Wait until Power Stable
- Power Supplya AVEE	AVEE ON			↓		Analog(Nega) Power (Typ.-5.0V)
- Wait	-		Min. 20ms	↓		
- Reset Release	RESX = 'High'			↓		
- Wait	-		Min. 1ms	↓		
- Reset Active	RESX = 'Low'			↓		
- Wait	-		Min. 10us	↓		
- Reset Release	RESX = 'High'			↓		
- Wait	-		Min. 150ms	↓		
--- *Initial Sequence for MIPI Data lane number selection*				LP State		Refer to "9-3-3 MIPI Data lane number selection"
Page select	0xFF	0x01		↓	0x15	CMD2, Page0 is selected
Reload CMD	0xFB	0x01		↓	0x15	Don't reload MTP
RD_CMDSTATUS	0xFE	Read value		↓	0x06	- Expected return value = '0x02'
MTP_CTRL2	0x3F	Read value		↓	0x06	- Expected return value = '0x00'
Page Leave	0xFF	0x00		↓	0x15	CMD1 is selected.
Reload CMD1	0xFB	0x01		↓	0x15	Don't reload MTP
--- *Initial Sequence for 3Power Mode*				HS State		Refer to "9-3-4 Initial Sequence for 3power mode"
EXIT_SLEEP_MODE	0x11	-		↓	0x05	Sleep out
- Wait	-		Min. 150ms	↓		
SET_DISPLAY_ON	0x29	-		↓	0x05	Display On
-- Host Display Data Transfer	START			↓		Image : Flicker Pattern
Page select	0xFF	0x01		↓	0x15	CMD2, Page0 is selected
Reload CMD	0xFB	0x01		↓	0x15	Don't reload MTP
RD_CMDSTATUS	0xFE	Read value		↓	0x06	- Expected return value = '0x02'
Page Leave	0xFF	0x00		↓	0x15	CMD1 is selected.
Reload CMD	0xFB	0x01		↓	0x15	Don't reload MTP
RD_CMDSTATUS	0xFE	Read value		↓	0x06	- Expected return value = '0x01'
REG CTRL 7	0x11	*0xYY*		↓	0x15	*Set VCOMDC3_REG[7:0], YY:Optimize value setting*
SET_DISPLAY_OFF	0x28	-		↓	0x05	Display Off
- Wait	-		Min. 20ms	↓		
- Host Display Data Transfer	STOP / Continue			LP State / HS State		
(Read each register value for check)						※ If all data is not good,

				↓		re-execute MTP Write
- Wait	-		Min. 50ms	↓		
- Added external 7.5V(typ.) Power Source to MTP_PWR_pin						
- Wait	-		Min. 120ms	↓		
Page select	0xFF	0x01		↓	0x15	CMD2, Page0 is selected.
Reload CMD	0xFB	0x01		↓	0x15	Don't reload MTP
RD_CMDSTATUS	0xFE	Read value		↓	0x06	- Expected return value = '0x02'
MTP_CTRL1	0x3D	0x01		↓		Enable MTP Write (MTP_W[0]='1')
MTP_CTRL3	0x40	0x55		↓	0x15	EPWRITE1 (4040h=0055h)
MTP_CTRL4	0x41	0xAA		↓	0x15	EPWRITE2 (4140h=00AAh)
MTP_CTRL5	0x42	0x66		↓	0x15	EPWRITE3 (4240h=0066h)
- Wait	-		Min. 400ms	↓		
MTP_CTRL2	0x3F	Read value		↓	0x06	- Expected return value = '0x01'
MTP_CTRL1	0x3D	0x00		↓	0x15	Disable MTP Write (MTP_W[0]='0')
- Removed external 7.5V(Typ.) Power Source from TP_PWR_pin				↓		
- Wait	-		Min .150ms	↓		
Page Leave	0xFF	0x00		↓	0x15	CMD1 is selected.
Reload CMD	0xFB	0x01		↓	0x15	Don't reload MTP
RD_CMDSTATUS	0xFE	Read value		↓		- Expected return value = '0x01'
ENTER_SLEEP_MODE	0x10	-		↓	0x15	
- Wait			Min. 100ms	↓		
- Reset Active	RESX = 'Low'			↓		
- Wait	-		Min. 10us	↓		
- Reset Release	RESX = 'High'			↓		
- Wait	-		Min. 150ms	↓		
Page Select	0xFF	0x01		↓	0x15	CMD2, Page0 is selected.
Reload CMD	0xFB	0x01		↓	0x15	Don't reload MTP
RD_CMDSTATUS	0xFE	Read value		↓	0x06	- Expected Return value = '0x02'
MTP_CTRL6	0x43	0x20		↓	0x15	Set Margin Read
(Read each register value for check)				↓		※ If all data is not good, re-execute MTP Write
- Reset Active	RESX = 'Low'			↓		
- Wait	-		Min. 10us	↓		
- Reset Release	RESX = 'High'			↓		
- Wait	-		Min. 20ms	↓		
EXIT_SLEEP_MODE	0x11	-		↓	0x05	Sleep out
- Wait			Min. 120ms	↓		
Page Select	0xFF	0x01		↓	0x15	CMD2, Page0 is selected.
MTP_CTRL2	0x3F	Read value		↓	0x15	- Expected return value = '0x10'
(Read each register value for check)				↓		※ If all data is not good, re-execute MTP Write
Page leave	0xFF	0x00		↓	0x15	CMD1 is selected.
ENTER_SLEEP_MODE	0x10		Min. 100ms	↓	0x05	Sleep in
- Host Display Data Transfer	STOP			LP11 State		Image Write Stop (Send Video Stream

						Packet)
- Wait	-	-	Min. 100ms	↓		
- Reset Active	RESX = 'Low'			LP00 State		
- Wait			Min. 10ms	↓		
- Power Supply AVEE	AVEE OFF			↓		
- Wait	-	-	Min. 0ms	↓		
- Power Supply AVDD	AVDD OFF			↓		
- Wait	-	-	Min. 0ms	↓		
- Power Supply VDDI	VDDI OFF			LP00 State		

9-4-2 Second times MTP Programming sequence



Sequence of each 2Power mode/3Power mode is shown below.
9-4-2-1 2Power(VDDI/VCI) Mode (2nd times MTP Programming)
<< 2 Power Mode >>

Item	Address	Parameter	Delay	MIPI State	Dat a ID	Comment
- Initial Condition	RESX = 'Low'			LP00 State		
- Power Supply VDDI	VDDI On			LP11 State		Logic Power (Typ.1.8V)
- Wait	-		Min. 0ms	↓		Wait until Power Stable
- Power Supply VCI	VCI ON			LP11 State		Analog Power (Typ.2.8V)
- Wait	-		Min. 20ms	↓		Wait until Power Stable
- Reset Release	RESX = 'High'			↓		
- Wait	-		Min. 1ms	↓		
- Reset Active	RESX = 'Low'			↓		
- Wait	-		Min. 10us	↓		
- Reset Release	RESX = 'High'			↓		
- Wait	-		Min. 150ms	↓		
--- Initial Sequence for MIPI Data lane number selection				LP State		Refer to "9-3-3 MIPI Data lane number selection"
Page select	0xFF	0x01		↓	0x15	CMD2, Page0 is selected
Reload CMD	0xFB	0x01		↓	0x15	Don't reload MTP
RD_CMDSTATUS	0xFE	Read value		↓	0x06	- Expected return value = '0x02'
MTP_CTRL2	0x3F	Read value		↓	0x06	- Expected return value = '0x10'
MTP_CTRL2	0x3F	Read value		↓	0x06	- Expected return value = '0x10'
DDB CTRL1	0x23	*user setting*		↓	0x15	*- SID[7:0] MIPI member ID number*
DDB CTRL2	0x24	*user setting*		↓	0x15	*- SID[15:8] MIPI member ID number*
DDB CTRL3	0x25	*user setting*		↓	0x15	*- MID[7:0] Module ID*
DDB CTRL4	0x26	*user setting*		↓	0x15	*- MID[15:8] Module ID*
DDB CTRL5	0x27	*user setting*		↓	0x15	*- RID[7:0] Revision ID*
DDBCTRL6	0x28	*user setting*		↓	0x15	*- RID[15:8] Revision ID*
WID_CTRL1	0x44	*user setting*		↓	0x15	*- This read byte identifies the display module's manufacturer.*
WID_CTRL2	0x45	*user setting*		↓	0x15	*- This read byte is used to track the display module/driver version.*
WID_CTRL3	0x46	*user setting*		↓	0x15	*- This read byte identifies the display module/driver.*
Page Leave	0xFF	0x00		↓	0x15	CMD1 is selected.
Reload CMD	0xFB	0x01		↓	0x15	Don't reload MTP
RD_CMDSTATUS	0xFE	Read value		↓	0x06	- Expected return value = '0x01'
--- Initial Sequence for 2Power Mode				HS State		Refer to "9-3-4 Initial Sequence for 2power mode"
EXIT_SLEEP_MODE	0x11	-		↓	0x05	Sleep out
- Wait	-		Min. 150ms	↓		
SET_DISPLAY_ON	0x29	-		↓	0x05	Display On
-- Host Display Data Transfer	START			↓		Image : Flicker Pattern
Page select	0xFF	0x01		↓	0x15	CMD2, Page0 is selected
Reload CMD	0xFB	0x01		↓	0x15	Don't reload MTP

RD_CMDSTATUS	0xFE	Read value		↓	0x06	- Expected return value = '0x02'
Page Leave	0xFF	0x00		↓	0x15	CMD1 is selected.
Reload CMD	0xFB	0x01		↓	0x15	Don't reload MTP
RD_CMDSTATUS	0xFE	Read value		↓	0x06	- Expected return value = '0x01'
REG CTRL 7	0x11	*0xYY*		↓	0x15	*Set VCOMDC3_REG[7:0], YY:Optimize value setting*
SET_DISPLAY_OFF	0x28	-		↓	0x05	Display Off
- Wait	-		Min. 20ms	↓		
- Host Display Data Transfer	STOP / Continue			LP State / HS State		
(Read each register value for check)						※ If all data is not good, re-execute MTP Write
- Wait	-		Min. 50ms	↓		
- Added external 7.5V(typ.) Power Source to MTP_PWR_pin						
- Wait	-		Min. 120ms	↓		
Page select	0xFF	0x01		↓	0x15	CMD2, Page0 is selected.
Reload CMD	0xFB	0x01		↓	0x15	Don't reload MTP
RD_CMDSTATUS	0xFE	Read value		↓	0x06	- Expected return value = '0x02'
MTP_CTRL1	0x3D	0x01		↓		Enable MTP Write (MTP_W[0]='1')
MTP_CTRL3	0x40	0x55		↓	0x15	EPWRITE1(4040h=0055h)
MTP_CTRL4	0x41	0xAA		↓	0x15	EPWRITE2(4140h=00AAh)
MTP_CTRL5	0x42	0x66		↓	0x15	EPWRITE3(4240h=0066h)
- Wait	-		Min. 400ms	↓		
MTP_CTRL2	0x3F	Read value		↓	0x06	- Expected return value = '0x11'
MTP_CTRL1	0x3D	0x00		↓	0x15	Disable MTP Write (MTP_W[0]='0')
- Removed external 7.5V(Typ.) Power Source from MTP_PWR_pin				↓		
- Wait	-		Min .150ms	↓		
Page Leave	0xFF	0x00		↓	0x15	CMD1 is selected.
Reload CMD	0xFB	0x01		↓	0x15	Don't reload MTP
RD_CMDSTATUS	0xFE	Read value		↓		- Expected return value = '0x01'
ENTER_SLEEP_MODE	0x10	-		↓	0x15	
- Wait			Min. 100ms	↓		
- Reset Active	RESX = 'Low'			↓		
- Wait	-		Min. 10us	↓		
- Reset Release	RESX = 'High'			↓		
- Wait	-		Min. 150ms	↓		
Page Select	0xFF	0x01		↓	0x15	CMD2, Page0 is selected.
Reload CMD	0xFB	0x01		↓	0x15	Don't reload MTP
RD_CMDSTATUS	0xFE	Read value		↓	0x06	- Expected Return value = '0x02'
MTP_CTRL6	0x43	0x20		↓	0x15	Set Margin Read
(Read each register value for check)				↓		※ If all data is not good, re-execute MTP Write
- Reset Active	RESX = 'Low'			↓		
- Wait	-		Min. 10us	↓		
- Reset Release	RESX = 'High'			↓		
- Wait	-		Min. 20ms	↓		
EXIT_SLEEP_MODE	0x11	-		↓	0x05	Sleep out

- Wait			Min. 120ms	↓		
Page Select	0xFF	0x01		↓	0x15	CMD2, Page0 is selected.
MTP_CTRL2	0x3F	Read value		↓	0x15	- Expected return value = '0x30'
(Read each register value for check)				↓		※ If all data is not good, re-execute MTP Write
Page leave	0xFF	0x00		↓	0x15	CMD1 is selected.
ENTER_SLEEP_MODE	0x10		Min. 100ms	↓	0x05	Sleep in
- Host Display Data Transfer	STOP			LP11 State		Image Write (Send Video Stream Packet) Stop
- Wait	-	-	Min. 100ms	↓		
- Reset Active	RESX = 'Low'			LP00 State		
- Wait			Min. 10ms	↓		
- Power Supply VCI	VCI OFF			↓		
- Wait	-	-	Min. 0ms	↓		
- Power Supply VDDI	VDDI OFF			LP00 State		

9-4-2-2 3Power(VDDI/AVDD/AVEE) Mode (2nd times MTP Programming)

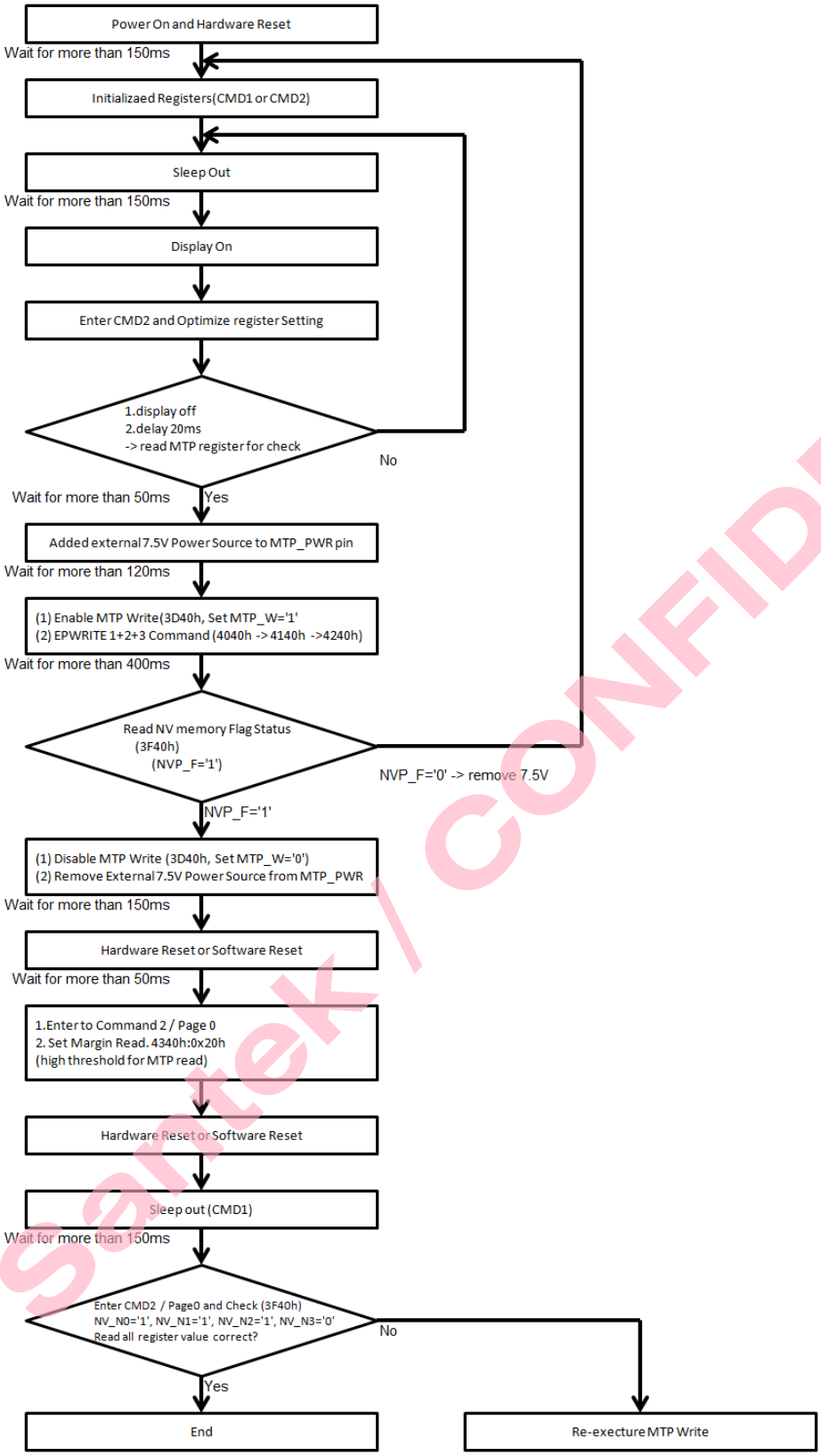
<< 3 Power Mode >>

Item	Address	Parameter	Delay	MIPI State	Data ID	Comment
- Initial Condition	RESX = 'Low'			LP00 State		
- Power Supply VDDI	VDDI ON			↓		Logic Power (Typ.1.8V)
- Wait	-		Min. 0ms	↓		Wait until Power stable
- Power Supply AVDD	AVDD ON			LP11 State		Analog(Posi) Power (Typ.5.0V)
- Wait	-		Min. 0ms	↓		Wait until Power Stable
- Power Supplya AVEE	AVEE ON			↓		Analog(Nega) Power (Typ.-5.0V)
- Wait	-		Min. 20ms	↓		
- Reset Release	RESX = 'High'			↓		
- Wait	-		Min. 1ms	↓		
- Reset Active	RESX = 'Low'			↓		
- Wait	-		Min. 10us	↓		
- Reset Release	RESX = 'High'			↓		
- Wait	-		Min. 150ms	↓		
--- *Initial Sequence for MIPI Data lane number selection*				LP State		Refer to "9-3-3 MIPI Data lane number selection"
Page select	0xFF	0x01		↓	0x15	CMD2, Page0 is selected
Reload CMD	0xFB	0x01		↓	0x15	Don't reload MTP
RD_CMDSTATUS	0xFE	Read value		↓	0x06	- Expected return value = '0x02'
MTP_CTRL2	0x3F	Read value		↓	0x06	- Expected return value = '0x10'
DDB CTRL1	0x23	*user setting*		↓	0x15	*- SID[7:0] MIPI member ID number*
DDB CTRL2	0x24	*user setting*		↓	0x15	*- SID[15:8] MIPI member ID number*
DDB CTRL3	0x25	*user setting*		↓	0x15	*- MID[7:0] Module ID*
DDB CTRL4	0x26	*user setting*		↓	0x15	*- MID[15:8] Module ID*
DDB CTRL5	0x27	*user setting*		↓	0x15	*- RID[7:0] Revision ID*
DDBCTRL6	0x28	*user setting*		↓	0x15	*- RID[15:8] Revision ID*
WID_CTRL1	0x44	*user setting*		↓	0x15	*- This read byte identifies the display module's manufacturer.*
WID_CTRL2	0x45	*user setting*		↓	0x15	*- This read byte is used to track the display module/driver version.*
WID_CTRL3	0x46	*user setting*		↓	0x15	*- This read byte identifies the display module/driver.*
Page Leave	0xFF	0x00		↓	0x15	CMD1 is selected.
Reload CMD	0xFB	0x01		↓	0x15	Don't reload MTP
RD_CMDSTATUS	0xFE	Read value		↓	0x06	- Expected return value = '0x01'
--- *Initial Sequence for 3Power Mode*				HS State		Refer to "9-3-4 Initial Sequence for 3power mode"
EXIT_SLEEP_MODE	0x11	-		↓	0x05	Sleep out
- Wait	-		Min. 150ms	↓		
SET_DISPLAY_ON	0x29	-		↓	0x05	Display On
-- Host Display Data Transfer	START			↓		Image : Flicker Pattern
Page select	0xFF	0x01		↓	0x15	CMD2, Page0 is selected
Reload CMD	0xFB	0x01		↓	0x15	Don't reload MTP
RD_CMDSTATUS	0xFE	Read value		↓	0x06	- Expected return value =

						'0x02'
Page Leave	0xFF	0x00		↓	0x15	CMD1 is selected.
Reload CMD	0xFB	0x01		↓	0x15	Don't reload MTP
RD_CMDSTATUS	0xFE	Read value		↓	0x06	- Expected return value = '0x01'
REG CTRL 7	0x11	*0xYY*		↓	0x15	*Set VCOMDC3_REG[7:0], YY:Optimize value setting*
SET_DISPLAY_OFF	0x28	-		↓	0x05	Display Off
- Wait	-		Min. 20ms	↓		
- Host Display Data Transfer	STOP / Continue			LP State / HS State		
(Read each register value for check)						※ If all data is not good, re-execute MTP Write
- Wait	-		Min. 50ms	↓		
- Added external 7.5V(typ.) Power Source to MTP_PWR_pin						
- Wait	-		Min. 120ms	↓		
Page select	0xFF	0x01		↓	0x15	CMD2, Page0 is selected.
Reload CMD	0xFB	0x01		↓	0x15	Don't reload MTP
RD_CMDSTATUS	0xFE	Read value		↓	0x06	- Expected return value = '0x02'
MTP_CTRL1	0x3D	0x01		↓		Enable MTP Write (MTP_W[0]='1')
MTP_CTRL3	0x40	0x55		↓	0x15	EPWRITE1(4040h=0055h)
MTP_CTRL4	0x41	0xAA		↓	0x15	EPWRITE2(4140h=00AAh)
MTP_CTRL5	0x42	0x66		↓	0x15	EPWRITE3(4240h=0066h)
- Wait	-		Min. 400ms	↓		
MTP_CTRL2	0x3F	Read value		↓	0x06	- Expected return value = '0x11'
MTP_CTRL1	0x3D	0x00		↓	0x15	Disable MTP Write (MTP_W[0]='0')
- Removed external 7.5V(Typ.) Power Source from MTP_PWR_pin				↓		
- Wait	-		Min .150ms	↓		
Page Leave	0xFF	0x00		↓	0x15	CMD1 is selected.
Reload CMD	0xFB	0x01		↓	0x15	Don't reload MTP
RD_CMDSTATUS	0xFE	Read value		↓		- Expected return value = '0x01'
ENTER_SLEEP_MODE	0x10	-		↓	0x15	
- Wait			Min. 100ms	↓		
- Reset Active	RESX = 'Low'			↓		
- Wait	-		Min. 10us	↓		
- Reset Release	RESX = 'High'			↓		
- Wait	-		Min. 150ms	↓		
Page Select	0xFF	0x01		↓	0x15	CMD2, Page0 is selected.
Reload CMD	0xFB	0x01		↓	0x15	Don't reload MTP
RD_CMDSTATUS	0xFE	Read value		↓	0x06	- Expected Return value = '0x02'
MTP_CTRL6	0x43	0x20		↓	0x15	Set Margin Read
(Read each register value for check)				↓		※ If all data is not good, re-execute MTP Write
- Reset Active	RESX = 'Low'			↓		
- Wait	-		Min. 10us	↓		
- Reset Release	RESX = 'High'			↓		
- Wait	-		Min. 20ms	↓		
EXIT_SLEEP_MODE	0x11	-		↓	0x05	Sleep out
- Wait			Min. 120ms	↓		

Page Select	0xFF	0x01		↓	0x15	CMD2, Page0 is selected.
MTP_CTRL2	0x3F	Read value		↓	0x15	- Expected return value = '0x30'
(Read each register value for check)				↓		※ If all data is not good, re-execute MTP Write
Page leave	0xFF	0x00		↓	0x15	CMD1 is selected.
ENTER_SLEEP_MODE	0x10		Min. 100ms	↓	0x05	Sleep in
- Host Display Data Transfer	STOP			LP11 State		Image Write (Send Video Stream Packet) Stop
- Wait	-	-	Min. 100ms	↓		
- Reset Active	RESX = 'Low'			LP00 State		
- Wait			Min. 10ms	↓		
- Power Supply AVEE	AVEE OFF			↓		
- Wait	-	-	Min. 0ms	↓		
- Power Supply AVDD	AVDD OFF			↓		
- Wait	-	-	Min. 0ms	↓		
- Power Supply VDDI	VDDI OFF			LP00 State		

9-4-3 third times MTP Programming sequence



Sequence of each 2Power mode/3Power mode is shown below.
9-4-3-1 2Power(VDDI/VCI) Mode (3rd times MTP Programming)
<< 2 Power Mode >>

Item	Address	Parameter	Delay	MIPI State	Data ID	Comment
- Power Supply VDDI	VDDI ON			↓		Logic Power (Typ.1.8V)
- Wait	-		Min. 0ms	↓		Wait until Power stable
- Power Supply VCI	VCI ON			LP11 State		Analog Power (Typ.2.8V)
- Wait	-		Min. 20ms	↓		Wait until Power Stable
- Reset Release	RESX = 'High'			↓		
- Wait	-		Min. 1ms	↓		
- Reset Active	RESX = 'Low'			↓		
- Wait	-		Min. 10us	↓		
- Reset Release	RESX = 'High'			↓		
- Wait	-		Min. 150ms	↓		
--- *Initial Sequence for MIPI Data lane number selection*				LP State		Refer to "MIPI Data lane number selection"
Page select	0xFF	0x01		↓	0x15	CMD2, Page0 is selected
Reload CMD	0xFB	0x01		↓	0x15	Don't reload MTP
RD_CMDSTATUS	0xFE	Read value		↓	0x06	- Expected return value = '0x02'
MTP_CTRL2	0x3F	Read value		↓	0x06	- Expected return value = '0x30'
DDB CTRL1	0x23	*user setting*		↓	0x15	*- SID[7:0] MIPI member ID number*
DDB CTRL2	0x24	*user setting*		↓	0x15	*- SID[15:8] MIPI member ID number*
DDB CTRL3	0x25	*user setting*		↓	0x15	*- MID[7:0] Module ID*
DDB CTRL4	0x26	*user setting*		↓	0x15	*- MID[15:8] Module ID*
DDB CTRL5	0x27	*user setting*		↓	0x15	*- RID[7:0] Revision ID*
DDBCTRL6	0x28	*user setting*		↓	0x15	*- RID[15:8] Revision ID*
WID_CTRL1	0x44	*user setting*		↓	0x15	*- This read byte identifies the display module's manufacturer.*
WID_CTRL2	0x45	*user setting*		↓	0x15	*- This read byte is used to track the display module/driver version.*
WID_CTRL3	0x46	*user setting*		↓	0x15	*- This read byte identifies the display module/driver.*
Page Leave	0xFF	0x00		↓	0x15	CMD1 is selected.
Reload CMD	0xFB	0x01		↓	0x15	Don't reload MTP
RD_CMDSTATUS	0xFE	Read value		↓	0x06	- Expected return value = '0x01'
--- *Initial Sequence for 2Power Mode*				HS State		Refer to "9-3-4 Initial Sequence for 2power mode"
EXIT_SLEEP_MODE	0x11	-		↓	0x05	Sleep out
- Wait	-		Min. 150ms	↓		
SET_DISPLAY_ON	0x29	-		↓	0x05	Display On
-- Host Display Data Transfer	START			↓		Image : Flicker Pattern
Page select	0xFF	0x01		↓	0x15	CMD2, Page0 is selected
Reload CMD	0xFB	0x01		↓	0x15	Don't reload MTP

RD_CMDSTATUS	0xFE	Read value		↓	0x06	- Expected return value = '0x02'
Page Leave	0xFF	0x00		↓	0x15	CMD1 is selected.
Reload CMD1	0xFB	0x01		↓	0x15	Don't reload MTP
RD_CMDSTATUS	0xFE	Read value		↓	0x06	- Expected return value = '0x01'
REG CTRL 7	0x11	*0xYY*		↓	0x15	*Set VCOMDC3_REG[7:0], YY:Optimize value setting*
SET_DISPLAY_OFF	0x28	-		↓	0x05	Display Off
- Wait	-		Min. 20ms	↓		
- Host Display Data Transfer	STOP / Continue			LP State / HS State		
(Read each register value for check)						※ If all data is not good, re-execute MTP Write
- Wait	-		Min. 50ms	↓		
- Added external 7.5V(typ.) Power Source to MTP_PWR_pin						
- Wait	-		Min. 120ms	↓		
Page select	0xFF	0x01		↓	0x15	CMD2, Page0 is selected.
Reload CMD	0xFB	0x01		↓	0x15	Don't reload MTP
RD_CMDSTATUS	0xFE	Read value		↓	0x06	- Expected return value = '0x02'
MTP_CTRL1	0x3D	0x01		↓		Enable MTP Write (MTP_W[0]='1')
MTP_CTRL3	0x40	0x55		↓	0x15	EPWRITE1(4040h=0055h)
MTP_CTRL4	0x41	0xAA		↓	0x15	EPWRITE2(4140h=00AAh)
MTP_CTRL5	0x42	0x66		↓	0x15	EPWRITE3(4240h=0066h)
- Wait	-		Min. 400ms	↓		
MTP_CTRL2	0x3F	Read value		↓	0x06	- Expected return value = '0x31'
MTP_CTRL1	0x3D	0x00		↓	0x15	Disable MTP Write (MTP_W[0]='0')
- Removed external 7.5V(Typ.) Power Source from MTP_PWR_pin				↓		
- Wait	-		Min .150ms	↓		
Page Leave	0xFF	0x00		↓	0x15	CMD1 is selected.
Reload CMD	0xFB	0x01		↓	0x15	Don't reload MTP
RD_CMDSTATUS	0xFE	Read value		↓	0x06	- Expected return value = '0x01'
ENTER_SLEEP_MODE	0x10	-		↓	0x15	
- Wait			Min. 100ms	↓		
- Reset Active	RESX = 'Low'			↓		
- Wait	-		Min. 10us	↓		
- Reset Release	RESX = 'High'			↓		
- Wait	-		Min. 150ms	↓		
Page Select	0xFF	0x01		↓	0x15	CMD2, Page0 is selected.
Reload CMD	0xFB	0x01		↓	0x15	Don't reload MTP
RD_CMDSTATUS	0xFE	Read value		↓	0x06	- Expected Return value = '0x02'
MTP_CTRL6	0x43	0x20		↓	0x15	Set Margin Read
(Read each register value for check)				↓		※ If all data is not good, re-execute MTP Write
- Reset Active	RESX = 'Low'			↓		
- Wait	-		Min. 10us	↓		
- Reset Release	RESX = 'High'			↓		
- Wait	-		Min. 20ms	↓		
EXIT_SLEEP_MODE	0x11	-		↓	0x05	Sleep out

- Wait			Min. 120ms	↓		
Page Select	0xFF	0x01		↓	0x15	CMD2, Page0 is selected.
MTP_CTRL2	0x3F	Read value		↓	0x15	- Expected return value = '0x70'
(Read each register value for check)				↓		※ If all data is not good, re-execute MTP Write
Page leave	0xFF	0x00		↓	0x15	CMD1 is selected.
ENTER_SLEEP_MODE	0x10		Min. 100ms	↓	0x05	Sleep in
- Host Display Data Transfer	STOP			LP11 State		Image Write (Send Video Stream Packet) Stop
- Wait	-	-	Min. 100ms	↓		
- Reset Active	RESX = 'Low'			LP00 State		
- Wait			Min. 10ms	↓		
- Power Supply VCI	VCI OFF			↓		
- Wait	-	-	Min. 0ms	↓		
- Power Supply VDDI	VDDI OFF			LP00 State		

9-4-3-2 3Power(VDDI/AVDD/AVEE) Mode (3rd times MTP Programming)

<< 3 Power Mode >>

Item	Address	Parameter	Delay	MIPI State	Data ID	Comment
- Initial Condition	RESX = 'Low'			LP00 State		
- Power Supply VDDI	VDDI ON			↓		Logic Power (Typ.1.8V)
- Wait	-		Min. 0ms	↓		Wait until Power stable
- Power Supply AVDD	AVDD ON			LP11 State		Analog(Posi) Power (Typ.5.0V)
- Wait	-		Min. 0ms	↓		Wait until Power Stable
- Power Supplya AVEE	AVEE ON			↓		Analog(Nega) Power (Typ.-5.0V)
- Wait	-		Min. 20ms	↓		
- Reset Release	RESX = 'High'			↓		
- Wait	-		Min. 1ms	↓		
- Reset Active	RESX = 'Low'			↓		
- Wait	-		Min. 10us	↓		
- Reset Release	RESX = 'High'			↓		
- Wait	-		Min. 150ms	↓		
--- Initial Sequence for MIPI Data lane number selection				LP State		Refer to "9-3-3 MIPI Data lane number selection"
Page select	0xFF	0x01		↓	0x15	CMD2, Page0 is selected
Reload CMD	0xFB	0x01		↓	0x15	Don't reload MTP
RD_CMDSTATUS	0xFE	Read value		↓	0x06	- Expected return value = '0x02'
MTP_CTRL2	0x3F	Read value		↓	0x06	- Expected return value = '0x30'
DDB CTRL1	0x23	*user setting*		↓	0x15	*- SID[7:0] MIPI member ID number*
DDB CTRL2	0x24	*user setting*		↓	0x15	*- SID[15:8] MIPI menber ID number*
DDB CTRL3	0x25	*user setting*		↓	0x15	*- MID[7:0] Module ID*
DDB CTRL4	0x26	*user setting*		↓	0x15	*- MID[15:8] Module ID*
DDB CTRL5	0x27	*user setting*		↓	0x15	*- RID[7:0] Revision ID*
DDBCTRL6	0x28	*user setting*		↓	0x15	*- RID[15:8] Revision ID*
WID_CTRL1	0x44	*user setting*		↓	0x15	*- This read byte identifies the display module's manufacturer.*
WID_CTRL2	0x45	*user setting*		↓	0x15	*- This read byte is used to track the display module/driver version.*
WID_CTRL3	0x46	*user setting*		↓	0x15	*- This read byte identifies the display module/dirver.*
Page Leave	0xFF	0x00		↓	0x15	CMD1 is selected.
Reload CMD	0xFB	0x01		↓	0x15	Don't reload MTP
RD_CMDSTATUS	0xFE	Read value		↓	0x06	- Expected return value = '0x01'
--- Initial Sequence for 3Power Mode				HS State		Refer to "9-3-3 Initial Sequence for 3power mode"
EXIT_SLEEP_MODE	0x11	-		↓	0x05	Sleep out
- Wait	-		Min. 150ms	↓		
SET_DISPLAY_ON	0x29	-		↓	0x05	Display On
-- Host Display Data Transfer	START			↓		Image : Flicker Pattern
Page select	0xFF	0x01		↓	0x15	CMD2, Page0 is selected
Reload CMD	0xFB	0x01		↓	0x15	Don't reload MTP
RD_CMDSTATUS	0xFE	Read value		↓	0x06	- Expected return value =

						'0x02'
Page Leave	0xFF	0x00		↓	0x15	CMD1 is selected.
Reload CMD	0xFB	0x01		↓	0x15	Don't reload MTP
RD_CMDSTATUS	0xFE	Read value		↓	0x06	- Expected return value = '0x01'
REG CTRL 7	0x11	*0xYY*		↓	0x15	*Set VCOMDC3_REG[7:0], YY:Optimize value setting*
SET_DISPLAY_OFF	0x28	-		↓	0x05	Display Off
- Wait	-		Min. 20ms	↓		
- Host Display Data Transfer	STOP / Continue			LP State / HS State		
(Read each register value for check)						※ If all data is not good, re-execute MTP Write
- Wait	-		Min. 50ms	↓		
- Added external 7.5V(typ.) Power Source to MTP_PWR_pin						
- Wait	-		Min. 120ms	↓		
Page select	0xFF	0x01		↓	0x15	CMD2, Page0 is selected.
Reload CMD	0xFB	0x01		↓	0x15	Don't reload MTP
RD_CMDSTATUS	0xFE	Read value		↓	0x06	- Expected return value = '0x02'
MTP_CTRL1	0x3D	0x01		↓		Enable MTP Write (MTP_W[0]='1')
MTP_CTRL3	0x40	0x55		↓	0x15	EPWRITE1(4040h=0055h)
MTP_CTRL4	0x41	0xAA		↓	0x15	EPWRITE2(4140h=00AAh)
MTP_CTRL5	0x42	0x66		↓	0x15	EPWRITE3(4240h=0066h)
- Wait	-		Min. 400ms	↓		
MTP_CTRL2	0x3F	Read value		↓	0x06	- Expected return value = '0x31'
MTP_CTRL1	0x3D	0x00		↓	0x15	Disable MTP Write (MTP_W[0]='0')
- Removed external 7.5V(Typ.) Power Source from MTP_PWR_pin				↓		
- Wait	-		Min .150ms	↓		
Page Leave	0xFF	0x00		↓	0x15	CMD1 is selected.
Reload CMD	0xFB	0x01		↓	0x15	Don't reload MTP
RD_CMDSTATUS	0xFE	Read value		↓		- Expected return value = '0x01'
ENTER_SLEEP_MODE	0x10	-		↓	0x15	
- Wait			Min. 100ms	↓		
- Reset Active	RESX = 'Low'			↓		
- Wait	-		Min. 10us	↓		
- Reset Release	RESX = 'High'			↓		
- Wait	-		Min. 150ms	↓		
Page Select	0xFF	0x01		↓	0x15	CMD2, Page0 is selected.
Reload CMD	0xFB	0x01		↓	0x15	Don't reload MTP
RD_CMDSTATUS	0xFE	Read value		↓	0x06	- Expected Return value = '0x02'
MTP_CTRL6	0x43	0x20		↓	0x15	Set Margin Read
(Read each register value for check)				↓		※ If all data is not good, re-execute MTP Write
- Reset Active	RESX = 'Low'			↓		
- Wait	-		Min. 10us	↓		
- Reset Release	RESX = 'High'			↓		
- Wait	-		Min. 20ms	↓		
EXIT_SLEEP_MODE	0x11	-		↓	0x05	Sleep out
- Wait			Min. 120ms	↓		

Page Select	0xFF	0x01		↓	0x15	CMD2, Page0 is selected.
MTP_CTRL2	0x3F	Read value		↓	0x15	- Expected return value = '0x70'
(Read each register value for check)				↓		※ If all data is not good, re-execute MTP Write
Page leave	0xFF	0x00		↓	0x15	CMD1 is selected.
ENTER_SLEEP_MODE	0x10		Min. 100ms	↓	0x05	Sleep in
- Host Display Data Transfer	STOP			LP11 State		Image Write (Send Video Stream Packet) Stop
- Wait	-	-	Min. 100ms	↓		
- Reset Active	RESX = 'Low'			LP00 State		
- Wait			Min. 10ms	↓		
- Power Supply AVEE	AVEE OFF			↓		
- Wait	-	-	Min. 0ms	↓		
- Power Supply AVDD	AVDD OFF			↓		
- Wait	-	-	Min. 0ms	↓		
- Power Supply VDDI	VDDI OFF			LP00 State		

9-5 Gamma Table

Gamma setting value which shows the “Gamma2.2” characteristic in the light source”DL65” is shown below.

	Item	Address	Gamma 2.2
1	Page Select CMD2,Page0	0xFF	0x01
2	Don't reload MTP	0xFB	0x01
3	Gamma R+	0x75	0x00
4		0x76	0x5F
5		0x77	0x00
6		0x78	0x97
7		0x79	0x00
8		0x7A	0xA1
9		0x7B	0x00
10		0x7C	0xB8
11		0x7D	0x00
12		0x7E	0xCC
13		0x7F	0x00
14		0x80	0xE2
15		0x81	0x00
16		0x82	0xEC
17		0x83	0x00
18		0x84	0xF9
19		0x85	0x01
20		0x86	0x08
21		0x87	0x01
22		0x88	0x2F
23		0x89	0x01
24		0x8A	0x50
25		0x8B	0x01
26		0x8C	0x3E
27		0x8D	0x01
28		0x8E	0xB6
29		0x8F	0x01
30		0x90	0xFD
31		0x91	0x02
32		0x92	0x2E
33		0x93	0x02
34		0x94	0x2E
35		0x95	0x02
36		0x96	0x5E
37		0x97	0x02
38		0x98	0x94
39		0x99	0x02
40		0x9A	0xB4
41		0x9B	0x02
42		0x9C	0xDB
43		0x9D	0x02
44		0x9E	0xFD
45		0x9F	0x03
46		0xA0	0x24
47		0xA1	
48		0xA2	0x03
49		0xA3	0x30
50		0xA4	0x03
51		0xA5	0x3C
52		0xA6	0x03
53		0xA7	0x5B
54		0xA8	
55		0xA9	0x03
56		0xAA	0x80
57		0xAB	0x03
58		0xAC	0xA3
59		0xAD	0x03
60		0xAE	0xB1
61		0xAF	0x03
62		0xB0	0xBE
63		0xB1	0x03
64		0xB2	0xBD
65	Gamma R-	0xB3	0x00
66		0xB4	0xD9
67		0xB5	0x01
68		0xB6	0x0D
69		0xB7	0x01
70		0xB8	0x13
71		0xB9	0x01
72		0xBA	0x26
73		0xBB	0x01
74		0xBC	0x3A
75		0xBD	0x01
76		0xBE	0x4F
77		0xBF	0x01
78		0xC0	0x5A
79		0xC1	0x01
80		0xC2	0x66
81		0xC3	0x01
82		0xC4	0x6B
83		0xC5	0x01
84		0xC6	0x97
85		0xC7	0x01
86		0xC8	0xB1
87		0xC9	0x01
88		0xCA	0xE8
89		0xCB	0x02
90		0xCC	0x0C
91		0xCD	0x02
92		0xCE	0x48
93		0xCF	0x02
94		0xD0	0x7E
95		0xD1	0x02
96		0xD2	0x7E

	Item	Address	Gamma 2.2
97		0xD3	0x02
98		0xD4	0xAE
99		0xD5	0x02
100		0xD6	0xE4
101		0xD7	0x03
102		0xD8	0x03
103		0xD9	0x03
104		0xDA	0x33
105		0xDB	0x03
106		0xDC	0x57
107		0xDD	0x03
108		0xDE	0x83
109		0xDF	0x03
110		0xE0	0x8D
111		0xE1	0x03
112		0xE2	0x99
113		0xE3	0x03
114		0xE4	0xB7
115		0xE5	0x03
116		0xE6	0xCF
117		0xE7	0x03
118		0xE8	0xD8
119		0xE9	0x03
120		0xEA	0xE6
121		0xEB	0x03
122		0xEC	0xE8
123		0xED	0x03
124		0xEE	0xEA
125	Gamma G+	0xEF	0x00
126		0xF0	0x2D
127		0xF1	0x00
128		0xF2	0x71
129		0xF3	0x00
130		0xF4	0x87
131		0xF5	0x00
132		0xF6	0xA1
133		0xF7	0x00
134		0xF8	0xB2
135		0xF9	0x00
136		0xFA	0xCB
137		0xFB	0x01
138	Page Select CMD1	0xFF	0x00
139	Don't reload MTP	0xFB	0x01
140	Page Select CMD2,Page1	0xFF	0x02
141	Don't reload MTP	0xFB	0x01
142		0x00	0x00
143		0x01	0xD7
144		0x02	0x00

	Item	Address	Gamma 2.2
145		0x03	0xE6
146		0x04	0x00
147		0x05	0xF9
148		0x06	0x01
149		0x07	0x2C
150		0x08	0x01
151		0x09	0x4F
152		0x0A	0x01
153		0x0B	0x86
154		0x0C	0x01
155		0x0D	0xB3
156		0x0E	0x01
157		0x0F	0xFC
158		0x10	0x02
159		0x11	0x2E
160		0x12	0x02
161		0x13	0x2E
162		0x14	0x02
163		0x15	0x5D
164		0x16	0x02
165		0x17	0x92
166		0x18	0x02
167		0x19	0xB2
168		0x1A	0x02
169		0x1B	0xDC
170		0x1C	0x02
171		0x1D	0xFF
172		0x1E	0x03
173		0x1F	0x27
174		0x20	0x03
175		0x21	0x3B
176		0x22	0x03
177		0x23	0x45
178		0x24	0x03
179		0x25	0x63
180		0x26	0x03
181		0x27	0x77
182		0x28	0x03
183		0x29	0x95
184		0x2A	0x03
185		0x2B	0x9E
186		0x2C	
187		0x2D	0x03
188		0x2E	
189		0x2F	0xA4
190		0x30	0x03
191		0x31	0xBC
192	Gamma G-	0x32	0x00

	Item	Address	Gamma 2.2
193		0x33	0xB2
194		0x34	0x00
195		0x35	0xF1
196		0x36	0x00
197		0x37	0xFC
198		0x38	0x01
199		0x39	0x13
200		0x3A	0x01
201		0x3B	0x21
202		0x3C	
203		0x3D	0x01
204		0x3E	
205		0x3F	0x37
206		0x40	0x01
207		0x41	0x44
208		0x42	0x01
209		0x43	0x51
210		0x44	0x01
211		0x45	0x65
212		0x46	0x01
213		0x47	0x8A
214		0x48	0x01
215		0x49	0xA8
216		0x4A	0x01
217		0x4B	0xE2
218		0x4C	0x02
219		0x4D	0x0B
220		0x4E	0x02
221		0x4F	0x48
222		0x50	0x02
223		0x51	0x7E
224		0x52	0x02
225		0x53	0x7E
226		0x54	0x02
227		0x55	0xAD
228		0x56	0x02
229		0x57	
230		0x58	0xE4
231		0x59	0x03
232		0x5A	0x06
233		0x5B	0x03
234		0x5C	0x35
235		0x5D	0x03
236		0x5E	0x59
237		0x5F	0x03
238		0x60	0x80
239		0x61	0x03
240		0x62	0x93

	Item	Address	Gamma 2.2
241		0x63	0x03
242		0x64	0xA1
243		0x65	0x03
244		0x66	0xC0
245		0x67	0x03
246		0x68	0xD4
247		0x69	0x03
248		0x6A	0xDD
249		0x6B	0x03
250		0x6C	0xE3
251		0x6D	0x03
252		0x6E	0xE7
253		0x6F	0x03
254		0x70	0xEA
255	Gamma B+	0x71	0x00
256		0x72	0x5F
257		0x73	0x00
258		0x74	0x97
259		0x75	0x00
260		0x76	0xA1
261		0x77	0x00
262		0x78	0xB6
263		0x79	0x00
264		0x7A	0xC6
265		0x7B	0x00
266		0x7C	0xD9
267		0x7D	0x00
268		0x7E	0xE2
269		0x7F	0x00
270		0x80	0xF1
271		0x81	0x00
272		0x82	0xFD
273		0x83	0x01
274		0x84	0x26
275		0x85	0x01
276		0x86	0x45
277		0x87	0x01
278		0x88	0x83
279		0x89	0x01
280		0x8A	0xAF
281		0x8B	0x01
282		0x8C	0xF7
283		0x8D	0x02
284		0x8E	0x21
285		0x8F	0x02
286		0x90	0x21
287		0x91	0x02
288		0x92	0x5A

	Item	Address	Gamma 2.2
289		0x93	0x02
290		0x94	0x90
291		0x95	0x02
292		0x96	0xB1
293		0x97	0x02
294		0x98	0xDB
295		0x99	0x02
296		0x9A	0xF7
297		0x9B	0x03
298		0x9C	0x1E
299		0x9D	0x03
300		0x9E	0x29
301		0x9F	0x03
302		0xA0	0x37
303		0xA1	
304		0xA2	0x03
305		0xA3	0x56
306		0xA4	0x03
307		0xA5	0x79
308		0xA6	0x03
309		0xA7	0x99
310		0xA8	
311		0xA9	0x03
312		0xAA	0xA7
313		0xAB	0x03
314		0xAC	0xB9
315		0xAD	0x03
316		0xAE	0xBD
317	Gamma B-	0xAF	0x00
318		0xB0	0xD9
319		0xB1	0x01
320		0xB2	0x0C
321		0xB3	0x01
322		0xB4	0x13
323		0xB5	0x01
324		0xB6	0x26
325		0xB7	0x01
326		0xB8	0x33
327		0xB9	0x01
328		0xBA	0x45
329		0xBB	0x01
330		0xBC	0x50
331		0xBD	0x01
332		0xBE	0x5D
333		0xBF	0x01
334		0xC0	0x69
335		0xC1	0x01
336		0xC2	0x8E

	Item	Address	Gamma 2.2
337		0xC3	0x01
338		0xC4	0xA8
339		0xC5	0x01
340		0xC6	0xDC
341		0xC7	0x02
342		0xC8	0x04
343		0xC9	0x02
344		0xCA	0x43
345		0xCB	0x02
346		0xCC	0x87
347		0xCD	0x02
348		0xCE	0x87
349		0xCF	0x02
350		0xD0	0xAA
351		0xD1	0x02
352		0xD2	0xE4
353		0xD3	0x03
354		0xD4	0x05
355		0xD5	0x03
356		0xD6	0x2E
357		0xD7	0x03
358		0xD8	0x51
359		0xD9	0x03
360		0xDA	0x76
361		0xDB	0x03
362		0xDC	0x83
363		0xDD	0x03
364		0xDE	0x8F
365		0xDF	0x03
366		0xE0	0xB2
367		0xE1	0x03
368		0xE2	0xDA
369		0xE3	0x03
370		0xE4	0xE4
371		0xE5	0x03
372		0xE6	0xE6
373		0xE7	0x03
374		0xE8	0xE8
375		0xE9	0x03
376		0xEA	0xEA
377	Page select (CMD1)	0xFF	0x00
378		0xFB	0x01

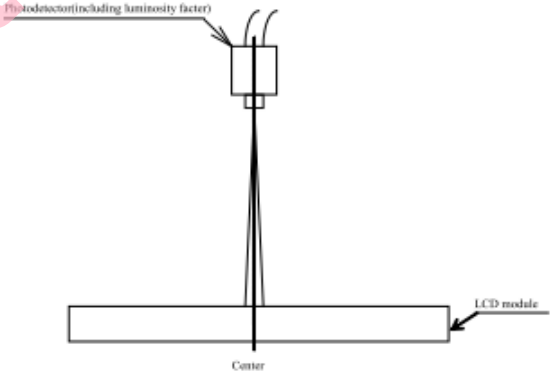
10. Optical Characteristics

Ta=25℃

Item		Symbol	Condition	Min	Typ.	Max.	Unit	Remark
View Angles		Θ11	CR≧10	70	80	-	Degree	Note10-1
		Θ12		70	80	-		
		Θ21		70	80	-		
		Θ22		70	80	-		
Contrast Ratio		CR	θ=0° Center	500	1000	-		Note 10-1 Note 10-2
Response Time		TON	25℃	-	21	35	ms	Note 10-3
		TOFF						
Chromaticity	WHITE	x	θ=0°	0.264	0.294	0.324		
		y		0.305	0.335	0.365		
	RED	x		0.620	0.650	0.680		
		y		0.298	0.328	0.358		
	GREEN	x		0.288	0.318	0.348		
		y		0.576	0.606	0.636		
	BLUE	x		0.120	0.150	0.180		
		y		0.035	0.065	0.095		
Uniformity		U		80	85	-	%	Note 10-5
NTSC		S		-	70	-	%	
Luminance		L	Center	550	650	-	cd/m^2	Note 10-4

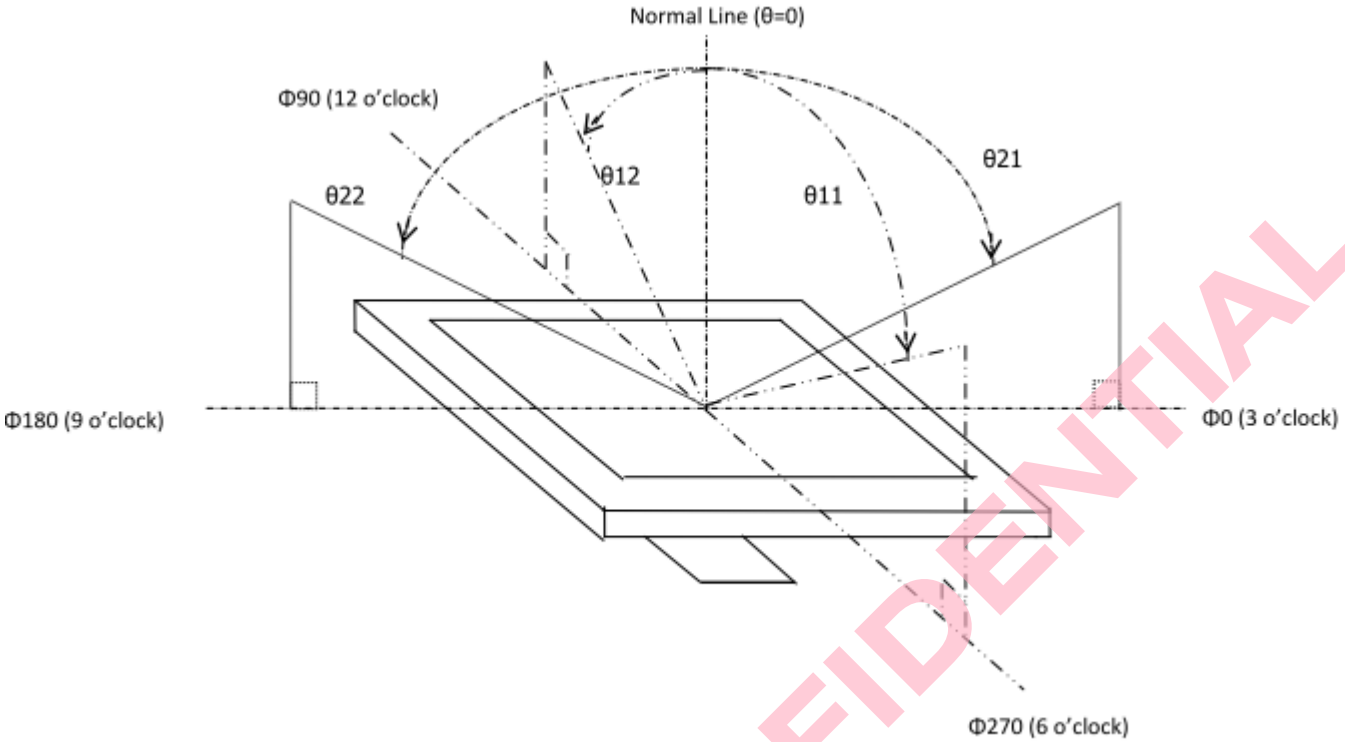
*The measuring method of the optical characteristics is shown by the following figure.

*A measurement device is TOPCON luminance meter SR-3. (Measurement angle: 1 degree.)



Measuring method for optical characteristics

Note 10-1: Contrast / Viewing angle is defined as follows.



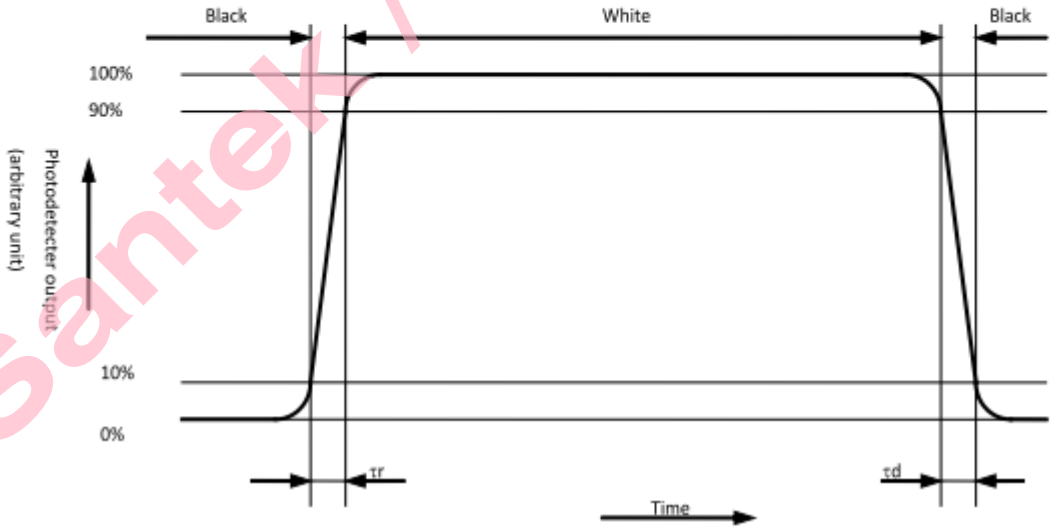
Note 10-2: Definition of contrast ratio:

The contrast ratio is defined as the follows:

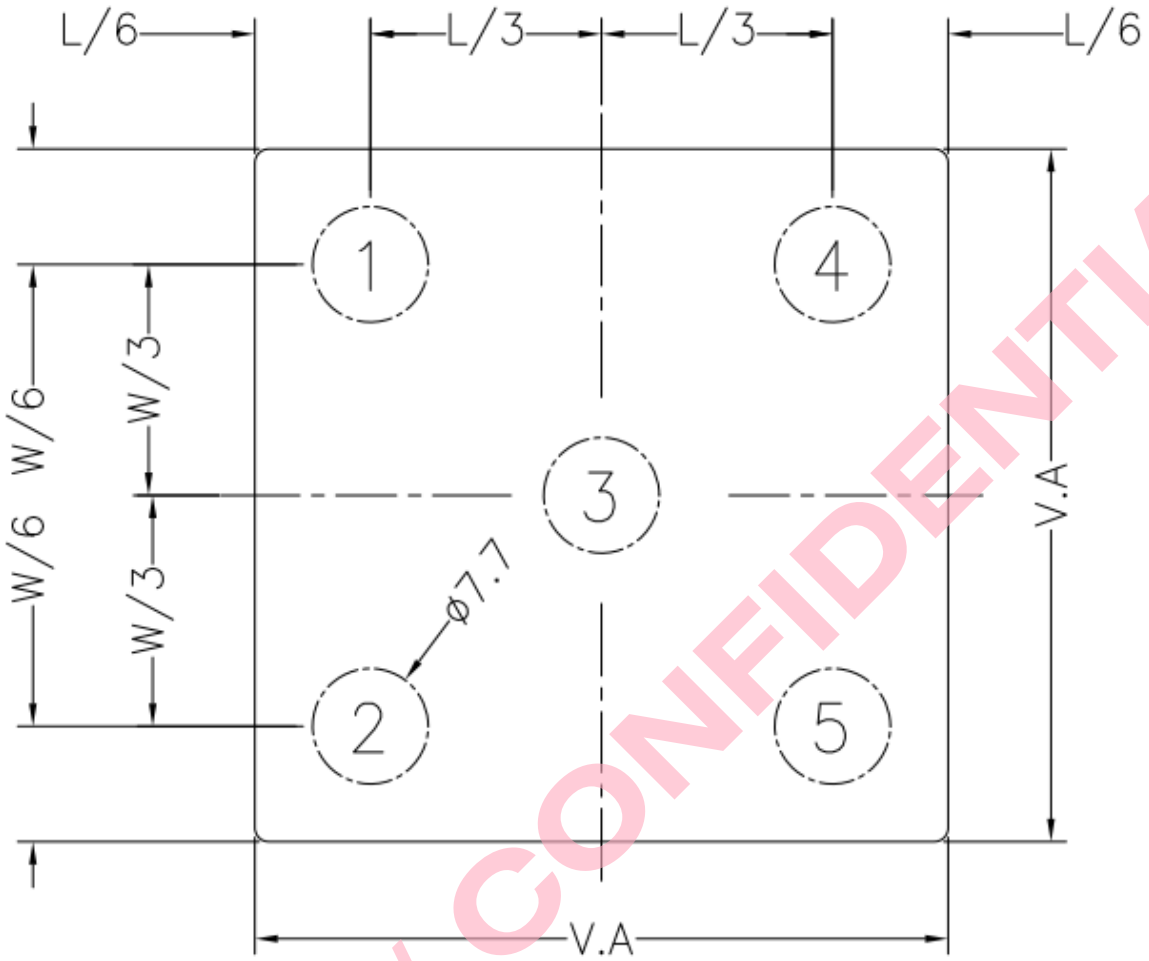
$$\text{Contrast ratio (CR)} = \frac{\text{Luminance (brightness) with all pixels white}}{\text{Luminance (brightness) with all pixels black}}$$

Note 10-3: Definition of response time:

The response time is defined as the following figure and shall be measured by switching the input signal for "black" and "white"



Note 10-4 Measurement Position and Point

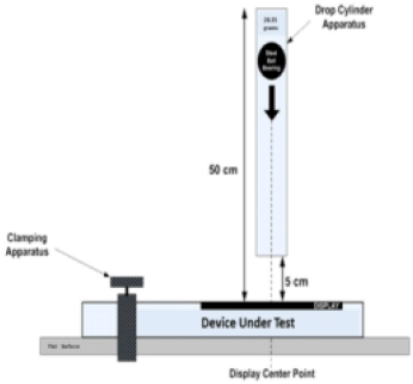


Note 10-5 Uniformity

(Min brightness / Max brightness) x 100%

11. Environmental / Reliability Tests

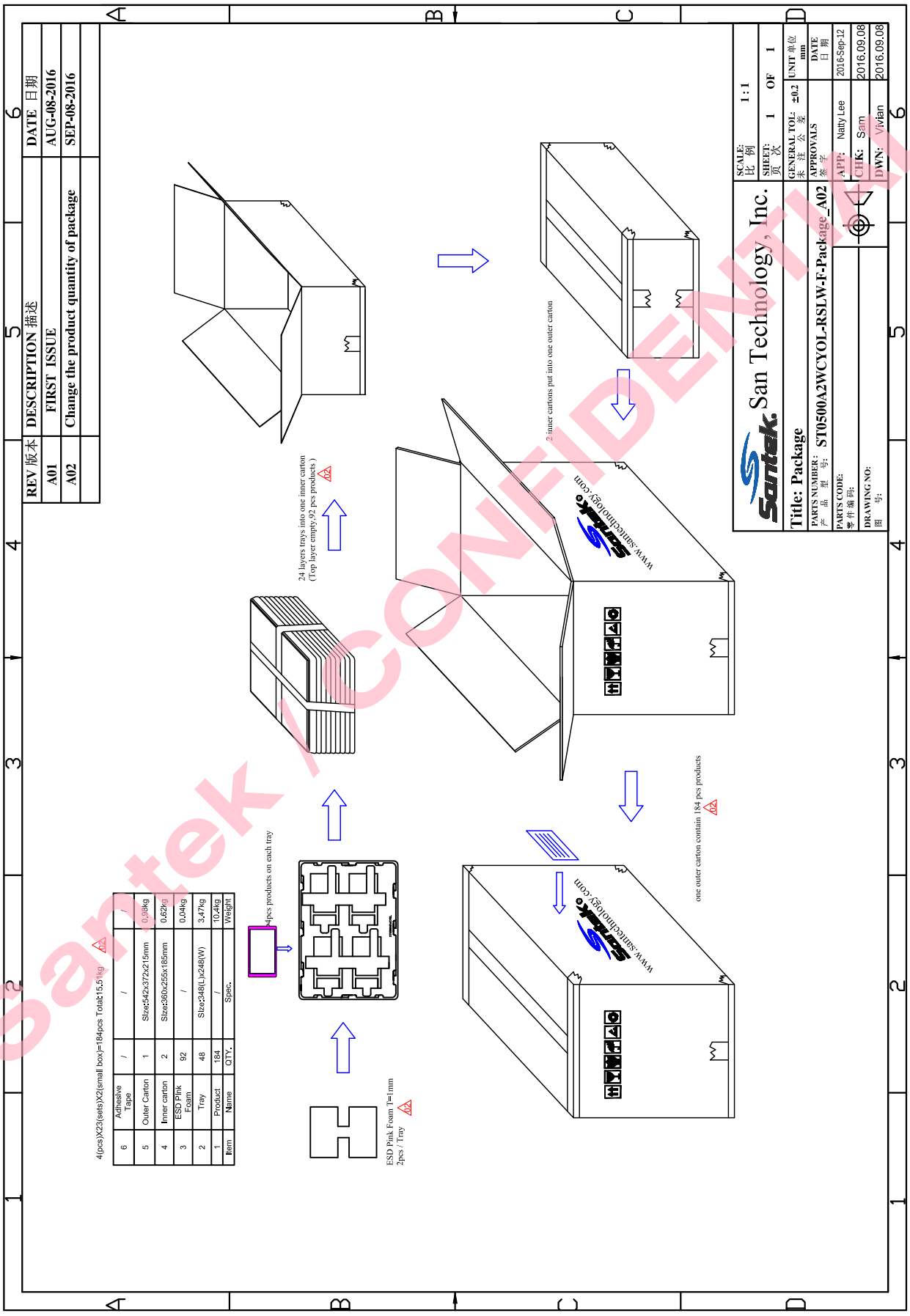
No	Test Item	Condition	Remarks
1	High Temperature Operation	Ts=+70℃, 240hrs	Note 1 IEC60068-2-2, GB2423.2—89
2	Low Temperature Operation	Ta=-20℃, 240hrs	Note 2 IEC60068-2-1, GB2423.1—89
3	High Temperature Storage	Ta=+80℃, 240hrs	IEC60068-2-2, GB2423.2—89
4	Low Temperature Storage	Ta=-30℃, 240hrs	IEC60068-2-1, GB2423.1—89
5	High Temperature & High Humidity Storage	+40℃, 95% RH max, 240 hours (No condensation)	IEC60068-2-3, GB/T2423.3—2006
6	Thermal Shock (Non-operation)	-30℃(30 min)~+80℃(30min) 50 Cycle.	Start with cold temperature, end with high temperature IEC60068-2-14, GB2423.22—87
7	Electro Static Discharge (Operation)	(Test at the center of surface) 150pF,330Ω±10KV Contact 150pF,330Ω±15KV Air	IEC61000-4-2 GB/T17626.2—1998
8	Vibration (Non-operation)	Frequency Range: 10~55Hz, Stroke: 1.5mm Sweep: 10Hz~55Hz~10Hz 2hours for each direction of X.Y.Z. (package condition)	IEC60068-2-6 GB/T2423.10—1995
9	Shock (Non-operation)	100G 6ms, ±X, ±Y, ±Z 1 times for each direction	IEC60068-2-6 GB/T2423.5—1995
10	Package Drop Test	1corner, 3edges, 6surfaces	IEC60068-2-32 GB/T2423.8—1995

11	Ball drop test  	Test requirements: A ball bearing approximately 32.5 Grams Test Procedure:Place the LCD on a flat platform where the LCD is not moving or it can be clamped from the ends.The diagram below is a suggested placement diagram and an apparatus.Drop the ball bearing from the height of 50cm directly to the center of the LCD. 1 times the product will not break as qualified. Hint: The ball bearing can be dropped via a tube to ensure a straight drop in the center of the LCD.	

Note 1: Ts is the temperature of panel's surface.

Note 2: Ta is the ambient temperature of sample.

12. Packing drawing



13.Incoming Inspection Standards

13.1 Acceptable quality level ("AQL")

The AQL for major and minor defects shall be respectively set forth below.

a) Major defects : AQL 0.4

b) Minor defects : AQL 1.0 Based on overall evaluation

13.2 Inspection conditions

Item	Inspection conditions
	Reflection inspection
Ambient illumination	300~700lx
Ambient temperature	18~27℃
Ambient Humidity	50~85%RH
Viewing distance	350mm ± 50mm
Direction of lighting	Set light tube with reflection on the panel surface
Viewing angle	The surface of the Module and the eyes of the inspector shall be 90±5 degrees.
Check pattern(Bright dot)	Black picture position
Check pattern(Black dot)	White & RGB picture position

13.3 Definition

No	Item		Definition
a	Dot	Pixel	3 sub-pixels (R+G+B)
		Dot	1 sub-pixel (R or G or B)
b	Bright dot	A dot, a foreign particle seen as a bright dot, and a CF scratch with a brightness higher than the gray scale levels specified below, visible on the full black pattern. Gray scale level: R:brightness>V150/255, G:brightness>V116/255, B:brightness>V165/255	
c	Black dot	When the Module lights, dot appear black in display at White& RGB picture position.	
d	Tiny bright dot	The gray scale level of R:brightness≦V150/255, G:brightness≦V116/255, B:brightness≦V165/255	

- Scratch that is located in the active area shall be judged according to the criteria for "Bright dot".
- CF scratch shall be judged according to the criteria for "Bright dot".

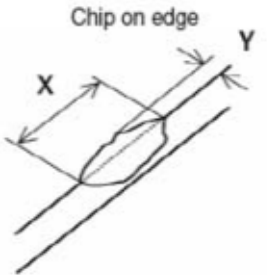
13.4 Acceptable dot defects(Bright dot, Black dot)

		Number of dot defects
Bright dot		3
Foreign particles seen as bright dot		
Tiny bright dot		Ignore
Black dot	1 dot	4
	2 adjacent dots	
	3 adjacent dots	0
Total (Black dots)		5

13.5 Defect distance

Item		Inspection criteria
Defect distance	Black dots	5mm or more
Adjacent dots	Black dots	Two adjacent black dots shall be count as 1 black dot. It shall be allowed according to 13.4
	Bright dots	Adjacent bright dots shall be allowed, in case the brightness is equal or lower than the brightness of the gray levels specified in 13.3b

13.6 Cosmetic & appearance inspection

No.	Defect Description	Acceptable Criteria				Remark
		Size (mm)		Number	Distance	
1	Polarizer Dent or Bubble	D≦0.1		Ignore	Ignore	
		0.1<D≦0.2		N≦5	≧5mm	
		0.2<D≦0.3		N≦3	≧5mm	
		0.3<D≦0.4		N≦1	≧5mm	
		D>0.4		NG	NG	
2	Circular Defects (e.g. particle or OCA bubble)	D≦0.15		Ignore	Ignore	
		0.15<D≦0.3		N≦3	≧5mm	
		0.3 <D≦0.35		N≦2	≧5mm	
		D>0.35		NG	NG	
3	Linera Defects (e.g. fiber)	W≦0.05		Ignore	Ignore	
		0.05<W≦0.1	L≦6.0	N≦3	≧5mm	
		W>0.1	L>5.0	NG	NG	
4	Dent/Fisheye	Follow the limit sample.				
5	Scratch	W≦0.05		Ignore	Ignore	
		0.05<W≦0.1	L≦8.0	N≦3	≧5mm	
		W>0.1	L>8.0	NG	NG	
6	CG Chipping-Edge	Invisible from front side.		Ignore	Ignore	
		X≦3.0	Y≦3.0	N≦4	≧5mm	Reject if N≧3 at any edge.
7	Pinhole in BM area	D≦0.10		Ignore	Ignore	
		0.10<D≦0.2		N≦2	≧5mm	
8	BM Ink Leakage	W≦0.1mm		Ignore	≧5mm	
		0.10≦W≦0.15	L≦10	N≦2	≧5mm	

14. Precautions For Use of LCD modules

14.1 Handling Precautions

14.1.1 The display panel is made of glass. Do not subject it to a mechanical shock by dropping it from a high place, etc.

14.1.2 If the display panel is damaged and the liquid crystal substance inside it leaks out, be sure not to get any in your mouth, if the substance comes into contact with your skin or clothes, promptly wash it off using soap and water.

14.1.3 Do not apply excessive force to the display surface or the adjoining areas since this may cause the color tone to vary.

14.1.4 The polarizer covering the display surface of the LCD module is soft and easily scratched. Handle this polarizer carefully.

14.1.5 If the display surface is contaminated, breathe on the surface and gently wipe it with a soft dry cloth. If still not completely clear, moisten cloth with one of the following solvents:

— Isopropyl alcohol
— Ethyl alcohol

Solvents other than those mentioned above may damage the polarizer. Especially, do not use the following:

— Water
— Ketone
— Aromatic solvents

14.1.6 Do not attempt to disassemble the LCD Module.

14.1.7 If the logic circuit power is off, do not apply the input signals.

14.1.8 To prevent destruction of the elements by static electricity, be careful to maintain an optimum work environment.

14.1.8.1 Be sure to ground the body when handling the LCD Modules.

14.1.8.2 Tools required for assembly, such as soldering irons, must be properly ground.

14.1.8.3 To reduce the amount of static electricity, do not conduct assembly and other work under dry conditions.

14.1.8.4 The LCD Module is coated with a film to protect the display surface. Be care when peeling off this protective film since static electricity may be generated.

14.2 Storage Precautions

14.2.1 When storing the LCD modules, avoid exposure to direct sunlight or to the light of fluorescent lamps.

14.2.2 The LCD modules should be stored under the storage temperature range. If the LCD modules will be stored for a long time, the recommend condition is:
Temperature: 0℃ ~ 40℃ Relatively humidity: ≦80%

14.2.3 The LCD modules should be stored in the room without acid, alkali and harmful gas.

14.3 Transportation Precautions

The LCD modules should be no falling and violent shocking during transportation, and also should avoid excessive press, water, damp and sunshine.

14.4 Mechanical design

This LCM is very thin and narrow edge, Santek recommends there is some support from back side of LCM in customer's assembly.