TLP5231 Preliminary

1. Applications

・Isolated IGBT/Power MOSFET Gate Driers (Pre-driver)

・AC and brushless DC Motor Drives

・Industrial Inverters and Uninterruptible Power Supply (UPS)

2. General

The TLP5231 is a highly integrated 2.5 A dual-output IGBT gate drive photocoupler which a multi-functional IC is housed in a long creepage and clearance SO16L package. This photocoupler is suitable as a pre-driver to driver power devices via external p- and n- channel MOSFET as buffer.
The TLP5231, a smart gate driver photocoupler, includes functions of IGBT/power MOSFET desaturation detection, isolated fault status feedback, soft gate turn-off, active Miller cramping and under voltage lockout (UVLO).
The TLP5231 consists two GaAℓAs infrared light-emitting diodes (LEDs) and two high-gain and high-speed ICs. They realize output current control and fault status feedback with electrical isolation between first and second stage.

3. Features

(1) Peak output current: ±2.5 A (max)

(2) Guaranteed performance over temperature: -40 to 110 ℃

(3) Threshold input current: 3.5 mA (max)

(4) Propagation delay time: 300 ns (max)

(5) Common-mode transient immunity: ±25 kV/μs (min)

(6) Isolation voltage: 5000 Vrms (min)

(7) Safety standards

UL: UL1577, File No.E67349

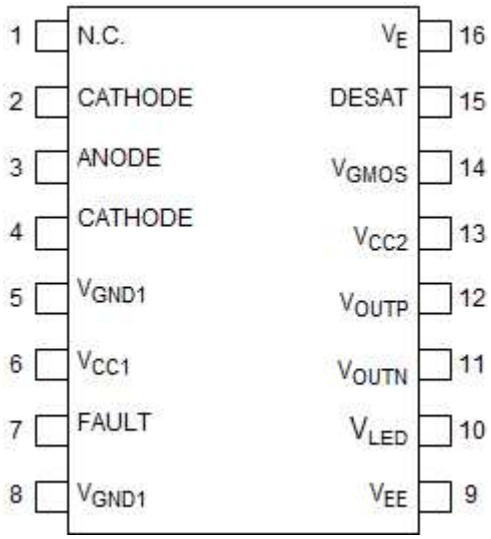
cUL: CSA Component Acceptance Service No.5A File No.E67349

VDE: EN60747-5-5, EN60065, EN60950-1, EN 62368-1 (Note 1)

CQC: GB4943.1, GB8898 (to be applied)

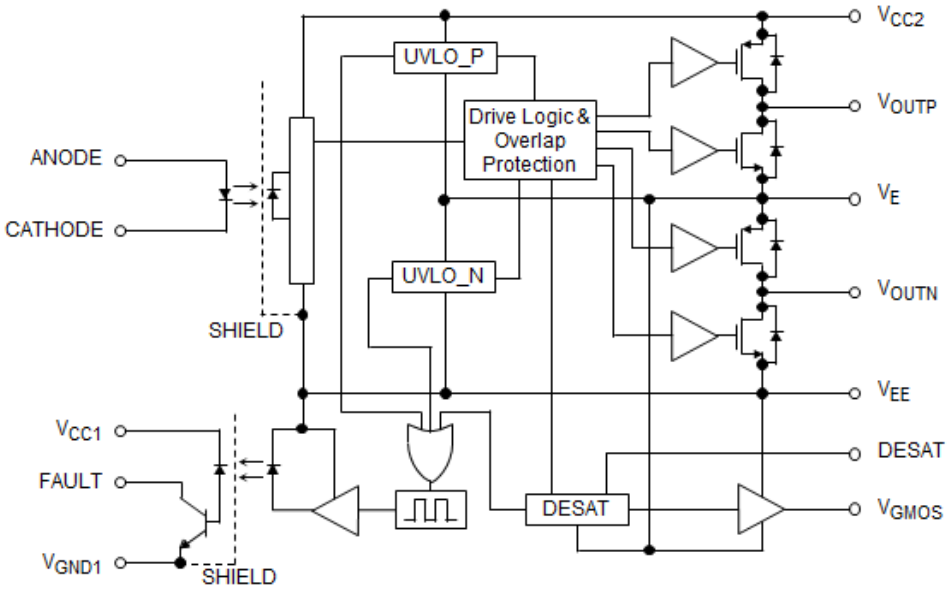
Note 1:When a VDE approved type is needed, please designate the Option (D4).

4. Pin Configuration



1 : No connection
2 : Cathode
3 : Anode
4 : Cathode
5 : Input side ground
6 : Input side supply voltage
7 : Fault output
8 : Input side ground
9 : Negative output supply voltage
10 : No connection, for testing only
11 : Low side voltage output
12 : High side voltage output
13 : Positive output supply voltage
14 : External MOSFET control pin
15 : Desat over current sensing
16 : Common output supply voltage
(power device emitter or source)

5. Internal Circuit (Note)



Note: A 10-μF bypass capacitor must be connected between pins 9 (V_{EE}) and 13 (V_{CC2}), and a 1-μF bypass capacitor must be connected between pins 13 (V_{CC2}) and 16 (V_E), and pins 9 (V_{EE}) and 16 (V_E). The total lead length between capacitor and coupler should not exceed 1 cm.

6. Principle of Operation

6.1 Truth Table

I_F	UVLO_P, UVLO_N	DESAT	FAULT	V_{OUTP}	V_{OUTN}	V_{GMOS}
X	Active	Not active	H (V_{CC1})	H (V_{CC2})	H (V_E)	H (V_E)
ON	Not active	Active (with DESAT fault)	H (V_{CC1})	H (V_{CC2})	L (V_{EE})	H (V_E)
ON	Not active	Active (without DESAT fault)	L (V_{GND1})	L (V_E)	L (V_{EE})	L (V_{EE})
OFF	Not active	Not active	L (V_{GND1})	H (V_{CC2})	H (V_E)	L (V_{EE})

6.2 Mechanical Parameters

Characteristics	Size	Unit
Height	2.3 (max)	mm
Creepage distances	8.0 (min)	
Clearance distances	8.0 (min)	
Internal isolation thickness	0.4 (min)	

7. Absolute Maximum Ratings (Note) (Unless otherwise specified, Ta = 25 ℃)

	Characteristics	Symbol	Note	RATING	Unit
LED	Input forward current	I_F		25	mA
	Input forward current derating (Ta ≥ 95 ℃)	$\Delta I_F / \Delta T_a$		-0.84	mA/℃
	Peak transient input forward current	I_{FPT}	(Note 1)	1	A
	Peak transient input forward current derating (Ta ≥ 95 °C)	$\Delta I_{FPT} / \Delta T_a$	(Note 3)	-34	mA/℃
	Reverse Voltage	V_R		5	V
	Input power dissipation	P_D		150	mW
	Input power dissipation derating (Ta ≥ 95 ℃)	$\Delta P_D / \Delta T_a$	(Note 3)	-5.0	mW/℃
Detector	Positive input supply voltage	V_{CC1}		-0.5 to 7	V
	Peak high-level output current (Ta = -40 to 110 ℃)	I_{OPH}	(Note 2)	-2.5	A
	Peak low-level output current (Ta = -40 to 110 ℃)	I_{OPL}	(Note 2)	+2.5	
	FAULT output current	I_{FAULT}		8	mA
	FAULT pin voltage	V_{FAULT}		-0.5 to V_{CC1}	V
	Total output supply voltage	$(V_{CC2} - V_{EE})$	(Note 6)	-0.5 to 35	V
	Negative output supply voltage	$(V_E - V_{EE})$	(Note 6)	-0.5 to 17	V
	Positive output supply voltage	$(V_{CC2} - V_E)$	(Note 6)	-0.5 to 30	V
	High side output voltage	$V_{OUTP(Peak)}$		V_E – 0.5 to V_{CC2} + 0.5	V
	Low side output voltage	$V_{OUTN(Peak)}$		V_{EE} – 0.5 to V_E + 0.5	V
	DESAT voltage	V_{DESAT}		V_E – 0.5 to V_{CC2} + 0.5	V
	V_{GMOS} voltage	V_{GMOS}		V_{EE} – 0.5 to V_E + 0.5	V
	Output power dissipation	P_O		410	mW
	Output power dissipation derating (T_a ≥ 95 °C)	$\Delta P_O / \Delta T_a$	(Note 3)	-14.0	mW/℃
Common	Operating temperature	T_{opr}		-40 to 110	℃
	Storage temperature	T_{stg}		-55 to 125	
	Lead soldering temperature (10 s)	T_{sol}	(Note 4)	260	
	Isolation voltage (AC,1 min.,R.H. ≤ 60%,Ta=25 ℃)	BV_S	(Note 5)	5000	V_{rms}

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook (“Handling Precautions”/”Derating Concept and Methods”) and individual reliability data (i.e. reliability test report and estimated failure rate, etc.)

Note: A ceramic capacitor (10 μF) must be connected between pins 9 (V_{EE}) and 13 (V_{CC2}), and a ceramic capacitor (1 μF) must be connected between pins 13 (V_{CC2}) and 16 (V_E), and pins 9 (V_{EE}) and 16 (V_E) to stabilize the operation of the high gain linear amplifier. Failure to provide the bypassing may impair the switching property. The total lead length between capacitor and coupler should not exceed 1 cm.

Note 1: Pulse width ≤ 1 μs, 300 pps

Note 2: Exponential waveform. Pulse width ≤ 0.2 μs, f ≤ 15 kHz, V_{CC2} = 15 V

Note 3: Soldered on a substrate designated by JEDEC.

Note 4: For the effective lead soldering area..

Note 5: This device is considered as a two-terminal device: Pins 1 through 8 are shorted together, and pins 9 through 16 are shorted together.

Note 6: Power supply sequence must be 1) $V_E - V_{EE}$, 2) $V_{CC2} - V_E$.

8. Recommended Operating Conditions (Note)

Characteristics	Symbol	Note	Min	Typ.	Max	Unit
Total output supply voltage	(V_{CC2} - V_{EE})	(Note 1)	21	-	30	V
Negative output supply voltage	(V_E - V_{EE})	(Note 1)	6	-	15	V
Positive output supply voltage	(V_{CC2} - V_E)	(Note 1)	15	-	30 - (V_E - V_{EE})	V
Positive input supply voltage	V_{CC1}		3.3	-	5.5	V
Input on-state current	$I_{F(ON)}$	(Note 2)	5.3	-	12	mA
Input off-stage voltage	$V_{F(OFF)}$	(Note 2)	0	-	0.8	V

Note: The recommended operating conditions are given as a design guide necessary to obtain the intended performances of the device. Each parameter is an independent value. When creating a system design using this device, the electrical characteristics specified in this datasheet should also be considered.

Note 1: If the V_{CC2} and V_{EE} rise is sharp, an internal circuit might not be operate with stability. Please design the V_{CC2} and V_{EE} rise slope under 0.1 V/μs.

Note 2: The rise and fall times of the input on-current should be less than 0.5 μs.

9. Electrical Characteristics (Note)
(Unless otherwise specified, Ta = -40 to 110 ℃, V_{CC2} – V_E = 15 V, V_E – V_{EE} = 8 V)

Characteristics	Symbol	Note	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input forward voltage	V_F			I_F = 10 mA, T_a = 25 ℃	1.45	-	1.7	V
Input reverse current	I_R			V_R = 5 V	-	-	10	μA
Input capacitance	C_t			V = 0 V, f = 1 MHz, T_a = 25 ℃	-	60	-	pF
FAULT low level output voltage	V_{FAULTL}			V_{DESAT} = 0 V, R_F = 10 kΩ, C_F = 1 nF, V_{CC1} = 3.3 or 5.5 V	-	0.1	0.25	V
FAULT high level output voltage	V_{FAULTH}			V_{DESAT} = Open, R_F = 10 kΩ, C_F = 1 nF, V_{CC1} = 3.3 or 5.5 V	-	V_{CC1}	-	V
FAULT low level output current	I_{FAULTL}			V_{FAULT} = 0.15 V, V_{CC1} = 3.3 or 5 V	-	1.2	-	mA
FAULT high level output current	I_{FAULTH}			V_{FAULT} = V_{CC1} = 3.3 or 5 V	-	0.01	1	μA
V_{OUTP} high level output current	I_{OUTPH}	(Note 1)	TBD	V_{CC2} – V_{OUTP} = 7 V	—	—	-1.0	A
V_{OUTP} low level output current	I_{OUTPL}	(Note 1)	TBD	V_{OUTP} – V_E = 7 V, I_F = 8 mA	1.0	—	—	
V_{OUTN} high level output current	I_{OUTNH}	(Note 1)	TBD	V_E – V_{OUTN} = 7 V	—	—	-1.0	
V_{OUTN} low level output current	I_{OUTNL}	(Note 1)	TBD	V_{OUTN} – V_{EE} = 7 V, I_F = 8 mA	1.0	—	—	
V_{OUTP} high level output resistance	R_{OUTPH}	(Note 1)	—	I_{OUTP} = -1.0 A, V_F = 0 V	—	1.6	4.4	Ω
V_{OUTP} low level output resistance	R_{OUTPL}	(Note 1)	—	I_{OUTP} = 1.0 A, I_F = 8 mA	—	1.2	3.3	
V_{OUTN} high level output resistance	R_{OUTNH}	(Note 1)	—	I_{OUTN} = -1.0 A, V_F = 0 V	—	1.9	5.0	
V_{OUTN} low level output resistance	R_{OUTNL}	(Note 1)	—	I_{OUTN} = 1.0 A, I_F = 8 mA	—	1.0	3.3	
V_{OUTP} high level output voltage	V_{OUTPH}		TBD	I_{OUTP} = −100 mA, V_F = 0 V	V_{CC2}−0.43	V_{CC2}−0.15	—	V
V_{OUTP} low leve output voltage	V_{OUTPL}		TBD	I_{OUTP} = 100 mA, I_F = 8 mA	—	V_E+0.1	V_E+0.32	
V_{OUTN} high level output voltage	V_{OUTNH}		TBD	I_{OUTN} = −100 mA, V_F = 0 V	V_E−0.4	V_E−0.2	—	
V_{OUTN} low leve output voltage	V_{OUTNL}		TBD	I_{OUTN} = 100 mA, I_F = 8 mA	—	V_{EE}+0.1	V_{EE}+0.3	
V_{GMOS} high level ouptut current	I_{OUTGH}		TBD	V_E – V_{GMOS} = 8 V, I_F = 8 mA, DESAT = Open	-	-	−105	mA
V_{GMOS} low level output current	I_{OUTGL}		TBD	V_{GMOS} – V_{EE} = 8 V, V_F = 0 V, DESAT = Open	90	-	-	
V_{GMOS} high level output resistance	R_{OUTGH}		—	I_{OUTG} = -80 mA, I_F = 8 mA	-	10	30	Ω
V_{GMOS} low leve output resistance	R_{OUTGL}		—	I_{OUTN} = 80 mA, V_F = 0 V, DESAT = Open	-	4	10	
V_{GMOS} high level output voltage	V_{OUTGH}		—	I_{OUTG} = -1 mA, I_F = 8 mA, DESAT = Open	-	V_E	-	V
V_{GMOS} low level output voltage	V_{OUTGL}		—	I_{OUTN} = 1 mA, V_F = 0 V, DESAT = Open	-	V_{EE}	-	

Electrical Characteristics (Note)
(Unless otherwise specified, Ta = -40 to 110 ℃, V_{CC2} – V_E = 15 V, V_E – V_{EE} = 8 V)

Characteristics	Symbol	Note	Test Circuit	Test Condition	Min	Typ.	Max	Unit
High level supply current (V_{CC2})	I_{CC2H}		TBD	V_F = 0 V, no load	—	6	10.2	mA
Low level supply current (V_{CC2})	I_{CC2L}		TBD	I_F = 8 mA, no load	—	6.5	10.2	
High level supply current (V_{EE})	I_{EEH}		TBD	V_F = 0 V, no load	-9.2	-5	—	
Low leve supply current (V_{EE})	I_{EEL}		TBD	I_F = 8 mA, no load	-9.2	-5	—	
Threshold input current (H/L)	I_{FHL}		—	V_{OUTP} – V_E < 5 V, V_{OUTN} – V_{EE} < 1 V	—	1	3.5	
Threshold input voltage (L/H)	V_{FLH}		—	V_{OUTP} – V_E > 5 V, V_{OUTN} – V_{EE} > 1 V	0.8	—	—	V
UVLO_P threshold (V_{CC2} – V_E)	V_{UVLOP+}		TBD	I_F = 8 mA, V_{OUTP} – V_E < 5 V	12	13	14	
	V_{UVLOP-}			I_F = 8 mA, V_{OUTP} – V_E > 5 V	11	12	13	
UVLO_P hysteresis (V_{CC2} – V_E)	V_{UVLOP_HYS}			—	—	1	—	
UVLO_N threshold (V_E – V_{EE})	V_{UVLON+}			I_F = 8 mA, V_{OUTN} – V_{EE} < 1 V	-6	-5.3	-5	
	V_{UVLON-}			I_F = 8 mA, V_{OUTN} – V_{EE} > 1 V	-5.7	-5.0	-4.7	
UVLO_N hysteresis (V_E – V_{EE})	V_{UVLON_HYS}			—	—	0.3	—	
DESAT threshold	V_{DESAT}		—	V_{CC2} – V_E > V_{UVLOP-}, V_E – V_{EE} > V_{UVLON-}	7.5	8.0	9.0	
Blanking capacitor charging current	I_{CHG}		TBD	V_{DESAT} = 2 V	-0.9	-0.5	-0.2	mA
DESAT low voltage when blanking capacitor discharge	V_{DSCHG}		TBD	I_{DSCHG} = 10 mA	—	1.1	3.0	V

Note: All typical values are at T_a = 25 ℃.

Note: This device is designed for low power consumption, making it more sensitive to ESD than its predecessors. Extra care should be taken in the design of circuitry and pc board implementation to avoid ESD problems.

Note 1: I_O application time ≤ 10 μs, single pulse

10. Isolation Characteristics (Unless otherwise specified, Ta = 25 ℃)

Characteristics	Symbol	Note	Test conditions	Min	Typ.	Max	Unit
Total capacitance (input to output)	C_S	(Note 1)	V_S = 0 V, f = 1 MHz	-	1.0	-	pF
Isolation resistance	R_S	(Note 1)	V_S = 500 V, R.H. ≤ 60 %	1×10^{12}	1×10^{14}	-	Ω
Isolation voltage	BV_S	(Note 1)	AC, 60 s	5000	-	-	V_{rms}

Note1: This device considered a two-terminal device: All pins on the LED side are shorted together, and all pin on the photodetector side are shorted together.

11. Switching Characteristics (Note)
(Unless otherwise specified, Ta=-40 to 110 ℃, V_{CC2} – V_E = 15 V, V_E – V_{EE} = 8 V)

Characteristics	Symbol	Note	Test Circuit	Condition	Min	Typ.	Max	Unit
Propagation delay time (L/H)	t_{pLH}	(Note 1)	TBD	I_F = 8 → 0 mA, C_P = C_N = 4 nF, f = 20 kHz, duty = 50 %	100	200	300	ns
Propagation delay time (H/L)	t_{pHL}			I_F = 0 → 8 mA, C_P = C_N = 4 nF, f = 20 kHz, duty = 50 %	100	200	300	
Pulse width distortion	$\lvert t_{pHL} - t_{pLH} \rvert$			I_F = 0 ←→ 8 mA, C_P = C_N = 4 nF, f = 20 kHz, duty = 50 %	-	-	150	
Propagation delay skew (device to device)	t_{psk}	(Note 1) (Note 2)			-200	-	200	
LED off to 90 % of V_{OUTP}	t_{DP}	(Note 1)		I_F = 8 → 0 mA, C_P = C_N = 4 nF, f = 20 kHz, duty = 50 %	50	150	250	
LED on to 10 % of V_{OUTN}	t_{DN}			I_F = 0 → 8 mA, C_P = C_N = 4 nF, f = 20 kHz, duty = 50 %	50	130	250	
Non-overlap time low to high	t_{NLH}			I_F = 8 → 0 mA, C_P = C_N = 4 nF, f = 20 kHz, duty = 50 %	-	60	-	
Non-overlap time high to low	t_{NHL}			I_F = 0 → 8 mA, C_P = C_N = 4 nF, f = 20 kHz, duty = 50 %	-	50	-	
Rise time on V_{OUTP}	t_{PR}			I_F = 8 → 0 mA, C_P = C_N = 4 nF, f = 20 kHz, duty = 50 %	-	50	-	
Fall time on V_{OUTP}	t_{PF}			I_F = 0 → 8 mA, C_P = C_N = 4 nF, f = 20 kHz, duty = 50 %	-	50	-	
Rise time on V_{OUTN}	t_{NR}			I_F = 8 → 0 mA, C_P = C_N = 4 nF, f = 20 kHz, duty = 50 %	-	50	-	
Fall time on V_{OUTN}	t_{NF}			I_F = 0 → 8 mA, C_P = C_N = 4 nF, f = 20 kHz, duty = 50 %	-	40	-	
Propagation delay time from DESAT threshold to 50 % of high V_{GMOS}	t_1		TBD	C_P = C_N = 4 nF, C_G = 1 nF, f = 100 Hz, duty = 50 %, I_F = 8 mA, C_{BLANK} = 200 pF, V_{DESAT} = 8.0 V, Pos-edge	—	450	750	
Propagation delay time from DESAT threshold to 50 % of high V_{OUTP}	t_2				—	340	700	
Propagation delay time from DESAT threshold to 50 % of high V_{FAULT}	t_3			R_F = 10 kΩ, C_F = 1 nF, V_{CC1} = 3.3 or 5 V, f = 100 Hz, duty = 50 %, I_F = 8 mA	—	9	20	µs
Propagation delay time from 50% V_{GMOS} to 50 % of V_{OUTN}	t_4			C_P = C_N =4 nF, C_G = 1 nF, f = 100 Hz, duty = 50 %, I_F = 8 mA	—	11	—	ns
Mute time (Note 3)	t_{MUTE}	(Note 3)		I_F = 8 mA	0.68	1	1.7	ms
DESAT leading edge blanking time	$t_{DESAT(LEB)}$			—	—	520	—	ns
DESAT filter time	$t_{DESAT(FILTER)}$			R_{DESAT} = 100 Ω, V_{in} = 10 V, P_W = 1 µs, Monitor: V_{OUTP}, V_{GMOS}	—	270	—	
Common-mode transient immunity at high level	CM_H	(Note 4)	TBD	V_{CM} = 1000 V_{p-p}, I_F = 0 mA, V_{in} = 5 V, V_{CC} = 15 V, R_{in} = 220 Ω (with split resistors) T_a = 25 ℃, $V_{O(min)}$ = 10 V	±25	—	—	kV/µs
Common-mode transient immunity at low level	CM_L	(Note 5)		V_{CM} = 1000 V_{p-p}, I_F = 10 mA, V_{in} = 5 V, V_{CC} = 15 V, R_{in} = 220 Ω (with split resistors) T_a = 25 ℃, $V_{O(min)}$ = 1 V	±25	—	—	

Note: All typical values are at T_a = 25 ℃.

Note 1: Input signal: t_r = t_f = 5 ns or less
C_L is approximately 15 pF which includes probe and stray wiring capacitance.

Note 2: The propagation delay skew, t_{psk}, is equal to the magnitude of the worst-case difference in t_{pHL} and/or t_{pLH} that will be seen between units at the same given conditions (supply voltage, input current, temperature, etc).

Note 3: Automatic reset: This is the minimum time when V_{OUTP} is high, V_{OUTN} is low, V_{GMOS} is high and FAULT is high, after DESAT threshold is exceeded. LED trigger reset: After t_{MUTE}, operation will be resumed when IF changes from high to low.

Note 4: CM_H is the maximum rate of fall of the common mode voltage that can sustained with the output voltage in the logic high state (V_{OUTP} – V_E > 12 V, V_{OUTN} – V_{EE} > 5 V or V_{FAULT} > 2 V).

Note 5: CM_L is the maximum rate of rise of the common mode voltage that can sustained with the output voltage in the logic low state (V_{OUTP} – V_E < 1 V, V_{OUTN} – V_{EE} < 1 V or V_{FAULT} < 0.8 V).

12. Timing diagram

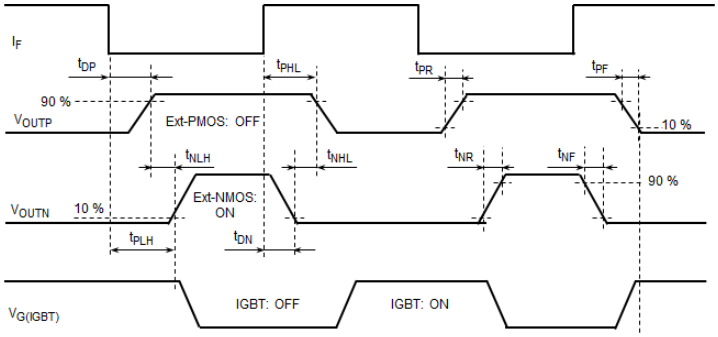


Fig.12.1 Normal state

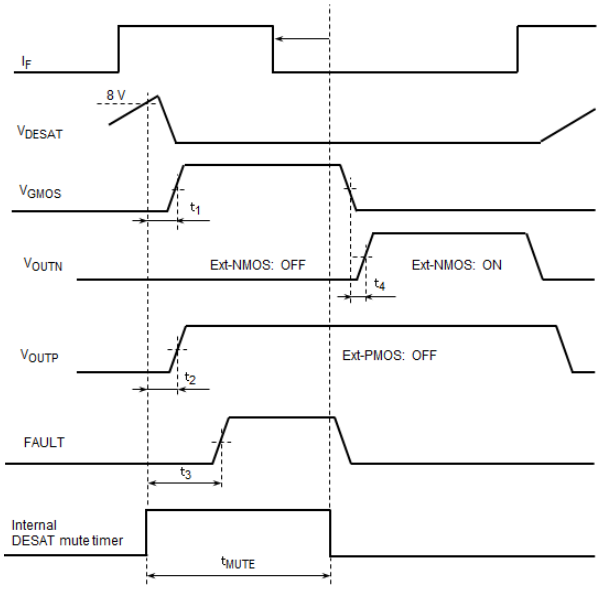


Fig.12.2 DESAT fault state (LED turn off before t_{MUTE} timeout: Automatic reset)

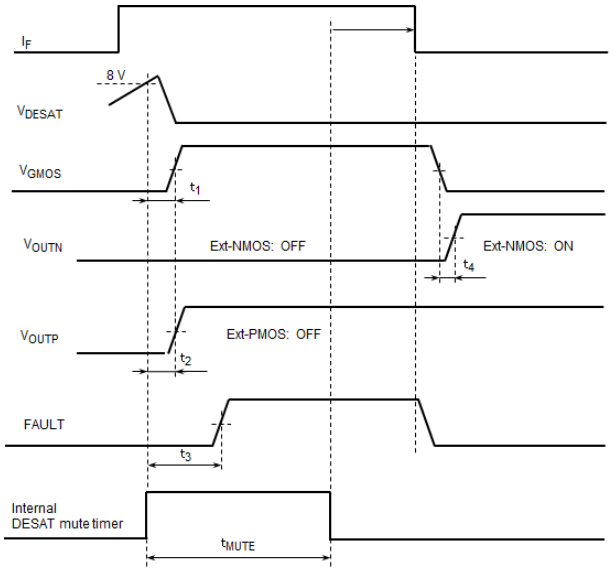


Fig.12.3 DESAT fault state (LED turn off after t_{MUTE} timeout: Reset by LED trigger)

RESTRICTIONS ON PRODUCT USE

Toshiba Corporation and its subsidiaries and affiliates are collectively referred to as “TOSHIBA”.
Hardware, software and systems described in this document are collectively referred to as “Product”.

- TOSHIBA reserves the right to make changes to the information in this document and related Product without notice.
- This document and any information herein may not be reproduced without prior written permission from TOSHIBA. Even with TOSHIBA's written permission, reproduction is permissible only if reproduction is without alteration/omission.
- Though TOSHIBA works continually to improve Product's quality and reliability, Product can malfunction or fail. Customers are responsible for complying with safety standards and for providing adequate designs and safeguards for their hardware, software and systems which minimize risk and avoid situations in which a malfunction or failure of Product could cause loss of human life, bodily injury or damage to property, including data loss or corruption. Before customers use the Product, create designs including the Product, or incorporate the Product into their own applications, customers must also refer to and comply with (a) the latest versions of all relevant TOSHIBA information, including without limitation, this document, the specifications, the data sheets and application notes for Product and the precautions and conditions set forth in the "TOSHIBA Semiconductor Reliability Handbook" and (b) the instructions for the application with which the Product will be used with or for. Customers are solely responsible for all aspects of their own product design or applications, including but not limited to (a) determining the appropriateness of the use of this Product in such design or applications; (b) evaluating and determining the applicability of any information contained in this document, or in charts, diagrams, programs, algorithms, sample application circuits, or any other referenced documents; and (c) validating all operating parameters for such designs and applications. **TOSHIBA ASSUMES NO LIABILITY FOR CUSTOMERS' PRODUCT DESIGN OR APPLICATIONS.**
- **PRODUCT IS NEITHER INTENDED NOR WARRANTED FOR USE IN EQUIPMENTS OR SYSTEMS THAT REQUIRE EXTRAORDINARILY HIGH LEVELS OF QUALITY AND/OR RELIABILITY, AND/OR A MALFUNCTION OR FAILURE OF WHICH MAY CAUSE LOSS OF HUMAN LIFE, BODILY INJURY, SERIOUS PROPERTY DAMAGE AND/OR SERIOUS PUBLIC IMPACT ("UNINTENDED USE"). ** Except for specific applications as expressly stated in this document, Unintended Use includes, without limitation, equipment used in nuclear facilities, equipment used in the aerospace industry, medical equipment, equipment used for automobiles, trains, ships and other transportation, traffic signaling equipment, equipment used to control combustions or explosions, safety devices, elevators and escalators, devices related to electric power, and equipment used in finance-related fields. **IF YOU USE PRODUCT FOR UNINTENDED USE, TOSHIBA ASSUMES NO LIABILITY FOR PRODUCT.** For details, please contact your TOSHIBA sales representative.
- Do not disassemble, analyze, reverse-engineer, alter, modify, translate or copy Product, whether in whole or in part.
- Product shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable laws or regulations.
- The information contained herein is presented only as guidance for Product use. No responsibility is assumed by TOSHIBA for any infringement of patents or any other intellectual property rights of third parties that may result from the use of Product. No license to any intellectual property right is granted by this document, whether express or implied, by estoppel or otherwise.
- **ABSENT A WRITTEN SIGNED AGREEMENT, EXCEPT AS PROVIDED IN THE RELEVANT TERMS AND CONDITIONS OF SALE FOR PRODUCT, AND TO THE MAXIMUM EXTENT ALLOWABLE BY LAW, TOSHIBA (1) ASSUMES NO LIABILITY WHATSOEVER, INCLUDING WITHOUT LIMITATION, INDIRECT, CONSEQUENTIAL, SPECIAL, OR INCIDENTAL DAMAGES OR LOSS, INCLUDING WITHOUT LIMITATION, LOSS OF PROFITS, LOSS OF OPPORTUNITIES, BUSINESS INTERRUPTION AND LOSS OF DATA, AND (2) DISCLAIMS ANY AND ALL EXPRESS OR IMPLIED WARRANTIES AND CONDITIONS RELATED TO SALE, USE OF PRODUCT, OR INFORMATION, INCLUDING WARRANTIES OR CONDITIONS OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, ACCURACY OF INFORMATION, OR NONINFRINGEMENT.**
- GaAs (Gallium Arsenide) is used in Product. GaAs is harmful to humans if consumed or absorbed, whether in the form of dust or vapor. Handle with care and do not break, cut, crush, grind, dissolve chemically or otherwise expose GaAs in Product.
- Do not use or otherwise make available Product or related software or technology for any military purposes, including without limitation, for the design, development, use, stockpiling or manufacturing of nuclear, chemical, or biological weapons or missile technology products (mass destruction weapons). Product and related software and technology may be controlled under the applicable export laws and regulations including, without limitation, the Japanese Foreign Exchange and Foreign Trade Law and the U.S. Export Administration Regulations. Export and re-export of Product or related software or technology are strictly prohibited except in compliance with all applicable export laws and regulations.
- Please contact your TOSHIBA sales representative for details as to environmental matters such as the RoHS compatibility of Product. Please use Product in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. **TOSHIBA ASSUMES NO LIABILITY FOR DAMAGES OR LOSSES OCCURRING AS A RESULT OF NONCOMPLIANCE WITH APPLICABLE LAWS AND REGULATIONS.**