

RELIABILITY REPORT
FOR
MAX8895xEWA+T
WAFER LEVEL PRODUCT

October 4, 2010

MAXIM INTEGRATED PRODUCTS

120 SAN GABRIEL DR.
SUNNYVALE, CA 94086

Approved by
Richard Aburano
Quality Assurance
Manager, Reliability Operations

Conclusion

The MAX8895xEWA+T successfully meets the quality and reliability standards required of all Maxim products. In addition, Maxim's continuous reliability monitoring program ensures that all outgoing product will continue to meet Maxim's quality and reliability standards.

Table of Contents

I.Device Description	V.Quality Assurance Information
II.Manufacturing Information	VI.Reliability Evaluation
III.Packaging Information	IV.Die Information
.....Attachments	

I. Device Description

A. General

The MAX8895_ USB-compliant linear battery chargers operate from either a USB port or dedicated charger with automatic detection of adapter type and USB enumeration capability. The MAX8895X/MAX8895Y integrate the battery disconnect switch, current-sense circuit, MOSFET pass elements, and thermal regulation circuitry, and eliminate the external reverse-blocking Schottky diode to create the simplest and smallest stand alone charging solutions. The MAX8895_ include an automated detection of charge adapter type, making it possible to distinguish between USB 2.0 device, USB charger, and dedicated charger devices. Furthermore, the MAX8895X/MAX8895Y include a USB enumeration function that automatically negotiates with a USB host, making it possible to achieve the highest current available from a USB 2.0 device or USB charger without processor intervention. The adapter type detection is compliant with USB 2.0 specification as well as USB charging Revision 1.1. The MAX8895_ control the charging sequence for single-cell Li+ batteries from initial power-OK indication, through prequalification, fast-charge, top-off, and finally charge termination. Charging is controlled using constant current, constant voltage, and constant die-temperature (CCCVCTJ) regulation for safe operation under all conditions. The maximum charging current is adaptively controlled by subtracting the system current from the input current limit, ensuring that the charging current is always maximized for any given operating condition. The MAX8895_ feature optimized smart power control to make the best use of limited USB or adapter power. Battery charge current is set independently of the SYS input current limit. Power not used by the system charges the battery. Automatic input selection switches the system from battery to external power. This allows the application to operate without a battery, discharged battery, or dead battery. Other features include undervoltage lockout (UVLO), overvoltage protection (OVP), charge status flag, charge fault flag, power-OK monitor, battery thermistor monitor, charge timer, and a 3.3V output.

The MAX8895_ operate from a +4.0V to +6.6V supply and include overvoltage protection up to +16V. The MAX8895_ are specified over the extended temperature range (-40°C to +85°C) and are available in a compact 2.38mm x 2.38mm, 25-bump WLP package (0.4mm pitch).

II. Manufacturing Information

A. Description/Function:	Li-ion Chargers with Smart Power Selector™, Adapter Type Detection and USB Enumeration
B. Process:	S18
C. Number of Device Transistors:	78478
D. Fabrication Location:	California
E. Assembly Location:	Japan
F. Date of Initial Production:	April 13, 2010

III. Packaging Information

A. Package Type:	25-bump WLP 5x5 array
B. Lead Frame:	N/A
C. Lead Finish:	N/A
D. Die Attach:	None
E. Bondwire:	N/A (N/A mil dia.)
F. Mold Material:	N/A
G. Assembly Diagram:	#05-9000-3900
H. Flammability Rating:	Class UL94-V0
I. Classification of Moisture Sensitivity per JEDEC standard J-STD-020-C	Level 1
J. Single Layer Theta Ja:	°C/W
K. Single Layer Theta Jc:	°C/W
L. Multi Layer Theta Ja:	52°C/W
M. Multi Layer Theta Jc:	11°C/W

IV. Die Information

A. Dimensions:	93.70 X 93.70 mils
B. Passivation:	Si ₃ N ₄ /SiO ₂ (Silicon nitride/ Silicon dioxide)
C. Interconnect:	Al with Ti/TiN Barrier
D. Backside Metallization:	None
E. Minimum Metal Width:	0.18μm
F. Minimum Metal Spacing:	0.18μm
G. Bondpad Dimensions:	5 mil. Sq.
H. Isolation Dielectric:	SiO ₂
I. Die Separation Method:	Wafer Saw

V. Quality Assurance Information

A. Quality Assurance Contacts:	Richard Aburano (Manager, Reliability Operations) Bryan Preeshl (Vice President of QA)
B. Outgoing Inspection Level:	0.1% for all electrical parameters guaranteed by the Datasheet. 0.1% For all Visual Defects.
C. Observed Outgoing Defect Rate:	< 50 ppm
D. Sampling Plan:	Mil-Std-105D

VI. Reliability Evaluation

A. Accelerated Life Test

The results of the 135°C biased (static) life test are shown in Table 1. Using these results, the Failure Rate (λ) is calculated as follows:

$$\lambda = \frac{1}{\text{MTTF}} = \frac{1.83}{192 \times 4340 \times 48 \times 2} \text{ (Chi square value for MTTF upper limit)}$$

(where 4340 = Temperature Acceleration factor assuming an activation energy of 0.8eV)

$$\lambda = 22.9 \times 10^{-9}$$
$$\lambda = 22.9 \text{ F.I.T. (60\% confidence level @ 25°C)}$$

The following failure rate represents data collected from Maxim's reliability monitor program. Maxim performs quarterly life test monitors on its processes. This data is published in the Reliability Report found at <http://www.maxim-ic.com/qa/reliability/monitor>. Cumulative monitor data for the S18 Process results in a FIT Rate of 0.40 @ 25C and 6.96 @ 55C (0.8 eV, 60% UCL)

B. E.S.D. and Latch-Up Testing (lot SB4ZAQ002C, D/C 1003)

The PR39 die type has been found to have all pins able to withstand a transient pulse of

ESD-HBM:	+/- 2500V per JEDEC JESD22-A114
ESD-CDM:	+/- 750V per JEDEC JESD22-C101

Latch-Up testing has shown that this device withstands a current of +/- 250mA and overvoltage per JEDEC JESD78.

Table 1
Reliability Evaluation Test Results

MAX8895xEWA+T

TEST ITEM	TEST CONDITION	FAILURE IDENTIFICATION	SAMPLE SIZE	NUMBER OF FAILURES	COMMENTS
Static Life Test (Note 1)	Ta = 135°C Biased Time = 192 hrs.	DC Parameters & functionality	48	0	SB4ZAQ002C, D/C 1003

Note 1: Life Test Data may represent plastic DIP qualification lots.