Dual D Flip-Flop with Set and Reset with LSTTL Compatible Inputs

High-Performance Silicon-Gate CMOS

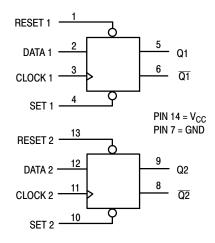
The MC74HCT74A is identical in pinout to the LS74. This device may be used as a level converter for interfacing TTL or NMOS outputs to High Speed CMOS inputs.

This device consists of two D flip–flops with individual Set, Reset, and Clock inputs. Information at a D–input is transferred to the corresponding Q output on the next positive going edge of the clock input. Both Q and \overline{Q} outputs are available from each flip–flop. The Set and Reset inputs are asynchronous.

Features

- Output Drive Capability: 10 LSTTL Loads
- TTL NMOS Compatible Input Levels
- Outputs Directly Interface to CMOS, NMOS, and TTL
- Operating Voltage Range: 4.5 to 5.5 V
- Low Input Current: 1.0 μA
- In Compliance With the JEDEC Standard No. 7.0 A Requirements
- Chip Complexity: 136 FETs or 34 Equivalent Gates
- These Devices are Pb-Free, Halogen Free and are RoHS Compliant

LOGIC DIAGRAM



Design Criteria	Value	Units
Internal Gate Count†	34	ea.
Internal Gate Propagation Delay	1.5	ns
Internal Gate Power Dissipation	5.0	μW
Speed Power Product	.0075	рЈ

[†]Equivalent to a two-input NAND gate.



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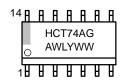
http://onsemi.com



PIN ASSIGNMENT

			_
RESET 1	1 •	14	□ v _{cc}
DATA 1	2	13	RESET 2
CLOCK 1	3	12	DATA 2
SET 1	4	11	CLOCK 2
Q1 [5	10	SET 2
Q1 [6	9] Q2
GND [7	8] Q2

MARKING DIAGRAM



A = Assembly Location

WL = Wafer Lot

Y, YY = Year

WW = Work Week

G = Pb-Free Package

FUNCTION TABLE

	Inp	Out	puts		
Set	Reset	Clock	Data	Q	Q
L	Н	Х	Χ	Н	L
Н	L	Χ	X	L	Н
L	L	Χ	X	H*	H*
Н	Н		Н	Н	L
Н	Н	\mathcal{L}	L	L	Н
Н	Н	L	Χ	No Change	
Н	Н	Н	Χ	No Change	
Н	Н	$\overline{}$	Χ	No CI	nange

*Both outputs will remain high as long as Set and Reset are low, but the output states are unpredictable if Set and Reset go high simultaneously.

ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	-0.5 to +7.0	V
V _{in}	DC Input Voltage (Referenced to GND)	-0.5 to V _{CC} + 0.5	V
V _{out}	DC Output Voltage (Referenced to GND)	-0.5 to V _{CC} + 0.5	V
I _{in}	DC Input Current, per Pin	±20	mA
I _{out}	DC Output Current, per Pin	±25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±50	mA
P _D	Power Dissipation in Still Air SOIC Package†	500	mW
T _{stg}	Storage Temperature	- 65 to + 150	°C
TL	Lead Temperature, 1 mm from Case for 10 Seconds	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

†Derating: SOIC Package: -7 mW/°C from 65° to 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range GND \leq (V_{in} or V_{out}) \leq V_{CC} .

Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or $V_{\rm CC}$). Unused outputs must be left open.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage (Referenced to GND)	4.5	5.5	V
V _{in} , V _{out}	DC Input Voltage, Output Voltage (Referenced to GND)	0	V _{CC}	V
T _A	Operating Temperature, All Package Types	- 55	+125	°C
t _r , t _f	Input Rise and Fall Time (Figure 1)	0	500	ns

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (Voltages Referenced to GND)

				Gua	aranteed Li	imit	
Symbol	Parameter	Test Conditions	V _{CC} V	–55 to 25°C	≤ 85 ° C	≤ 125°C	Unit
V _{IH}	Minimum High-Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \le 20 \mu\text{A}$	4.5 5.5	2.0 2.0	2.0 2.0	2.0 2.0	V
V _{IL}	Maximum Low–Level Input Voltage	$V_{out} = 0.1 \text{ V or } V_{CC} - 0.1 \text{ V}$ $ I_{out} \le 20 \mu\text{A}$	4.5 5.5	0.8 0.8	0.8 0.8	0.8 0.8	V
V _{OH}	Minimum High-Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \le 20 \mu A$	4.5 5.5	4.4 5.4	4.4 5.4	4.4 5.4	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \le 4.0 \text{ mA}$	4.5	3.98	3.84	3.7	
V _{OL}	Maximum Low–Level Output Voltage	$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \le 20 \mu A$	4.5 5.5	0.1 0.1	0.1 0.1	0.1 0.1	V
		$V_{in} = V_{IH} \text{ or } V_{IL}$ $ I_{out} \le 4.0 \text{ mA}$	4.5	0.26	0.33	0.4	
l _{in}	Maximum Input Leakage Current	V _{in} = V _{CC} or GND	5.5	± 0.1	± 1.0	± 1.0	μΑ
I _{CC}	Maximum Quiescent Supply Current (per Package)	$V_{in} = V_{CC}$ or GND $I_{out} = 0 \mu A$	5.5	2.0	20	80	μΑ
ΔI_{CC}	Additional Quiescent Supply Current	V _{in} = 2.4 V, Any One Input V _{in} = V _{CC} or GND, Other Inputs		≥ -55 °C	25°C	to 125°C	
		$I_{out} = 0 \mu A$	5.5	2.9		2.4	mA

AC ELECTRICAL CHARACTERISTICS (V_{CC} = $5.0~V \pm 10\%$, C_L = 50~pF, Input $t_r = t_f = 6.0~ns$)

		Gı	Guaranteed Limit		
Symbol	Parameter	–55 to 25°C	≤ 85 °C	≤ 125°C	Unit
f _{max}	Maximum Clock Frequency (50% Duty Cycle) (Figures 1 and 4)	30	24	20	MHz
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Clock to Q or Q (Figures 1 and 4)	24	30	36	ns
t _{PLH} , t _{PHL}	Maximum Propagation Delay, Set or Reset to Q or $\overline{\mathbb{Q}}$ (Figures 2 and 4)	24	30	36	ns
t _{TLH} , t _{THL}	Maximum Output Transition Time, Any Output (Figures 1 and 4)	15	19	22	ns
C _{in}	Maximum Input Capacitance	10	10	10	pF

		Typical @ 25°C, V _{CC} = 5.0 V	
C_{PD}	Power Dissipation Capacitance (Per Enabled Output)*	32	pF

^{1.} Used to determine the no–load dynamic power consumption: $P_D = C_{PD} V_{CC}^2 f + I_{CC} V_{CC}$.

TIMING REQUIREMENTS (V_{CC} = 5.0 V \pm 10%, C_L = 50 pF, Input t_r = t_f = 6.0 ns)

			Guaranteed Limit						
				5 to °C	≤ 85	5°C	≤ 12	25°C	
Symbol	Parameter	Fig.	Min	Max	Min	Max	Min	Max	Units
t _{su}	Minimum Setup Time, Data to Clock	3	15		19		22		ns
t _h	Minimum Hold Time, Clock to Data	3	3		3		3		ns
t _{rec}	Minimum Recovery Time, Set or Reset Inactive to Clock	2	6		8		9		ns
t _w	Minimum Pulse Width, Clock	1	15		19		22		ns
t _w	Minimum Pulse Width, Set or Reset	2	15		19		22		ns
t _r , t _f	Maximum Input Rise and Fall Times	1		500		500		500	ns

ORDERING INFORMATION

Device	Package	Shipping [†]
MC74HCT74ADG	SOIC-14 NB (Pb-Free)	55 Units / Rail
MC74HCT74ADR2G	SOIC-14 NB (Pb-Free)	2500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

SWITCHING WAVEFORMS

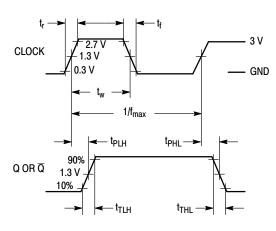


Figure 1.

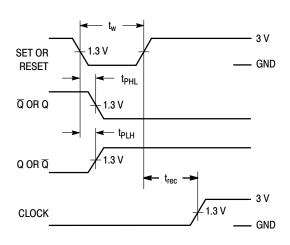


Figure 2.

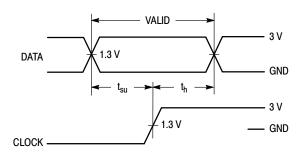
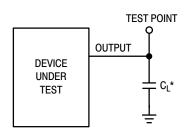


Figure 3.



*Includes all probe and jig capacitance

Figure 5.

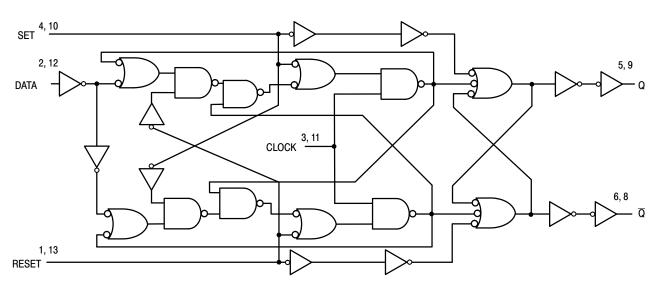


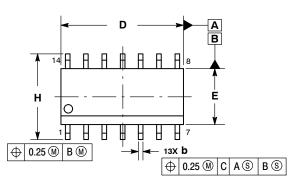
Figure 4. Expanded Logic Diagram

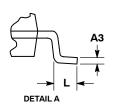


△ 0.10

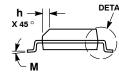
SOIC-14 NB CASE 751A-03 ISSUE L

DATE 03 FEB 2016





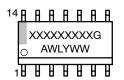




- NOTES:
 1. DIMENSIONING AND TOLERANCING PER
 - ASME Y14.5M, 1994.
 CONTROLLING DIMENSION: MILLIMETERS.
- DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF AT
- MAXIMUM MATERIAL CONDITION.
 DIMENSIONS D AND E DO NOT INCLUDE MOLD PROTRUSIONS.
- 5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE

	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	1.35	1.75	0.054	0.068
A1	0.10	0.25	0.004	0.010
АЗ	0.19	0.25	0.008	0.010
b	0.35	0.49	0.014	0.019
D	8.55	8.75	0.337	0.344
Е	3.80	4.00	0.150	0.157
е	1.27	1.27 BSC		BSC
Н	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.019
L	0.40	1.25	0.016	0.049
M	0 °	7°	0 °	7 °

GENERIC MARKING DIAGRAM*

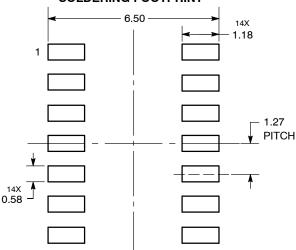


XXXXX = Specific Device Code Α = Assembly Location

WL = Wafer Lot Υ = Year WW = Work Week G = Pb-Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator. "G" or microdot " ■". may or may not be present.

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

C SEATING PLANE

STYLES ON PAGE 2

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^{*}For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

SOIC-14 CASE 751A-03 ISSUE L

DATE 03 FEB 2016

STYLE 1: PIN 1. COMMON CATHODE 2. ANODE/CATHODE 3. ANODE/CATHODE 4. NO CONNECTION 5. ANODE/CATHODE 6. NO CONNECTION 7. ANODE/CATHODE 8. ANODE/CATHODE 9. ANODE/CATHODE 10. NO CONNECTION 11. ANODE/CATHODE 12. ANODE/CATHODE 13. NO CONNECTION 14. COMMON ANODE	STYLE 2: CANCELLED	STYLE 3: PIN 1. NO CONNECTION 2. ANODE 3. ANODE 4. NO CONNECTION 5. ANODE 6. NO CONNECTION 7. ANODE 8. ANODE 9. ANODE 10. NO CONNECTION 11. ANODE 12. ANODE 13. NO CONNECTION 14. COMMON CATHODE	STYLE 4: PIN 1. NO CONNECTION 2. CATHODE 3. CATHODE 4. NO CONNECTION 5. CATHODE 6. NO CONNECTION 7. CATHODE 8. CATHODE 9. CATHODE 10. NO CONNECTION 11. CATHODE 12. CATHODE 13. NO CONNECTION 14. COMMON ANODE
STYLE 5: PIN 1. COMMON CATHODE 2. ANODE/CATHODE 3. ANODE/CATHODE 4. ANODE/CATHODE 5. ANODE/CATHODE 6. NO CONNECTION 7. COMMON ANODE 8. COMMON CATHODE 9. ANODE/CATHODE 10. ANODE/CATHODE 11. ANODE/CATHODE 12. ANODE/CATHODE 13. NO CONNECTION 14. COMMON ANODE	STYLE 6: PIN 1. CATHODE 2. CATHODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE 7. CATHODE 8. ANODE 9. ANODE 10. ANODE 11. ANODE 12. ANODE 13. ANODE 14. ANODE	STYLE 7: PIN 1. ANODE/CATHODE 2. COMMON ANODE 3. COMMON CATHODE 4. ANODE/CATHODE 5. ANODE/CATHODE 6. ANODE/CATHODE 7. ANODE/CATHODE 8. ANODE/CATHODE 9. ANODE/CATHODE 10. ANODE/CATHODE 11. COMMON CATHODE 12. COMMON ANODE 13. ANODE/CATHODE 14. ANODE/CATHODE	STYLE 8: PIN 1. COMMON CATHODE 2. ANODE/CATHODE 3. ANODE/CATHODE 4. NO CONNECTION 5. ANODE/CATHODE 6. ANODE/CATHODE 7. COMMON ANODE 8. COMMON ANODE 9. ANODE/CATHODE 10. ANODE/CATHODE 11. NO CONNECTION 12. ANODE/CATHODE 13. ANODE/CATHODE 14. COMMON CATHODE

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