



PRODUCT / PROCESS CHANGE NOTIFICATION

PCN-000257

Date: July 7 2014

P1/2

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-

Change Details

Part Number(s) Affected:

GS3440-INE3, GS3440-INTE3, GS3440-INTE3Z

GS3441-INE3, GS3441-INTE3, GS3441-INTE3Z

BMD-6EQ02, BMD-6EQ02-TE3, BMD-6EQ02-TE3Z

GV8601AINE3

Customer Part Number(s) Affected: N/A

Description, Purpose and Effect of Change:

New Primary Source for Wafer Sort

Wafer sort is currently performed at ASE-SG (Singapore). Semtech is transitioning wafer sort to KYEC in Taiwan as a new primary test location. KYEC is currently a qualified test supplier for Semtech products.

Upon approval of the PCN, Semtech's wafer sort will be done at KYEC, with ASE-SG remaining as a secondary source.

The test coverage, test platform, and inspection criteria will remain unchanged.

Production Flow	Wafer Sort	Final Electrical Test
Current Flow	ASE-SG	ASE-M
Future Flow	KYEC (or ASE-SG as 2 nd source)	ASE-M

Change Classification	<input type="checkbox"/> Major <input checked="" type="checkbox"/> Minor	Impact to Form, Fit, Function	<input type="checkbox"/> Yes <input checked="" type="checkbox"/> No
Impact to Data Sheet	<input type="checkbox"/> Yes <input checked="" type="checkbox"/> No	New Revision or Date	<input checked="" type="checkbox"/> N/A

Impact to Performance, Characteristics or Reliability:

The customer will experience no change to the form, fit, function, quality, reliability, or test coverage of the final product. No critical parameters are affected by this change. There are no other changes included in this PCN besides the wafer sort change.

This PCN is for information purposes only. The only action required for the customer is to review supporting documents and provide written acceptance of this change to Semtech SIPG Division.



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Date: July 7 2014

P2/2

Implementation Date	August 7, 2014	Work Week	32
Last Time Ship (LTS) Of unchanged product	N/A	Affecting Lot No. / Serial No. (SN)	See chart below.
Sample Availability	YES	Qualification Report Availability	Available

Sample Lots:

ASE_LOT_NO	PKG	LC	ISSUE_QTY	CSOD	PO #	LOT #	DEVICE_TYPE
L11GN18E	QFN	16	3708	20140404	5500003825	110457.1	BMD-6EQ02
L11GN17E	QFN	24	1473	20140404	5500003825	110456.1	GS3441-INE3
L11GN19E	QFN	16	1462	20140404	5500003825	110498.1	GS3440-INE3
L11GN20E	QFN	16	1497	20140404	5500003825	110499.1	GV8601AINE3

Supporting Documents for Change Validation/Attachments:

- *GS6042_BMD6EQ02_GS3440_WaferProbeTesterMigration_Jan2014_ExternalDocument.docx*. – Qualification report containing the results and conclusions from the execution of the qualification plan. (CUSTDOC000147)

Issuing Authority

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**KYEC & ASE (SG)
Wafer Probe Qualification Report for
BMD6EQ02, GS6042 & GS3440
(Verigy Tester)**

CUSTDOC000147



Revision History

Version	ECO	Date	Modifications / Changes	Author
0	ECO-017416	January 14 th , 2014	Initial release	Kasia Wtorek



Contents

- Revision History 2
- Contents 3
- 1 Executive Summary 4
- 2 Process Changes 4
 - 2.1 Process Change Summary 4
 - 2.2 Products Affected 4
 - 2.3 Qualification Approach 4
- 3 Data Analysis Methods 5
 - 3.1 Datalogs 5
 - 3.2 Average Difference between KYEC and ASE-SG 5
 - 3.3 Average Shift as a Percentage of Limits 5
 - 3.4 StdDev Comparison 5
 - 3.5 Parametric Correlation 6
 - 3.6 Histogram Comparison 6
 - 3.7 Yield & BIN Comparison 6
- 4 Conclusion 6



1 Executive Summary

To both improve security of supply and increase supply chain efficiency, KYEC is under consideration as a primary source for wafer probe of the BMD-6EQ02 and the GS3440-INE3. The wafers are currently probed at ASE-SG.

After reviewing mean and standard deviations at KYEC, and after comparing yield & BIN results, and parametric correlation analysis, KYEC is qualified as a primary source for wafer probe of these devices listed above, with ASE-SG retained as 2nd source.

2 Process Changes

2.1 Process Change Summary

Semtech and our supply chain partners are implementing Semtech's wafer probe at King Yuan Electronics Corporation in Taiwan (henceforth known as KYEC) to both improve security of supply and increase supply chain efficiency. The Verigy tester has been previously qualified at ASEM Singapore (henceforth known as ASE-SG).

This report details the correlation analysis and process verification performed to qualify the Verigy tester at KYEC as compared to the Verigy tester at ASE-SG for testing of products which listed in products affected section.

2.2 Products Affected

DEVICE NAME	BMD-6EQ02	GS3440-INE3
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2.3 Qualification Approach

Based on test program coverage and the exercise of all tester instruments, as well as similar functionality of the products listed in Section 1.2, the BMD-6EQ02 wafer was selected as the qualification vehicle for both the GS3440-INE3 and the BMD-6EQ02. Foundry Lot J49188, Wafer #9 was selected for qualification.

Qualification method was as follows: Half of the wafer was tested at ASE-SG (including fuse-burning), and then the full wafer was tested at KYEC (burning the remaining fuses and measuring the fuses that had previously been burnt at ASE-SG). In total 2,349 die were tested at ASE-SG and 4,687 die at KYEC.

Therefore in total 2,349 die were used to calculate the means and standard deviations, except for trim settings, in which case the initial 2,349 die's trim data at ASE-SG were compared to trim data of the remaining 2,338 fresh die tested at KYEC.

The product wafers were tested using the respective Verigy testers at ASE-SG and KYEC. The same tester hardware (production probe card, load board) and production test program were used at both locations.

3 Data Analysis Methods

The general analysis plan was:

1. Calculate the average difference on a per-part basis using XY coordinates.
2. Compare the average difference a percentage of limit range.
3. Compare differences in standard deviation at both locations as a percentage of limit range.
4. Generate a parametric correlation and review parameters where either $R_{sq} < 90\%$ OR #2 and #3 above are anomalous.
5. Visually compare individual test histograms to ensure consistent distributions.
6. Analyze yield and BIN differences in the two datasheets, focusing on
 - a. Die that pass at KYEC but failed at ASE-SG.

3.1 Datalogs

The data from ASE-SG and KYEC was uploaded to Semtech's Test Data Server. The test data was then compared to ensure tester-to-tester correlation.

3.2 Average Difference between KYEC and ASE-SG

For each parameter in the test program, the difference (Δ_{ave}) was calculated as follows:

$$\Delta_{ave} = \text{value@KYEC} - \text{value@ASE-SG}$$

This was calculated on a per-part basis using XY coordinates. The average difference across the wafer was then calculated. This average was then used in the following sections.

3.3 Average Shift as a Percentage of Limits

Acceptance is achieved if the mean value from the tester at KYEC is within 10% of the mean value from the same tester at the ASE-SG location as it relates to the guard-banded test boundaries. The calculated value is as follows:

$$\frac{\Delta_{ave}}{T_{high} - T_{low}} \leq 10\%$$

Result: All shifts were less than 10% except for two Rterm measurements which were slightly higher at 10.4% and 10.2%. These differences are considered negligible.

3.4 StdDev Comparison

For the standard deviation comparison, acceptance is achieved if the standard deviation from the tester at ASE-SG is within 10% of the standard deviation from the same tester at the KYEC location as it relates to the guard-banded test boundaries. The calculated value is as follows:

$$\frac{|\sigma_{NEW} - \sigma_{REF}|}{T_{high} - T_{low}} \leq 10\%$$

Result: No standard deviation shifts as calculated above showed values > 10%.

3.5 Parametric Correlation

For parametric parameters, correlation is achieved if the correlation coefficient is greater than *90%.

Note: In order to achieve a correlation coefficient >90% the distribution of parametric measurements must be greater than the tester resolution. If a parameter is within the tester resolution for all parts tested and is within the 10% Mean and StdDev, it is said to be acceptable even though the correlation coefficient is <90%.

Result: The majority of tests had good parametric correlation. Those that did not were either digital tests (for which Rsq mathematically cannot be calculated) or were very setup sensitive tests with small measurement values such as leakage, where even though the Rsq is < 90%, the stdev and mean analyses from Sections 3.3 and 3.4 showed shifts much less than 10%.

Therefore all parameters pass this correlation test.

3.6 Histogram Comparison

Each histogram is compared to historic histograms one-to-one and evaluated for anomalies such as multi-modes, skew, and kurtosis.

Result: Distributions at KYEC and ASE-SG are equivalent.

3.7 Yield & BIN Comparison

Overall yields were compared between KYEC and the same tester at ASE-SG.

Result: The yields were comparable.

BINs from KYEC and ASE-SG was compared for each sample, both the common and unique failures are reviewed and analysed. Bin to Bin correlation is achieved if all samples have the same Bin and failure mode on the same tester at both KYEC and ASE-SG.

Result: Bin comparison showed no anomalies between passing/failing parts at ASE-SG and passing/failing parts at KYEC.

4 Conclusion

The Verigy WP solution at KYEC is equivalent to the ASE-SG solution. ASE-SG can be replaced by routing through KYEC without impact to the customer quality. Both locations are deemed qualified for production of the products listed in Section 2.2.

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