12.5 GHz to 16.5 GHz GaAs MMIC I/Q Upconverter

Preliminary Technical Data

HMC9060

FEATURES

- Conversion gain: 15 dB typical
- Sideband rejection: 25 dB typical
- Input power for 1 dB compression (P1dB): 8.5 dBm typical
- Output third-order intercept (OIP3): 32 dBm typical
- LO leakage at the RF output: 2 dBm typical
- LO leakage at the IF input: −18 dBm typical
- RF return loss: 13 dB typical
- LO return loss: 8 dB typical
- 32-lead, 5 mm × 5 mm LFCSP package

APPLICATIONS

- Point to point and point to multipoint radios
- Military radars, electronic warfare (EW), and electronic intelligence (ELINT)
- Satellite communications
- Sensors

GENERAL DESCRIPTION

The HMC9060 is a compact, gallium arsenide (GaAs), pseudomorphic high electron mobility transistors (pHEMT), monolithic microwave integrated circuit (MMIC) upconverter in a RoHS compliant low stress injection molded plastic LFCSP package that operates from 12.5 GHz to 16.5 GHz. This device provides a small signal conversion gain of 15 dB with 25 dBc of sideband rejection. The HMC9060 uses a radio frequency (RF) amplifier preceded by an in-phase/quadrature (I/Q) mixer, where the local oscillator (LO) is driven by a driver amplifier. IF1 and IF2 mixer inputs are provided, and an external 90° hybrid is needed to select the required sideband. The I/Q mixer topology reduces the need for filtering of the unwanted sideband. The HMC9060 is a much smaller alternative to hybrid style single-sideband (SSB) upconverter assemblies, and it eliminates the need for wire bonding by allowing the use of surface-mount manufacturing techniques.

FUNCTIONAL BLOCK DIAGRAM

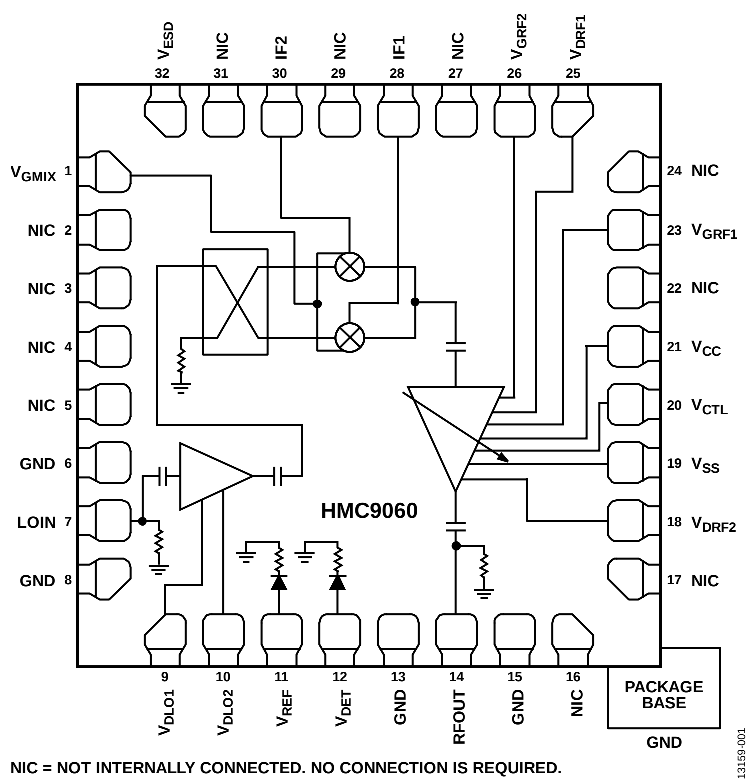

Figure 1.

Rev. PrA Document Feedback

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Technical Support www.analog.com

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SPECIFICATIONS

12.5 GHz TO 14 GHz FREQUENCY RANGE

T_A = 25°C, IF = 1 GHz, V_{DLOx} = 2.4 V, V_{DRFx} = 5 V, V_{CC} = 5 V, V_{CTL} = −6 V, V_{ESD} = −5 V, V_{SS} = −5 V, V_{GMIX} = −0.5 V, LO = 2 dBm. Measurements performed with upper sideband selected and external 90° hybrid at the IF ports, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit
OPERATING CONDITIONS				
Frequency Range				
RF	12.5		14	GHz
LO	9		17.5	GHz
Intermediate Frequency (IF)	DC		3.5	GHz
LO Drive Range	2		8	dBm
PERFORMANCE				
Conversion Gain	11	15		dB
Sideband Rejection	20	25		dBc
Input Power for 1 dB Compression (P1dB)		8.5		dBm
Output Third-Order Intercept (OIP3) at Maximum Gain	29	32		dBm
LO Leakage at RFOUT[1]		2		dBm
LO Leakage at IFx[2]		−18		dBm
Noise Figure		13		dB
Return Loss				
RF		13		dB
LO		8		dB
IFx[2]		20		dB
POWER SUPPLY				
Total Supply Current				
LO Amplifier		100		mA
RF Amplifier[3]		240		mA

[1] The LO signal level at the RF output port is not calibrated.
[2] Measurement taken without 90° hybrid at the IF ports.
[3] Adjust V_{GRF1} and V_{GRF2} between −2 V and 0 V to achieve a total amplifier quiescent drain current = 240 mA.

14 GHz TO 16.5 GHz FREQUENCY RANGE

T_A = 25°C, IF = 1 GHz, V_{DLOx} = 2.4 V, V_{DRFx} = 5 V, V_{CC} = 5 V, V_{CTL} = −6 V, V_{ESD} = −5 V, V_{SS} = −5 V, V_{GMIX} = −0.5 V, LO = 2 dBm. Measurements performed with upper sideband selected and external 90° hybrid at the IF ports, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit
OPERATING CONDITIONS				
Frequency Range				
RF	14		16.5	GHz
LO	10.5		20	GHz
IF	DC		3.5	GHz
LO Drive Range	2		8	dBm
PERFORMANCE				
Conversion Gain	8	13		dB
Sideband Rejection	15	22		dBc
Input Power for 1 dB Compression (P1dB)		8.5		dBm
Output Third-Order Intercept (OIP3) at Maximum Gain	27	30		dBm
LO Leakage at RFOUT[1]		0		dBm
LO Leakage at IFx		−30		dBm
Noise Figure		15		dB
Return Loss				
RF		20		dB
LO		6		dB
IF		20		dB
POWER SUPPLY				
Total Supply Current				
LO Amplifier		100		mA
RF Amplifier[2]		240		mA

[1] The LO signal level at the RF output port is not suppressed.
[2] Adjust V_{GRF1} and V_{GRF2} between −2 V and 0 V to achieve a total amplifier quiescent drain current = 240 mA.

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Drain Bias Voltage	
V_{DRFx}, V_{DLOx}, V_{CC}, V_{REF}, V_{DET}	5.5 V
Gate Bias Voltage	
V_{GRFx}	−3 V to 0 V
V_{CTL}, V_{ESD}, V_{SS}	−7 V to 0 V
V_{GMIX}	−2 V to 0 V
LO Input Power	10 dBm
IF Input Power	10 dBm
Maximum Junction Temperature	175°C
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
ESD Sensitivity, Human Body Model (HBM)	150 V (Class 0)

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. The θ_{JA} value in Table 4 assume a 4-layer JEDEC standard board with zero airflow.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
32-Lead LFCSP_VQ	43.1	27.3	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

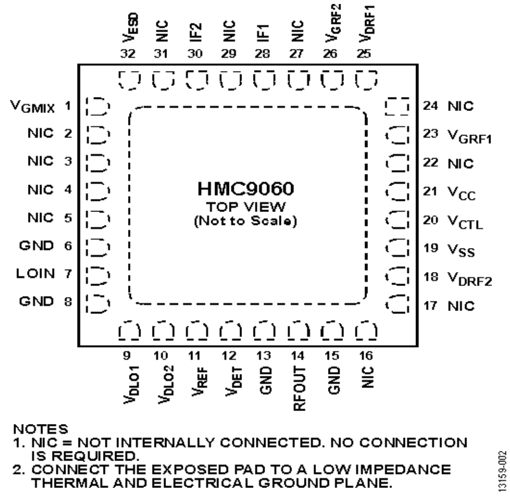

Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V_{GMIX}	Gate Voltage for FET Mixer. See Figure 3. Refer to the typical application circuit for the required external components (see Figure 164).
2, 3, 4, 5, 16, 17, 22, 24, 27, 29, 31	NIC	Not Internally Connected. No connection is required. These pins are not connected internally. However, all data shown herein was measured with these pins connected to RF/dc ground externally.
6, 8, 13, 15	GND	Ground Connect. See Figure 4. These pins and package bottom must be connected to RF/dc ground.
7	LOIN	Local Oscillator Input. See Figure 5. This pin is dc-coupled and matched to 50 Ω.
9, 10	V_{DLO1}, V_{DLO2}	Power Supply Voltage for the Local Oscillator Amplifier. See Figure 6. Refer to the typical application circuit for the required external components (see Figure 164).
11	V_{REF}	Reference Voltage for the Power Detector. See Figure 8. V_{REF} is the dc bias of diode biased through external resistor used for temperature compensation of V_{DET}. Refer to the typical application circuit for the required external components (see Figure 164).
12	V_{DET}	Detector Voltage for the Power Detector. See Figure 7. V_{DET} is the dc voltage representing RF output power rectified by the diode, which is biased through an external resistor. Refer to the typical application circuit for the required external components (see Figure 164).
14	RFOUT	Radio Frequency Output. See Figure 9. This pin is dc-coupled and matched to 50 Ω.
18, 25	V_{DRF2}, V_{DRF1}	Power Supply Voltage for RF Amplifier (see Figure 10). Refer to the typical application circuit for the required external components (see Figure 164).
19	V_{SS}	Gate Voltage for Gain Control Circuitry. See Figure 11. Refer to the typical application circuit for the required external components (see Figure 164).
20	V_{CTL}	Gain Control Voltage for RF Amplifier. See Figure 11. Refer to the typical application circuit for the required external components (see Figure 164).
21	V_{CC}	DC Voltage for Gain Control Circuitry. See Figure 11. Refer to the typical application circuit for the required external components (see Figure 164).
23, 26	V_{GRF1},V_{GRF2}	Gate Voltage for RF Amplifier. See Figure 12. Refer to the typical application circuit for the required external components (see Figure 164).
28, 30	IF1, IF2	Quadrature IF Inputs. See Figure 13. For applications not requiring operation to dc, use an off chip dc blocking capacitor. For operation to dc, these pins must not source/sink more than ±3 mA of current or device malfunction and failure may result.
32	V_{ESD}	DC Voltage for ESD Protection. See Figure 14. Refer to the typical application circuit for the required external components (see Figure 164).
	EPAD	Exposed Pad. Connect the exposed pad to a low impedance thermal and electrical ground plane.

INTERFACE SCHEMATICS

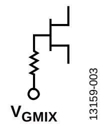

Figure 3. V_{GMIX} Interface

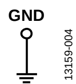

Figure 4. GND Interface

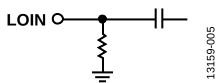

Figure 5. LOIN Interface

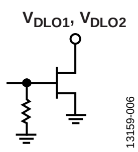

Figure 6. V_{DLO1}, V_{DLO2} Interface

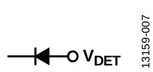

Figure 7. V_{DET} Interface

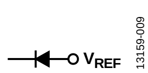

Figure 8. V_{REF} Interface

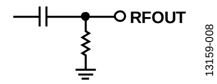

Figure 9. RFOUT Interface

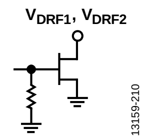

Figure 10. V_{DRF1}, V_{DRF2} Interface

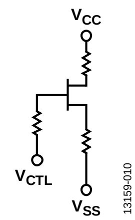

Figure 11. V_{SS}, V_{CTL}, V_{CC} Interface

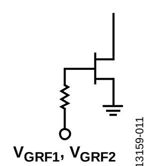

Figure 12. V_{GRF1}, V_{GRF2} Interface

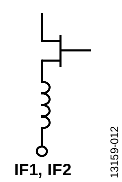

Figure 13. IF1, IF2 Interface

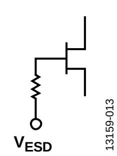

Figure 14. V_{ESD} Interface

TYPICAL PERFORMANCE CHARACTERISTICS

UPPER SIDEBAND SELECTED

Data taken as SSB upconverter with external IF 90° hybrid at the IF ports, IF = 1 GHz.

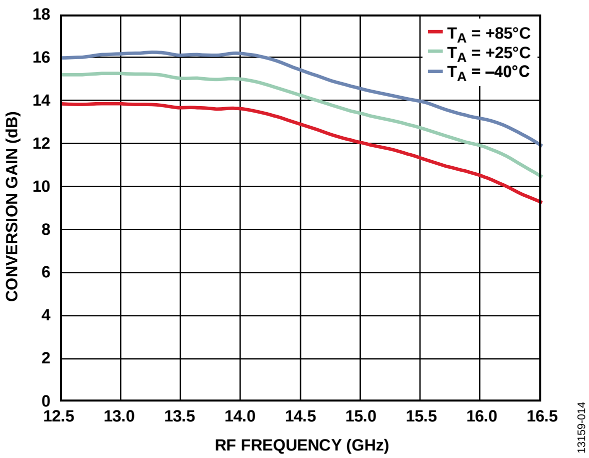

Figure 15. Conversion Gain vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 2.4 V

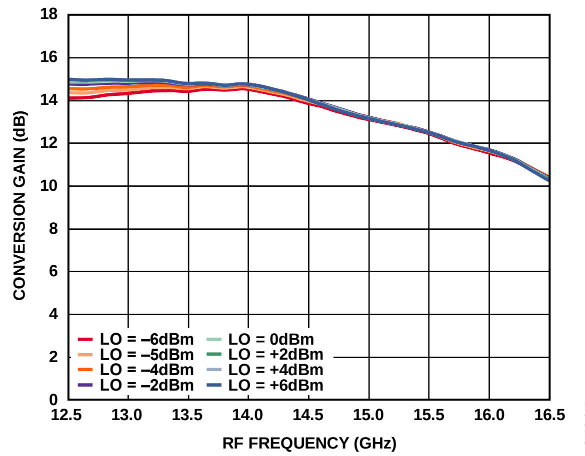

Figure 18. Conversion Gain vs. RF Frequency at Various LO Powers, V_{DLOx} = 2.4 V

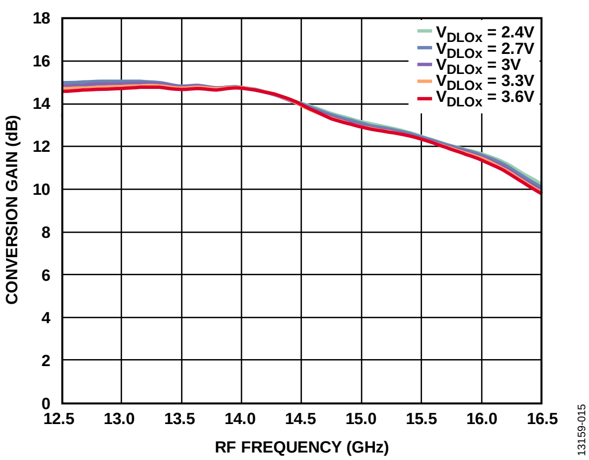

Figure 16. Conversion Gain vs. RF Frequency at Various V_{DLOx}, LO = 2 dBm

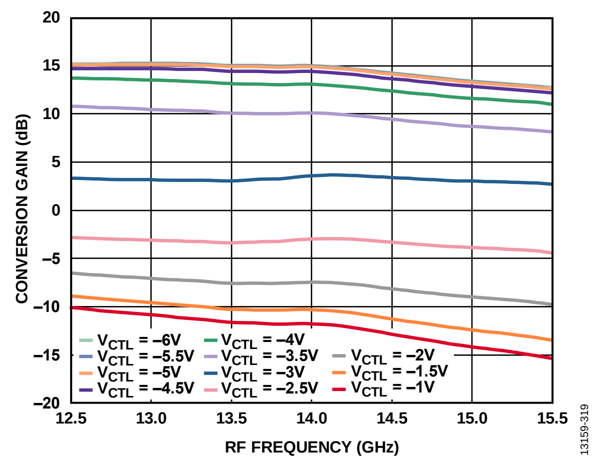

Figure 19. Conversion Gain vs. RF Frequency at Various Control Voltages, LO = 2 dBm, V_{DLOx} = 2.4 V

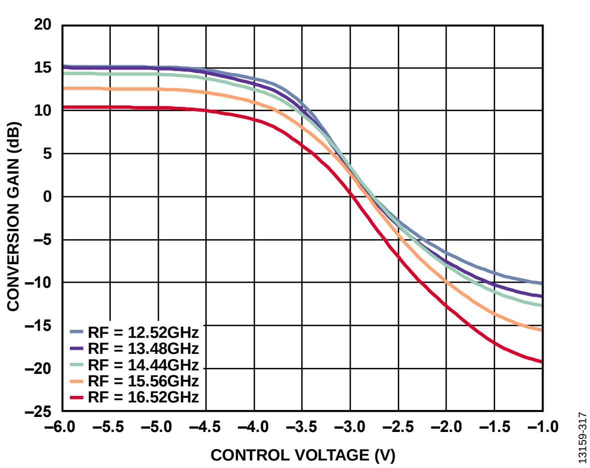

Figure 17. Conversion Gain vs. Control Voltage at Various RF Frequencies, LO = 2 dBm, V_{DLOx} = 2.4 V

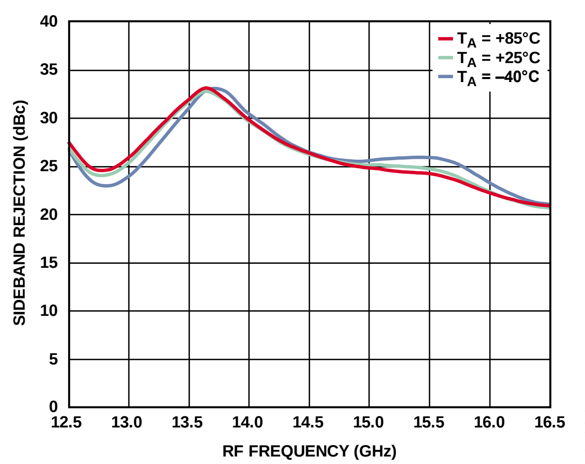

Figure 20. Sideband Rejection vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 2.4 V

Data taken as SSB upconverter with external IF 90° hybrid at the IF ports, IF = 1 GHz.

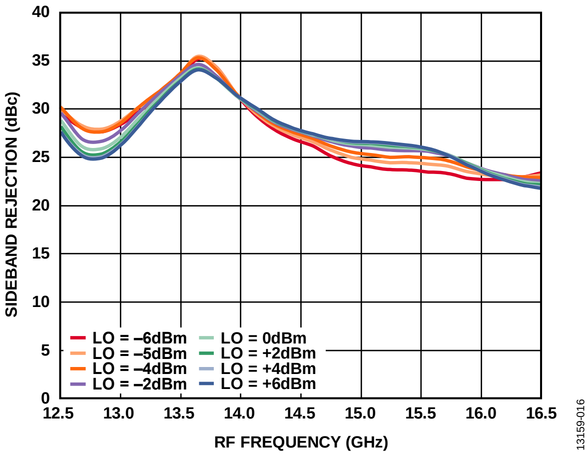

Figure 21. Sideband Rejection vs. RF Frequency at Various LO Powers, V_{DLOx} = 2.4 V

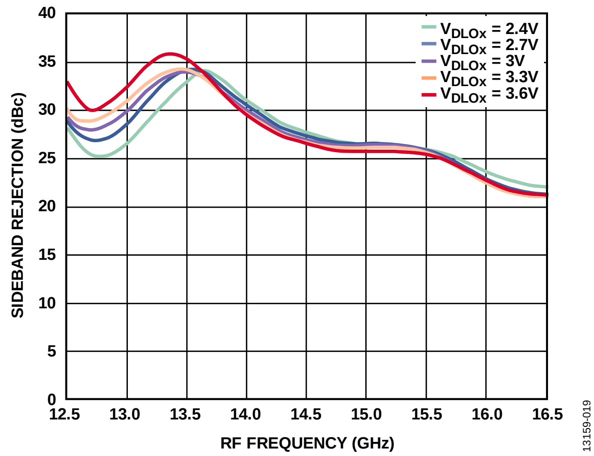

Figure 24. Sideband Rejection vs. RF Frequency at Various V_{DLOx}, LO = 2 dBm

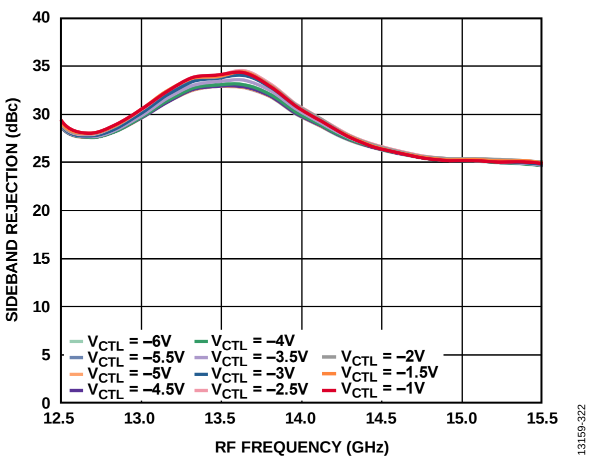

Figure 22. Sideband Rejection vs. RF Frequency at Various Control Voltages, LO = 2 dBm, V_{DLOx} = 2.4 V

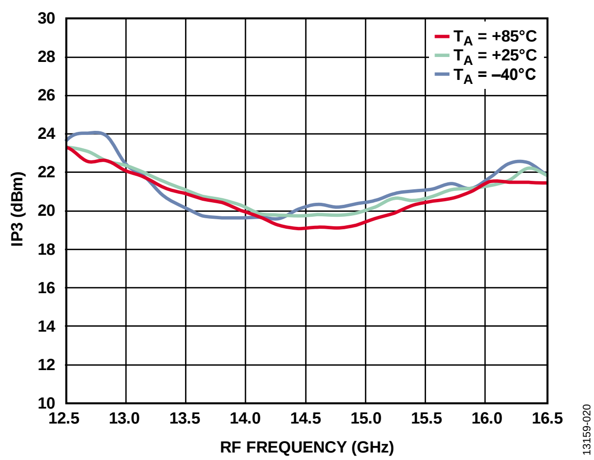

Figure 25. Input IP3 vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 2.4 V

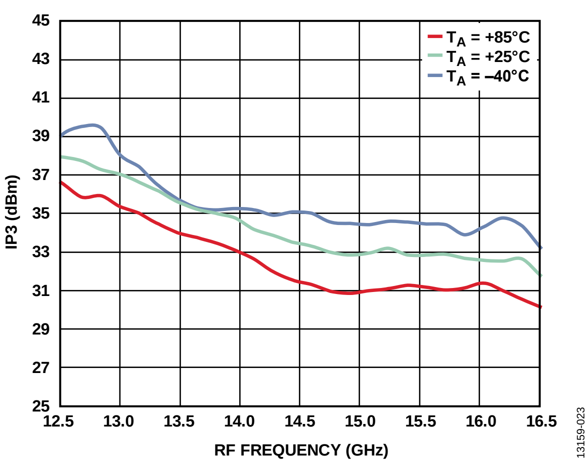

Figure 23. Output IP3 vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 2.4 V

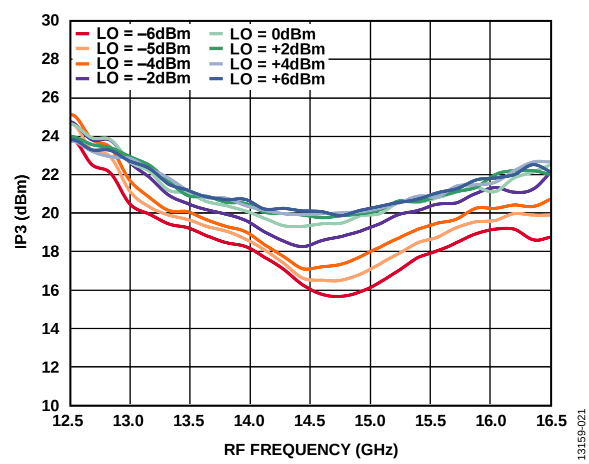

Figure 26. Input IP3 vs. RF Frequency at Various LO Powers, V_{DLOx} = 2.4 V

Data taken as SSB upconverter with external IF 90° hybrid at the IF ports, IF = 1 GHz.

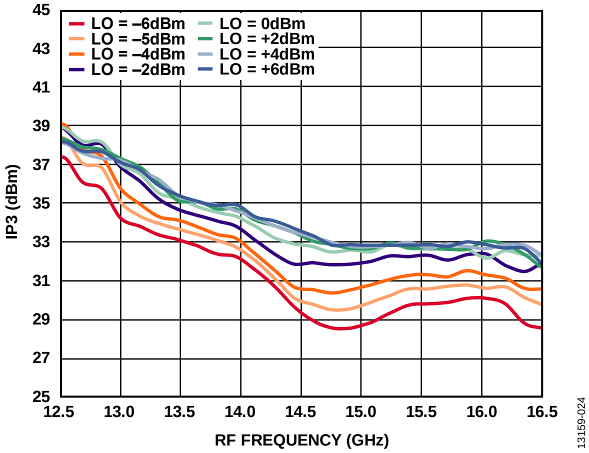

Figure 27. Output IP3 vs. RF Frequency at Various LO Powers, V_{DLOx} = 2.4 V

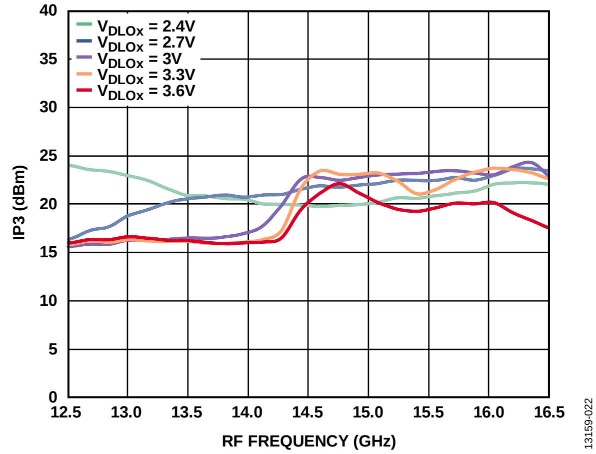

Figure 30. Input IP3 vs. RF Frequency at Various V_{DLOx}, LO = 2 dBm

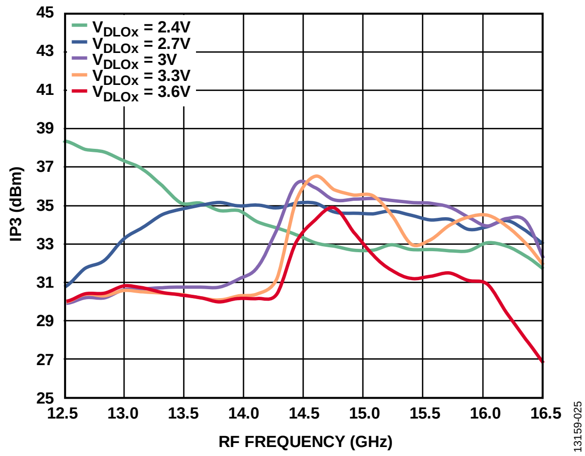

Figure 28. Output IP3 vs. RF Frequency at Various V_{DLOx}, LO = 2 dBm

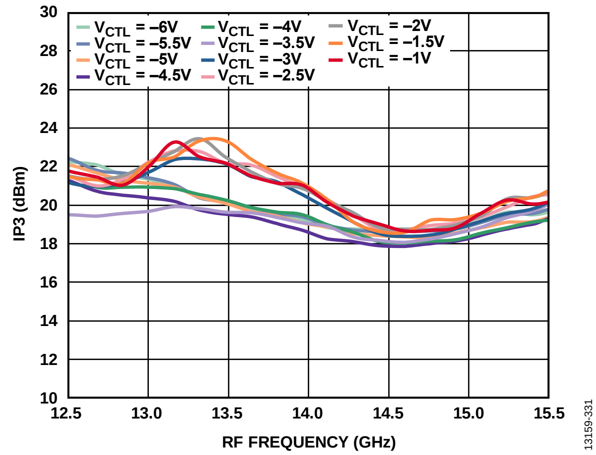

Figure 31. Input IP3 vs. RF Frequency at Various Control Voltages, LO = 2 dBm, V_{DLOx} = 2.4 V

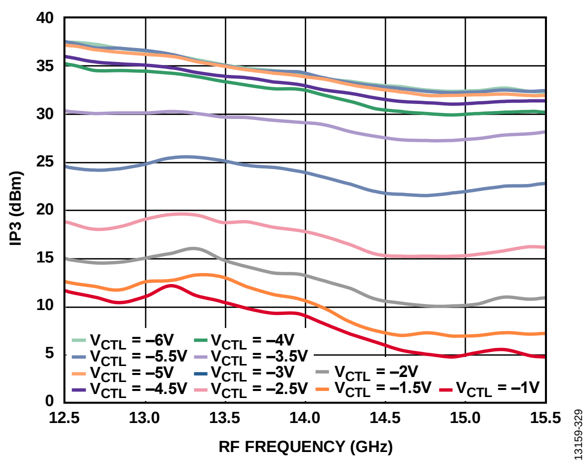

Figure 29. Output IP3 vs. RF Frequency at Various Control Voltages, LO = 2 dBm, V_{DLOx} = 2.4 V

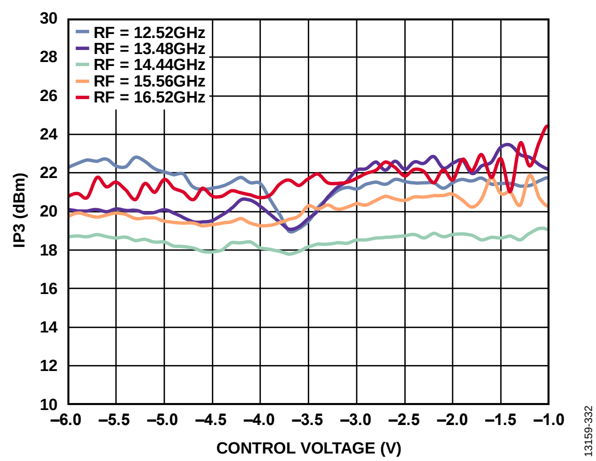

Figure 32. Input IP3 vs. Control Voltage at Various RF Frequencies, LO = 2 dBm, V_{DLOx} = 2.4 V

Data taken as SSB upconverter with external IF 90° hybrid at the IF ports, IF = 1 GHz.

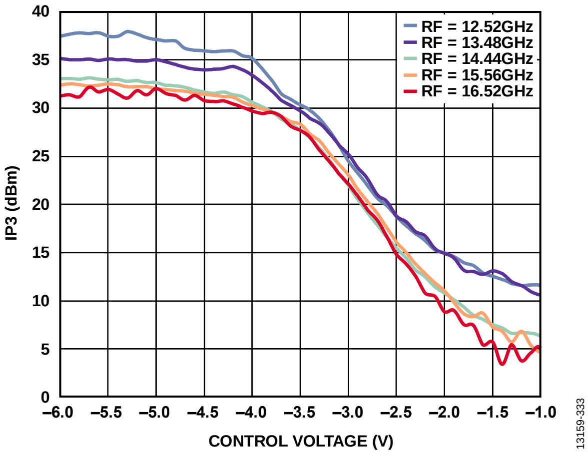

Figure 33. Output IP3 vs. Control Voltage at Various RF Frequencies, LO = 2 dBm, V_{DLOx} = 2.4 V

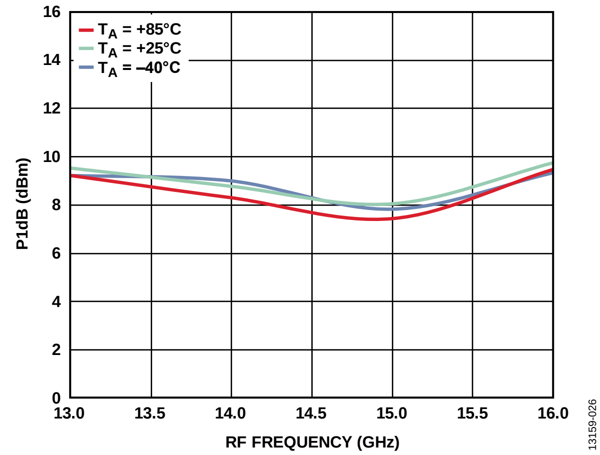

Figure 35. Input P1dB vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 2.4 V

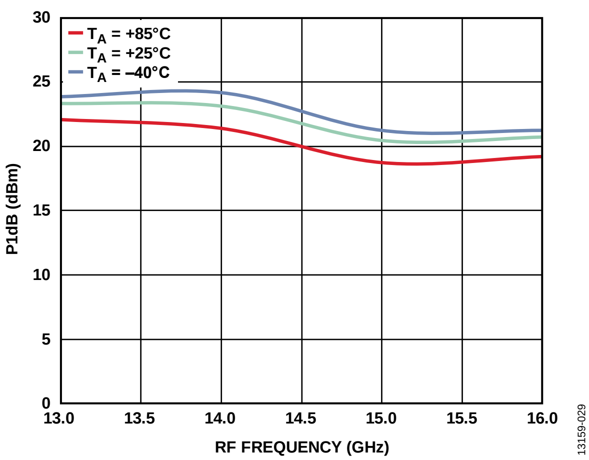

Figure 34. Output P1dB vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 2.4 V

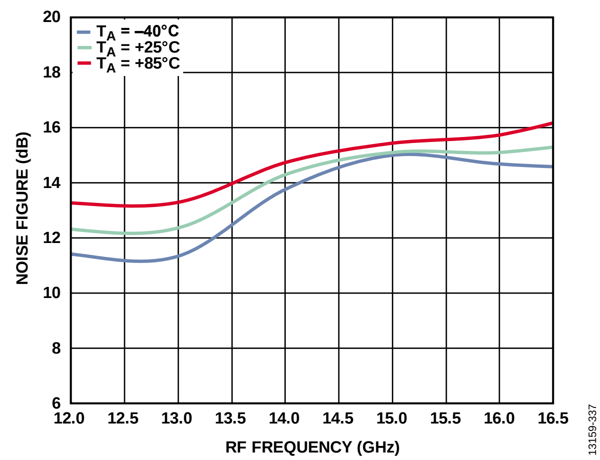

Figure 36. Noise Figure vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 2.4 V

Data taken as SSB upconverter with external IF 90° hybrid at the IF ports, IF = 2 GHz.

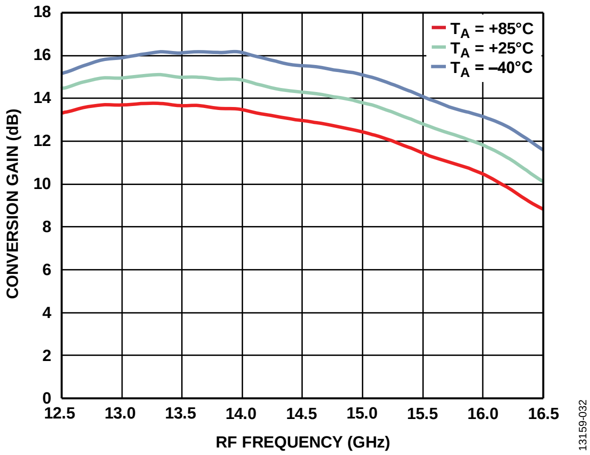

Figure 37. Conversion Gain vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 2.4 V

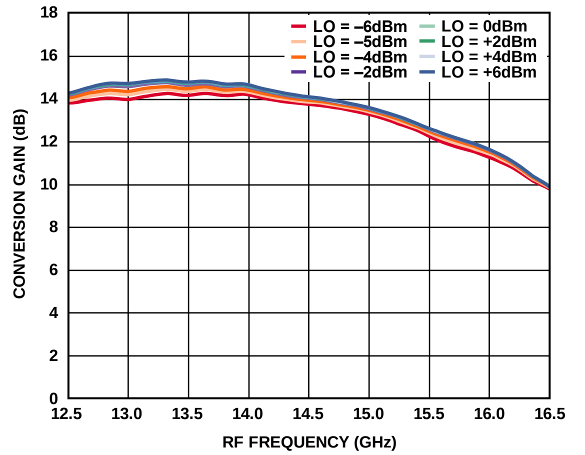

Figure 40. Conversion Gain vs. RF Frequency at Various LO Powers, V_{DLOx} = 2.4 V

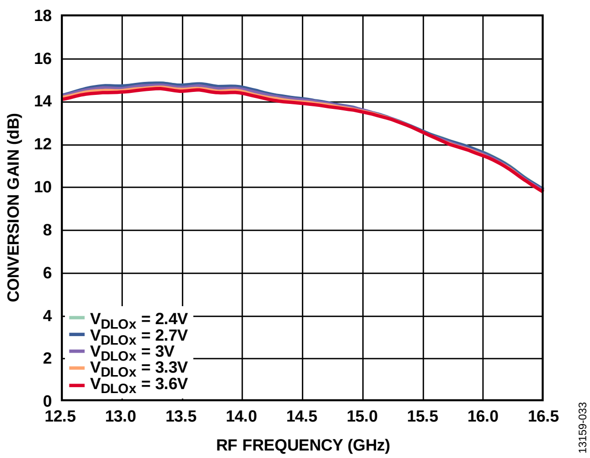

Figure 38. Conversion Gain vs. RF Frequency at Various V_{DLOx}, LO = 2 dBm

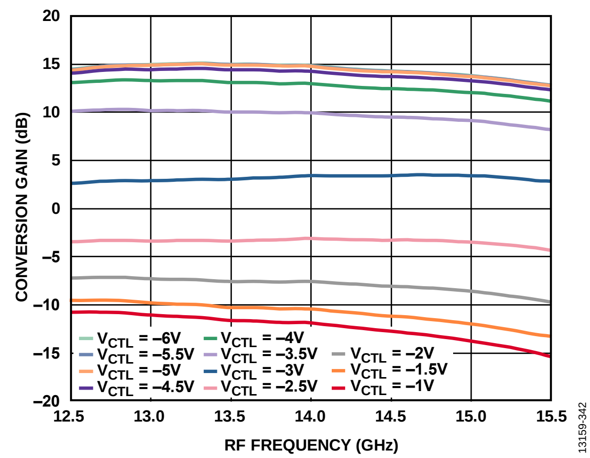

Figure 41. Conversion Gain vs. RF Frequency at Various Control Voltages, LO = 2 dBm, V_{DLOx} = 2.4 V

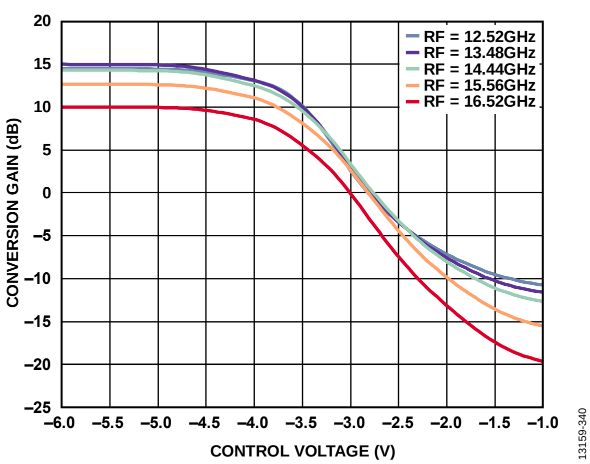

Figure 39. Conversion Gain vs. Control Voltage at Various RF Frequencies, LO = 2 dBm, V_{DLOx} = 2.4 V

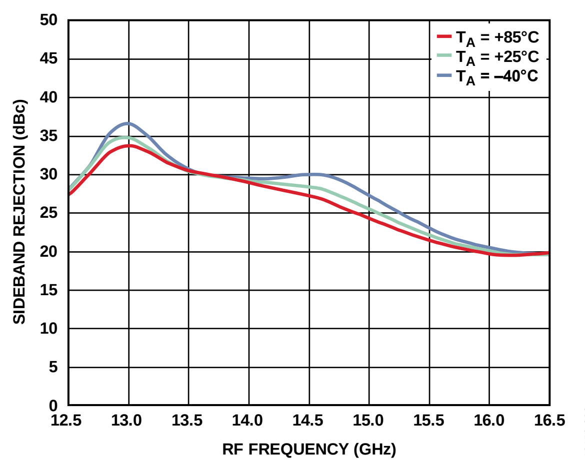

Figure 42. Sideband Rejection vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 2.4 V

Data taken as SSB upconverter with external IF 90° hybrid at the IF ports, IF = 2 GHz.

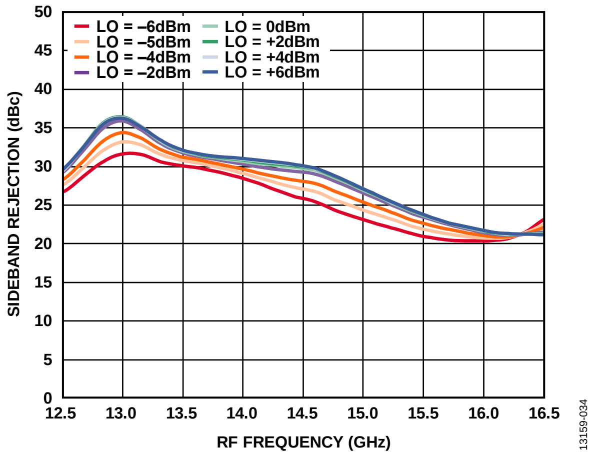

Figure 43. Sideband Rejection vs. RF Frequency at Various LO Powers, V_{DLOx} = 2.4 V

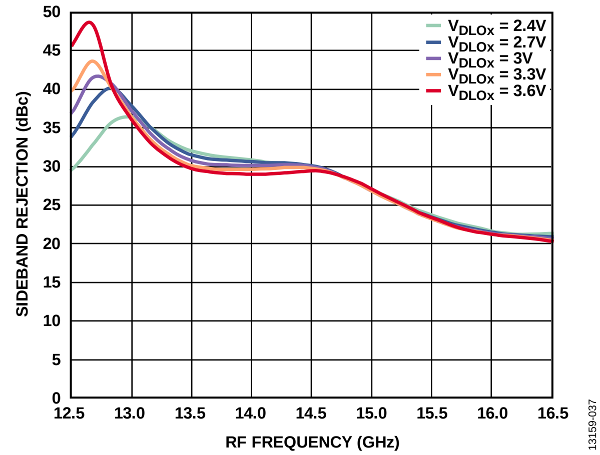

Figure 46. Sideband Rejection vs. RF Frequency at Various V_{DLOx}, LO = 2 dBm

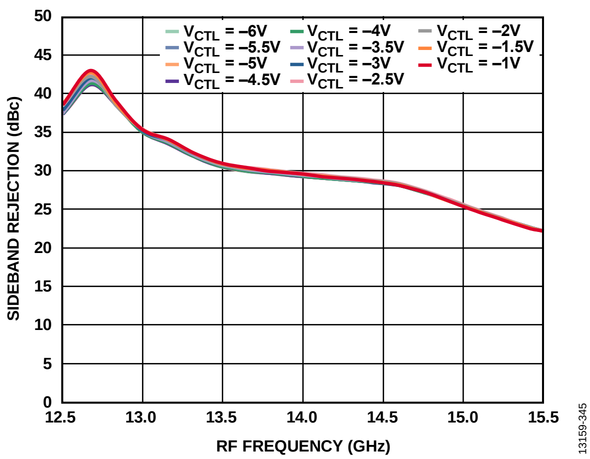

Figure 44. Sideband Rejection vs. RF Frequency at Various Control Voltages, LO = 2 dBm, V_{DLOx} = 2.4 V

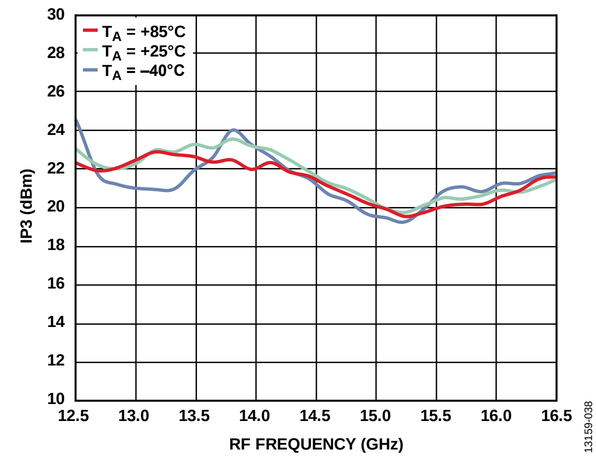

Figure 47. Input IP3 vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 2.4 V

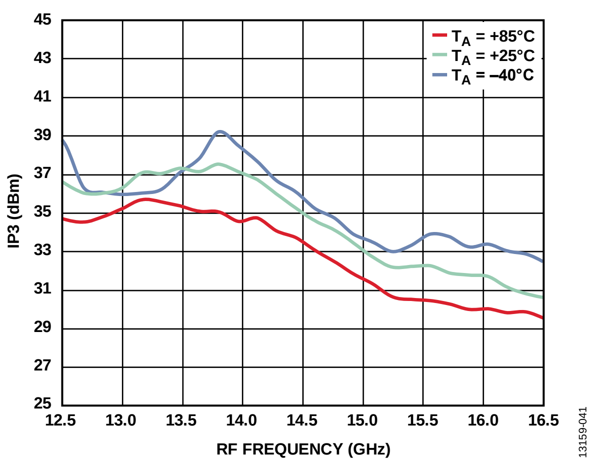

Figure 45. Output IP3 vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 2.4 V

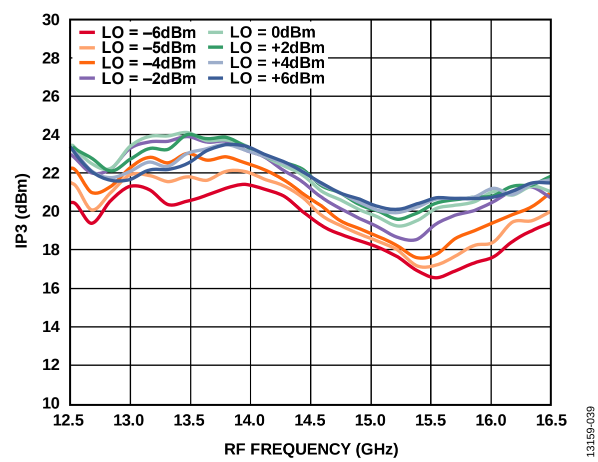

Figure 48. Input IP3 vs. RF Frequency at Various LO Powers, V_{DLOx} = 2.4 V

Data taken as SSB upconverter with external IF 90° hybrid at the IF ports, IF = 2 GHz.

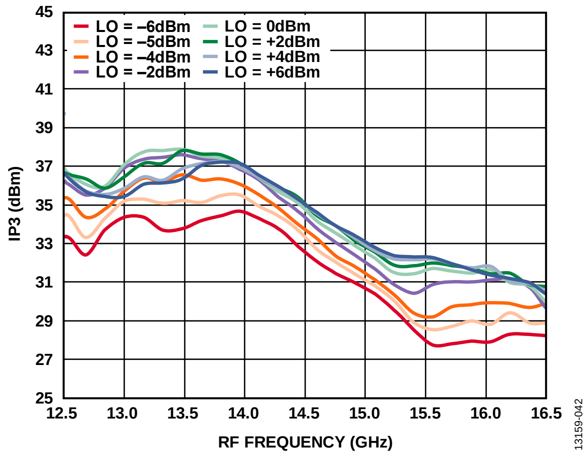

Figure 49. Output IP3 vs. RF Frequency at Various LO Powers, V_{DLOx} = 2.4 V

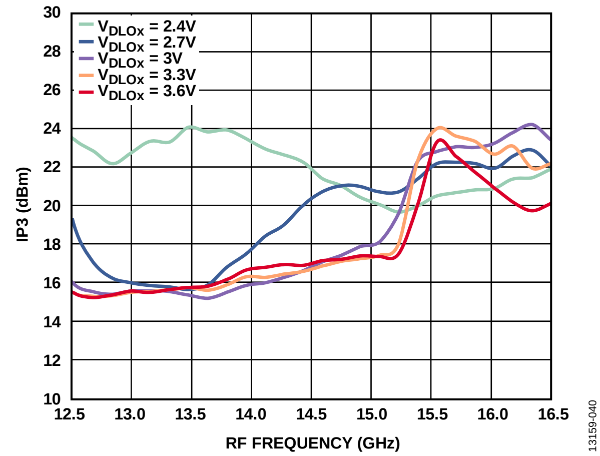

Figure 52. Input IP3 vs. RF Frequency at Various V_{DLOx}, LO = 2 dBm

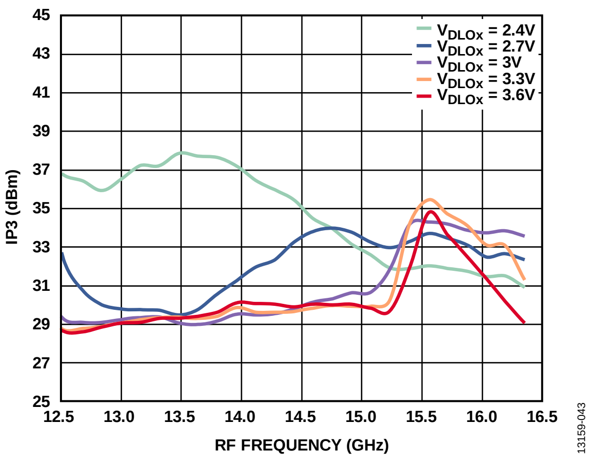

Figure 50. Output IP3 vs. RF Frequency at Various V_{DLOx}, LO = 2 dBm

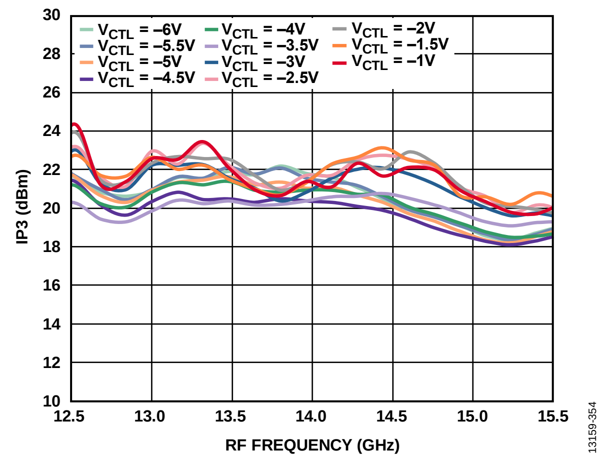

Figure 53. Input IP3 vs. RF Frequency at Various Control Voltages, LO = 2 dBm, V_{DLOx} = 2.4 V

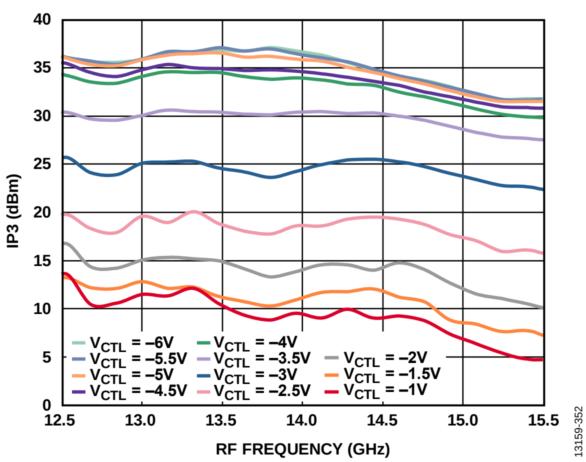

Figure 51. Output IP3 vs. RF Frequency at Various Control Voltages, LO = 2 dBm, V_{DLOx} = 2.4 V

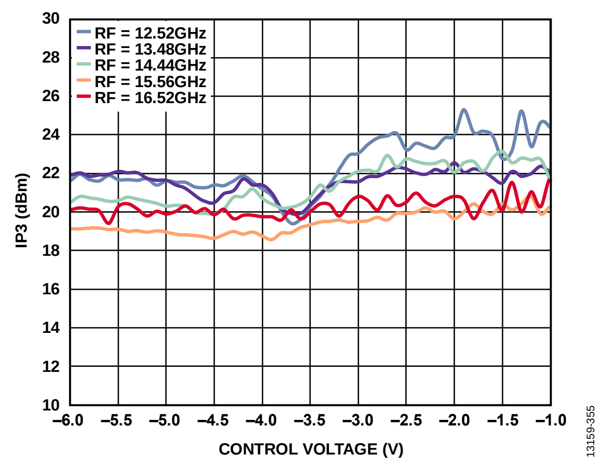

Figure 54. Input IP3 vs. Control Voltage at Various RF Frequencies, LO = 2 dBm, V_{DLOx} = 2.4 V

Data taken as SSB upconverter with external IF 90° hybrid at the IF ports, IF = 2 GHz.

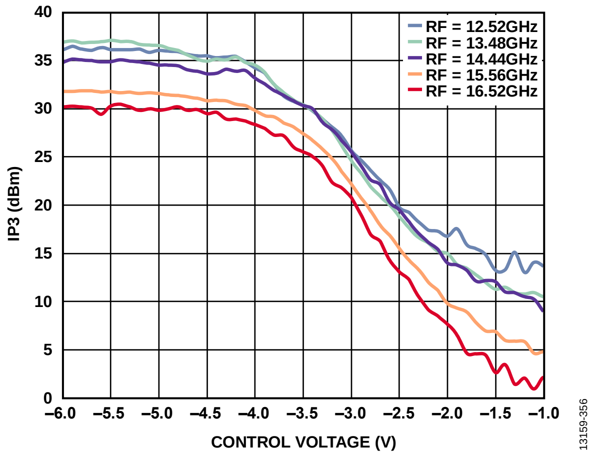

Figure 55. Output IP3 vs. Control Voltage at Various RF Frequencies, LO = 2 dBm, V_{DLOx} = 2.4 V

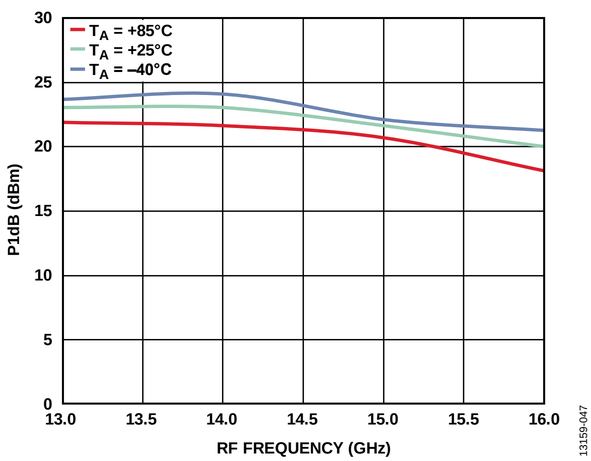

Figure 56. Output P1dB vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 2.4 V

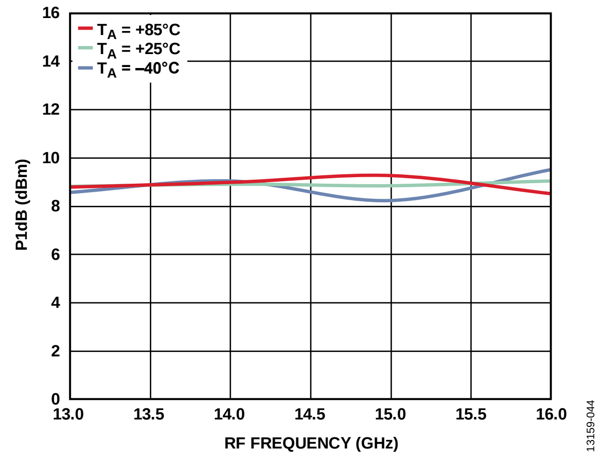

Figure 57. Input P1dB vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 2.4 V

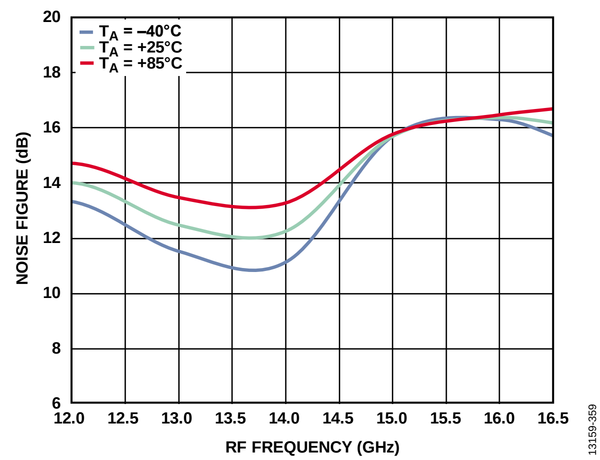

Figure 58. Noise Figure vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 2.4 V

Data taken as SSB upconverter with external IF 90° hybrid at the IF ports, IF = 3 GHz.

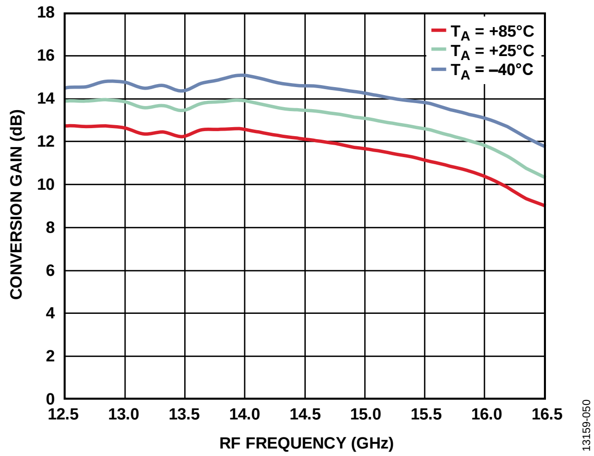

Figure 59. Conversion Gain vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLO1} = 2.4 V

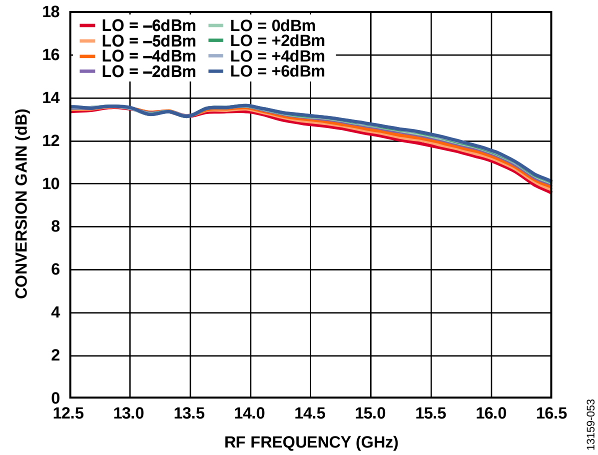

Figure 62. Conversion Gain vs. RF Frequency at Various LO Powers, V_{DLOx} = 2.4 V

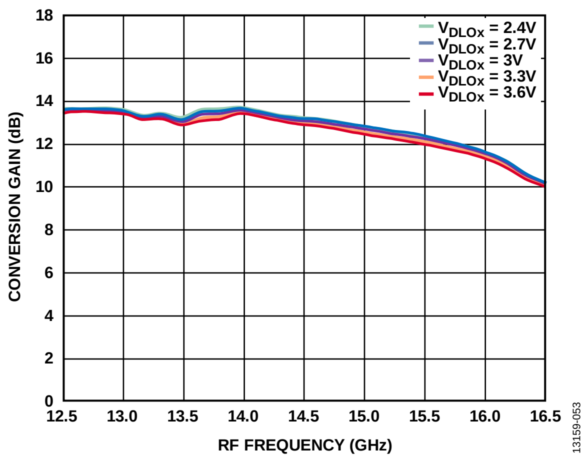

Figure 60. Conversion Gain vs. RF Frequency at Various V_{DLOx}, LO = 2 dBm

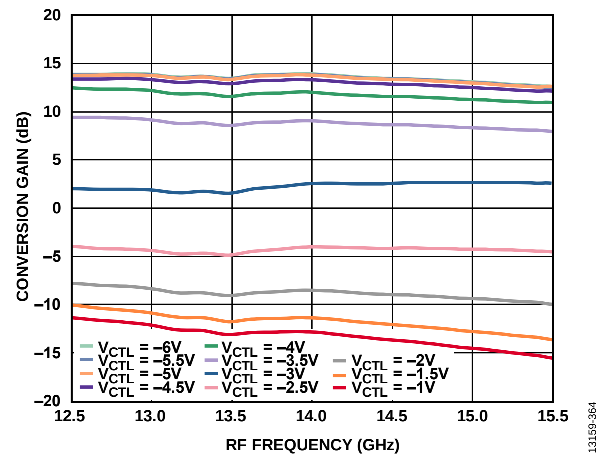

Figure 63. Conversion Gain vs. RF Frequency at Various Control Voltages, LO = 2 dBm, V_{DLOx} = 2.4 V

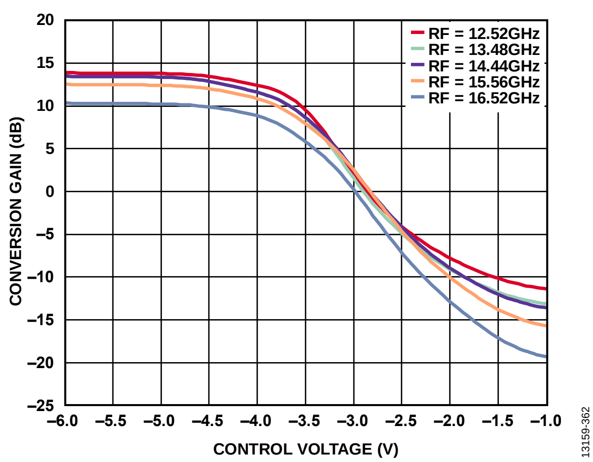

Figure 61. Conversion Gain vs. Control Voltage at Various RF Frequencies, LO = 2 dBm, V_{DLOx} = 2.4 V

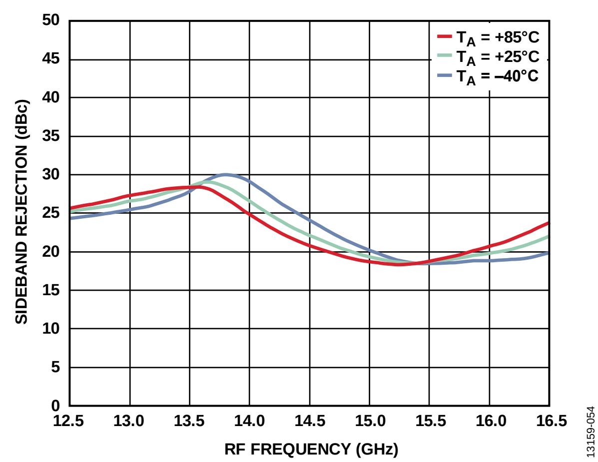

Figure 64. Sideband Rejection vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 2.4 V

Data taken as SSB upconverter with external IF 90° hybrid at the IF ports, IF = 3 GHz.

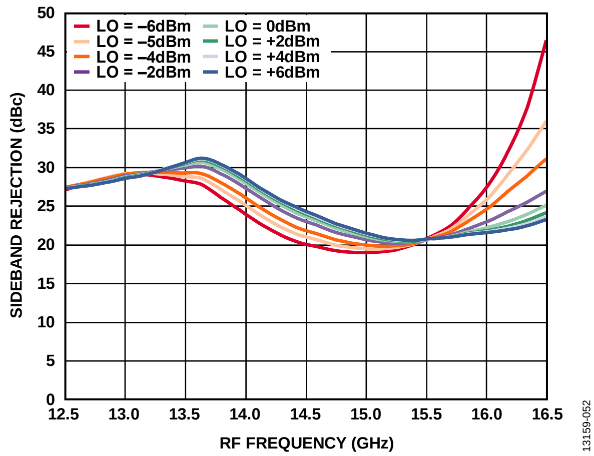

Figure 65. Sideband Rejection vs. RF Frequency at Various LO Powers, V_{DLOx} = 2.4 V

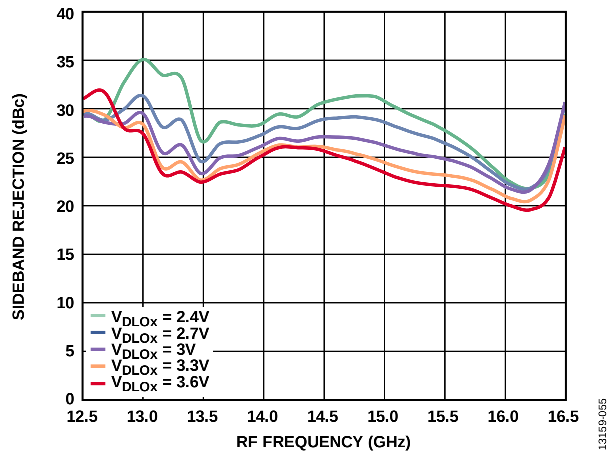

Figure 68. Sideband Rejection vs. RF Frequency at Various V_{DLOx}, LO = 2 dBm

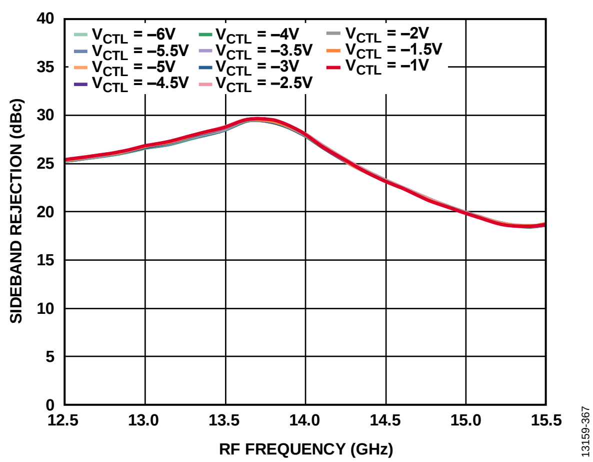

Figure 66. Sideband Rejection vs. RF Frequency at Various Control Voltages, LO = 2 dBm, V_{DLOx} = 2.4 V

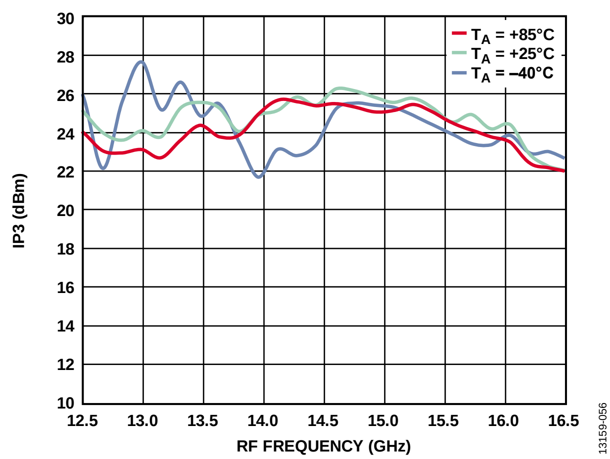

Figure 69. Input IP3 vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 2.4 V

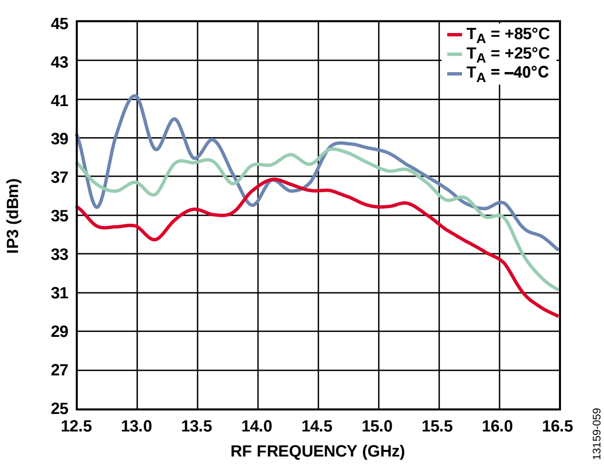

Figure 67. Output IP3 vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 2.4 V

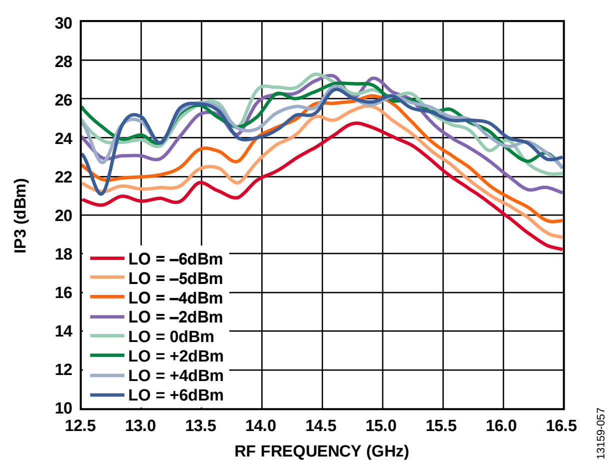

Figure 70. Input IP3 vs. RF Frequency at Various LO Powers, V_{DLOx} = 2.4 V

Data taken as SSB upconverter with external IF 90° hybrid at the IF ports, IF = 3 GHz.

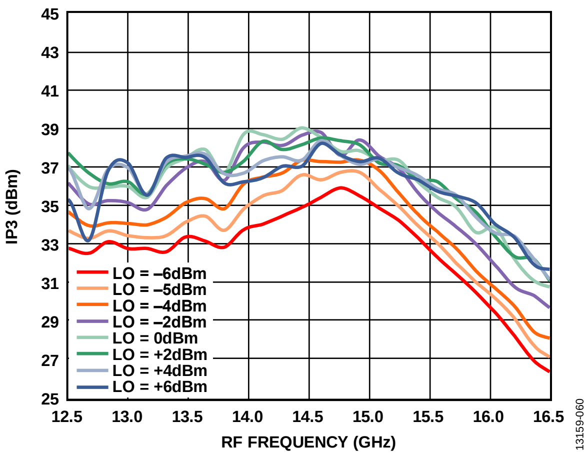

Figure 71. Output IP3 vs. RF Frequency at Various LO Powers, V_{DLOx} = 2.4 V

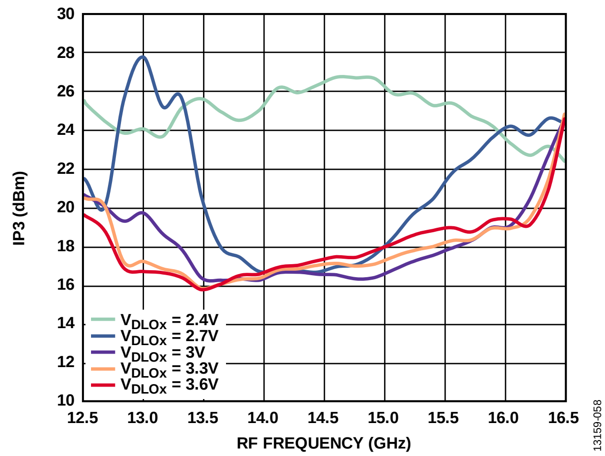

Figure 74. Input IP3 vs. RF Frequency at Various V_{DLOx}, LO = 2 dBm

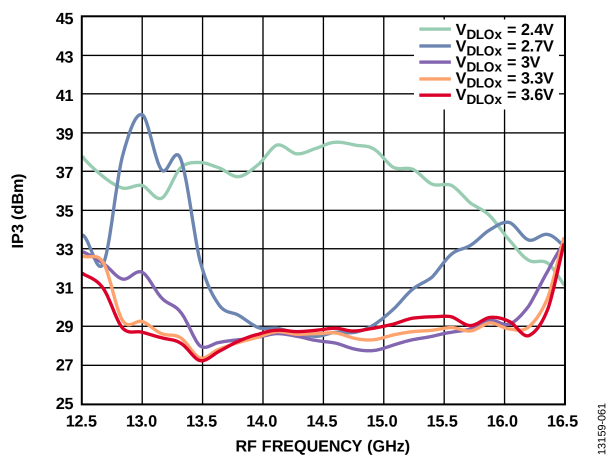

Figure 72. Output IP3 vs. RF Frequency at Various V_{DLOx}, LO = 2 dBm

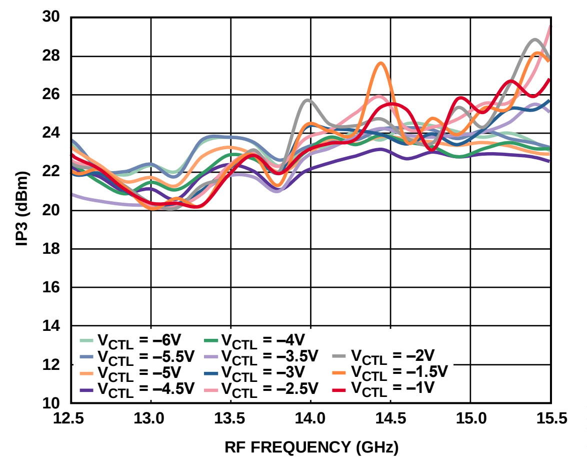

Figure 75. Input IP3 vs. RF Frequency at Various Control Voltages, LO = 2 dBm, V_{DLOx} = 2.4 V

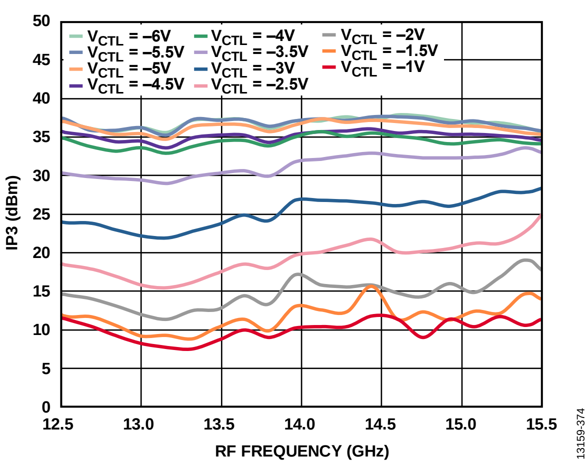

Figure 73. Output IP3 vs. RF Frequency at Various Control Voltages, LO = 2 dBm, V_{DLOx} = 2.4 V

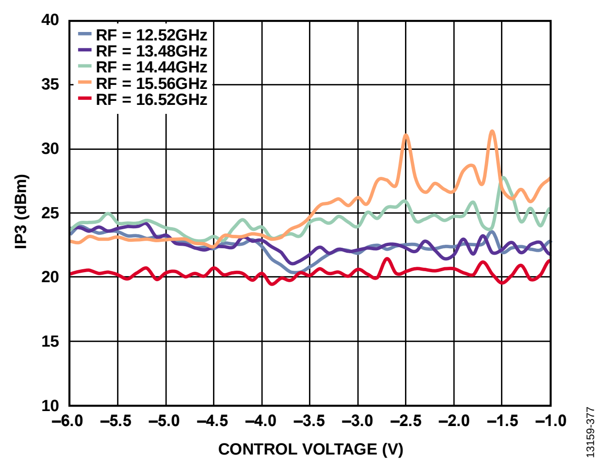

Figure 76. Input IP3 vs. Control Voltage at Various RF Frequencies, LO = 2 dBm, V_{DLOx} = 2.4 V

Data taken as SSB upconverter with external IF 90° hybrid at the IF ports, IF = 3 GHz.

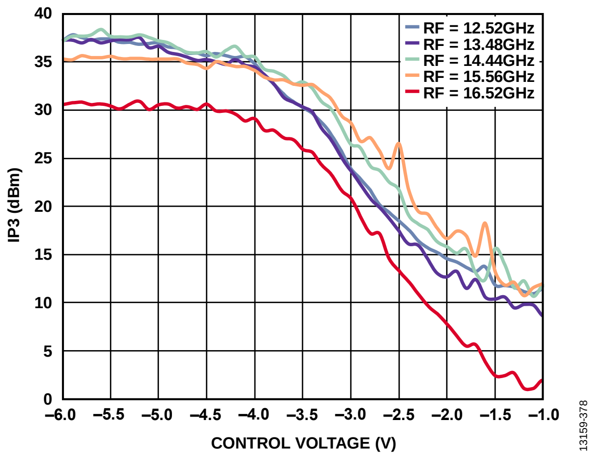

Figure 77. Output IP3 vs. Control Voltage at Various RF Frequencies, LO = 2 dBm, V_{DLOx} = 2.4 V

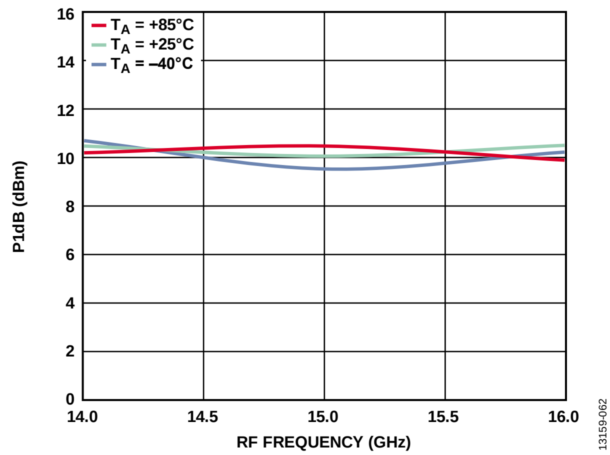

Figure 79. Input P1dB vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 2.4 V

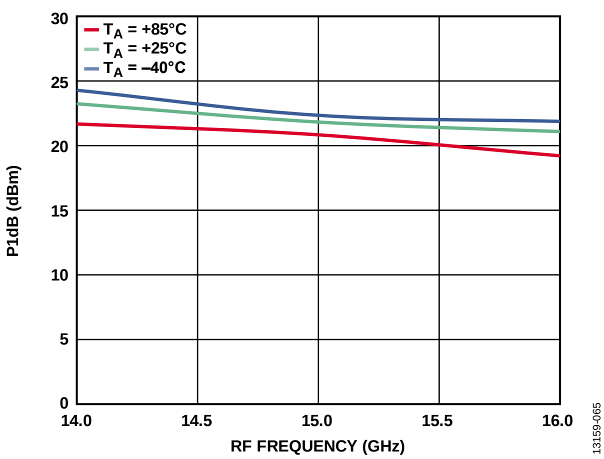

Figure 78. Output P1dB vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 2.4 V

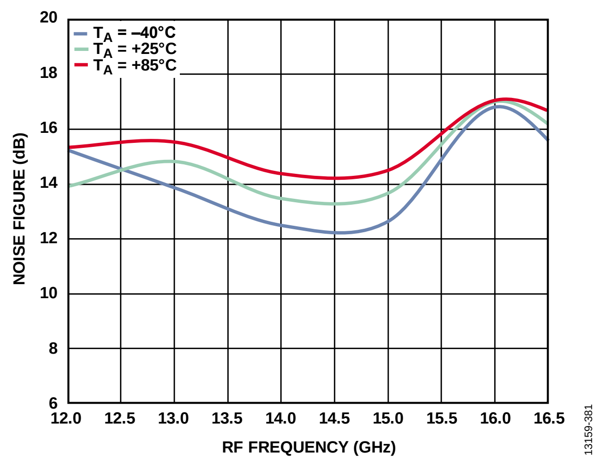

Figure 80. Noise Figure vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 2.4 V

LOWER SIDEBAND SELECTED

Data taken as SSB upconverter with external IF 90° hybrid at the IF ports, IF = 1 GHz.

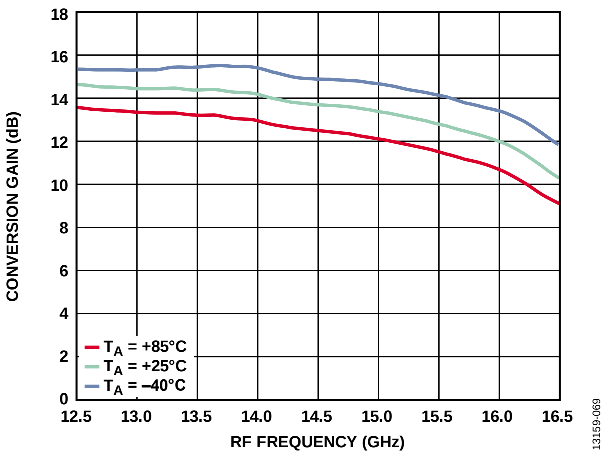

Figure 81. Conversion Gain vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLO1} = 3.3 V

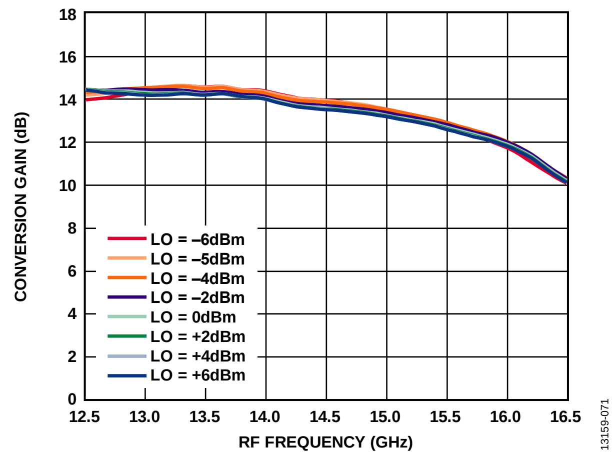

Figure 84. Conversion Gain vs. RF Frequency at Various LO Powers, V_{DLOx} = 3.3 V

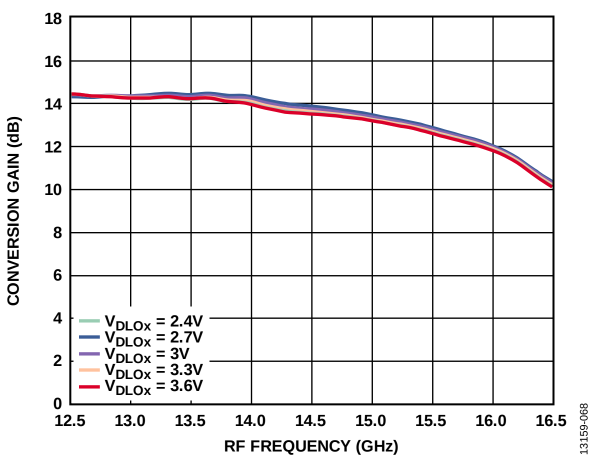

Figure 82. Conversion Gain vs. RF Frequency at Various V_{DLOx}, LO = 2 dBm

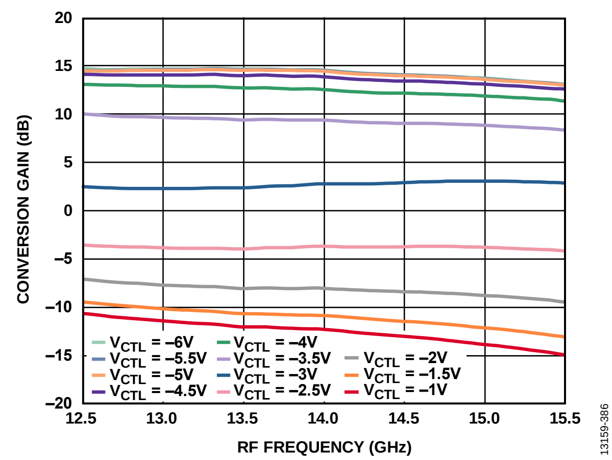

Figure 85. Conversion Gain vs. RF Frequency at Various Control Voltages, LO = 2 dBm, V_{DLOx} = 3.3 V

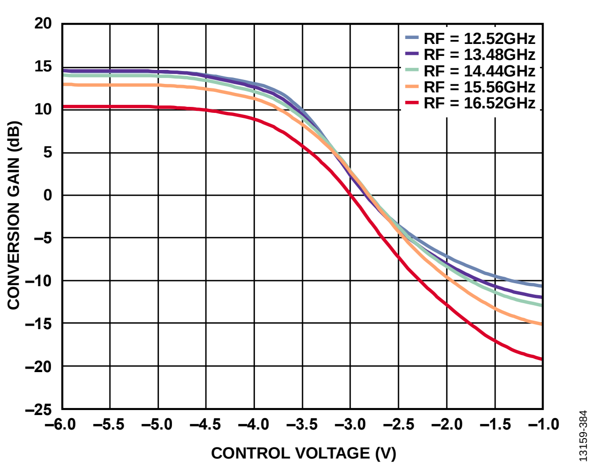

Figure 83. Conversion Gain vs. Control Voltage at Various RF Frequencies, LO = 2 dBm, V_{DLOx} = 3.3 V

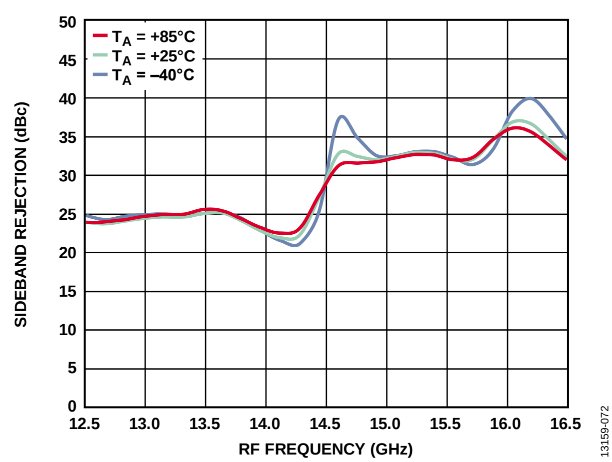

Figure 86. Sideband Rejection vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 3.3 V

Data taken as SSB upconverter with external IF 90° hybrid at the IF ports, IF = 1 GHz.

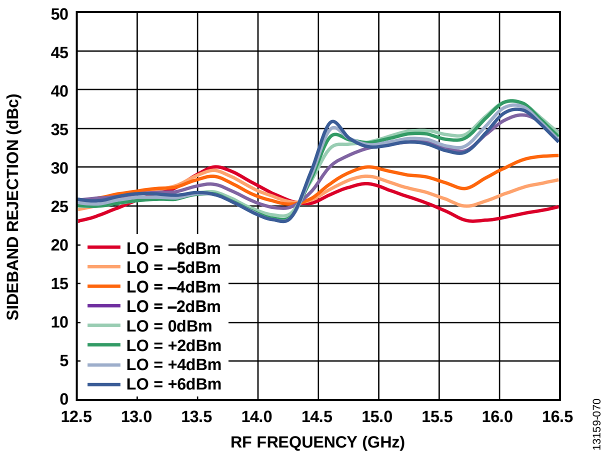

Figure 87. Sideband Rejection vs. RF Frequency at Various LO Powers, V_{DLOx} = 3.3 V

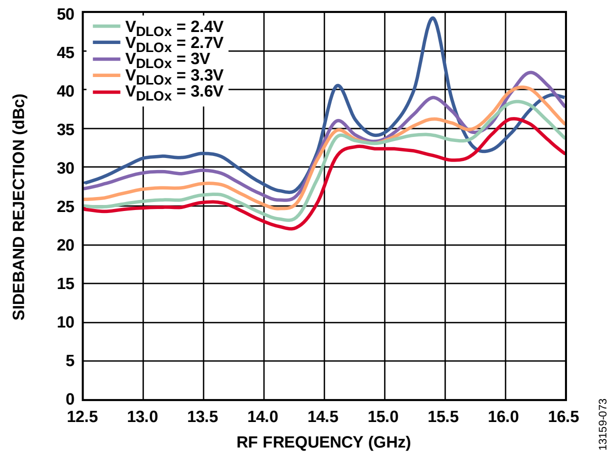

Figure 90. Sideband Rejection vs. RF Frequency at Various V_{DLOx}, LO = 2 dBm

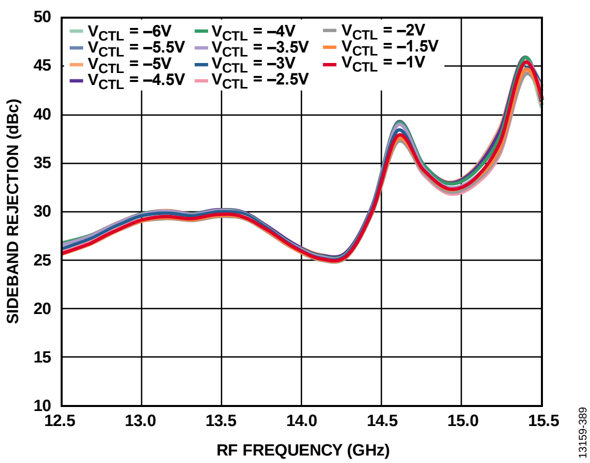

Figure 88. Sideband Rejection vs. RF Frequency at Various Control Voltages, LO = 2 dBm, V_{DLOx} = 3.3 V

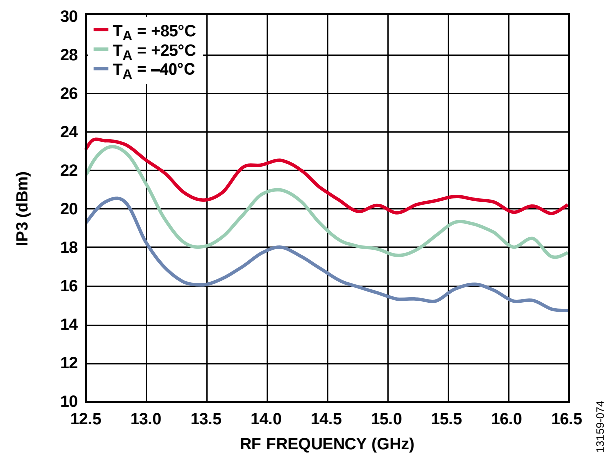

Figure 91. Input IP3 vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 3.3 V

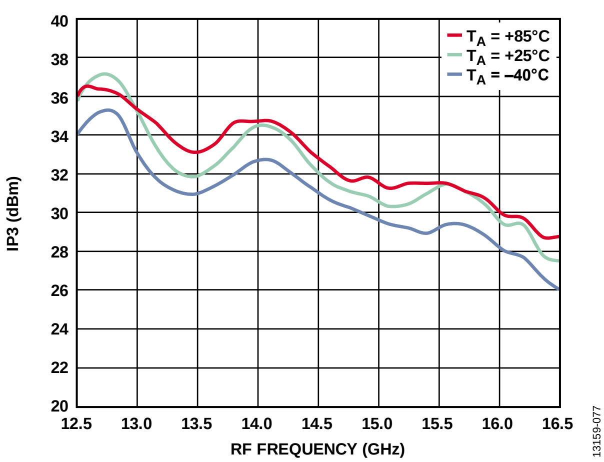

Figure 89. Output IP3 vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 3.3 V

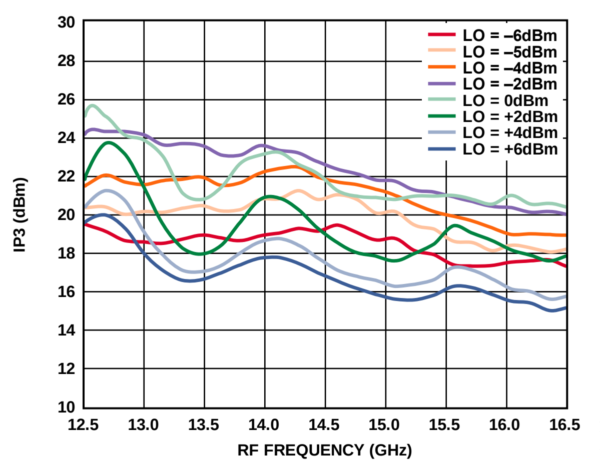

Figure 92. Input IP3 vs. RF Frequency at Various LO Powers, V_{DLOx} = 3.3 V

Data taken as SSB upconverter with external IF 90° hybrid at the IF ports, IF = 1 GHz.

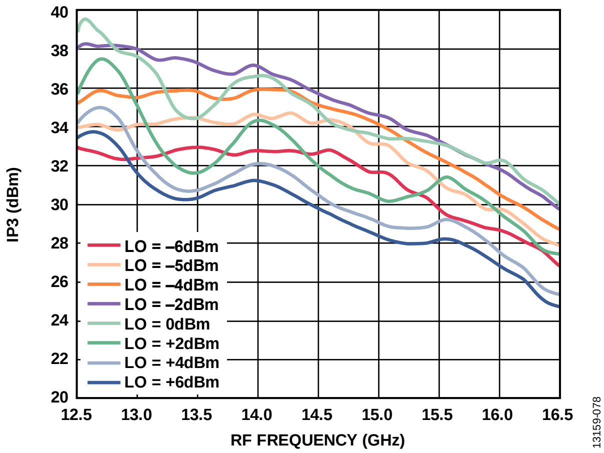

Figure 93. Output IP3 vs. RF Frequency at Various LO Powers, V_{DLOx} = 3.3 V

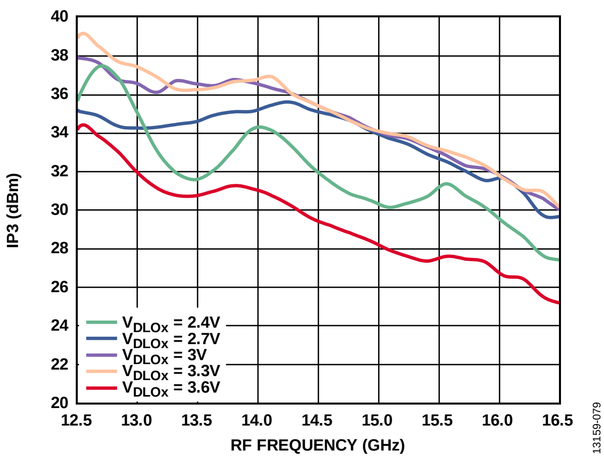

Figure 94. Output IP3 vs. RF Frequency at Various V_{DLOx}, LO = 2 dBm

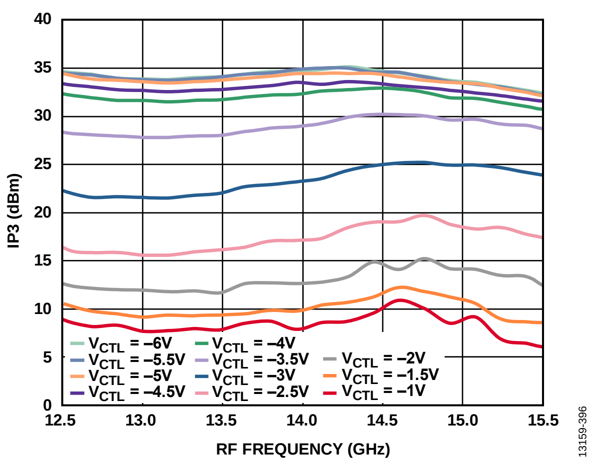

Figure 95. Output IP3 vs. RF Frequency at Various Control Voltages, LO = 2 dBm, V_{DLOx} = 3.3 V

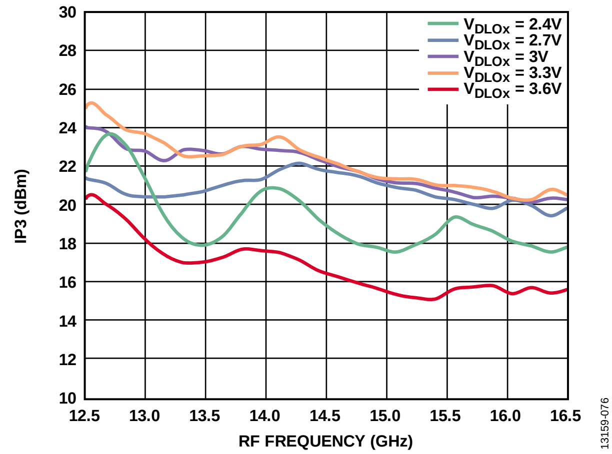

Figure 96. Input IP3 vs. RF Frequency at Various V_{DLOx}, LO = 2 dBm

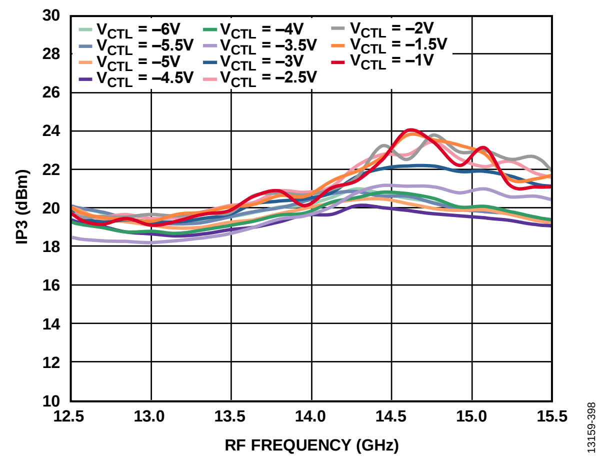

Figure 97. Input IP3 vs. RF Frequency at Various Control Voltages, LO = 2 dBm, V_{DLOx} = 3.3 V

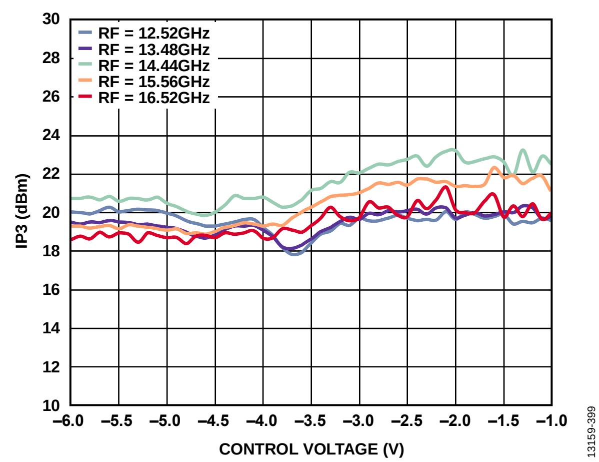

Figure 98. Input IP3 vs. Control Voltage at Various RF Frequencies, LO = 2 dBm, V_{DLOx} = 3.3 V

Data taken as SSB upconverter with external IF 90° hybrid at the IF ports, IF = 1 GHz.

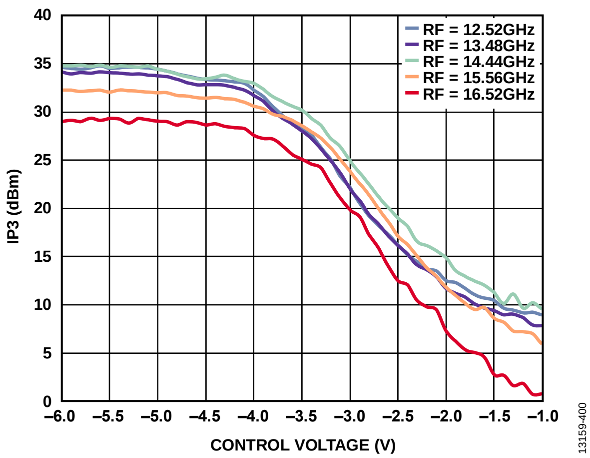

Figure 99. Output IP3 vs. Control Voltage at Various RF Frequencies, LO = 2 dBm, V_{DLOx} = 3.3 V

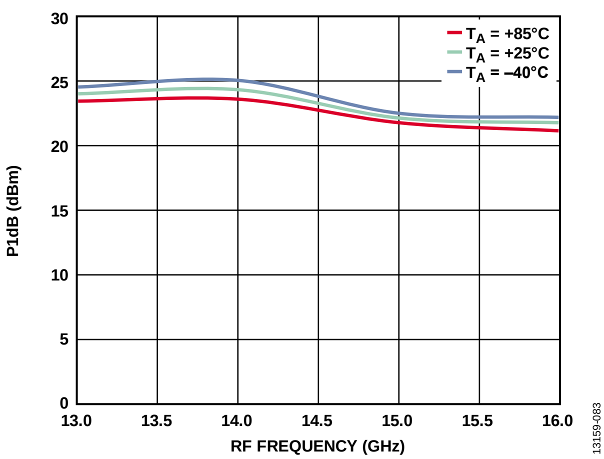

Figure 100. Output P1dB vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 3.3 V

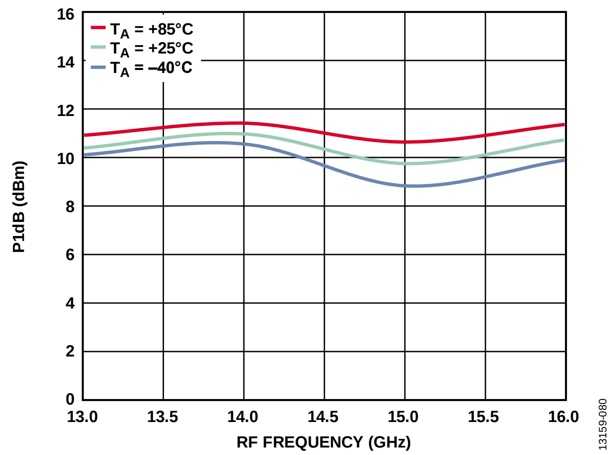

Figure 101. Input P1dB vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 3.3 V

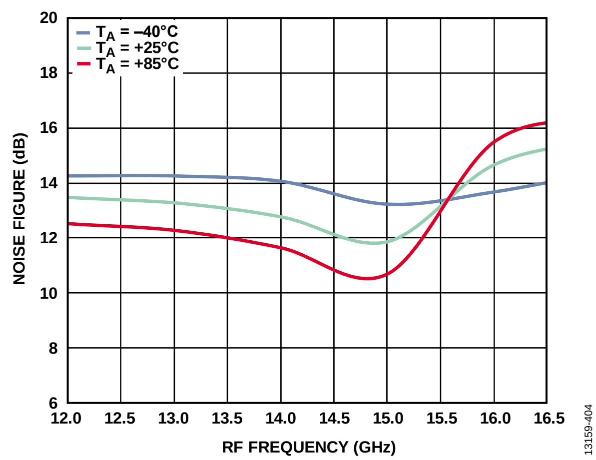

Figure 102. Noise Figure vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 3.3 V

Data taken as SSB upconverter with external IF 90° hybrid at the IF ports, IF = 2 GHz.

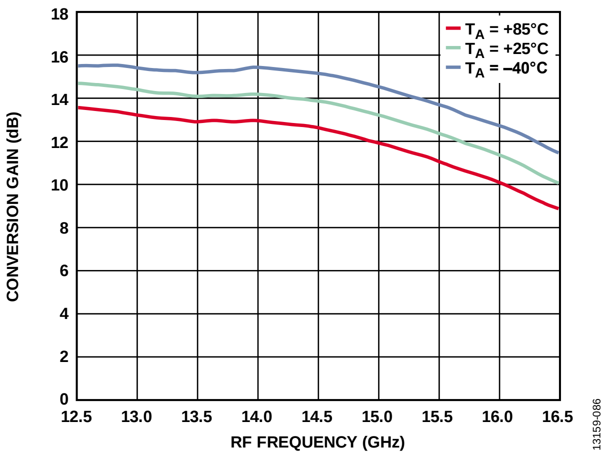

Figure 103. Conversion Gain vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 3.3 V

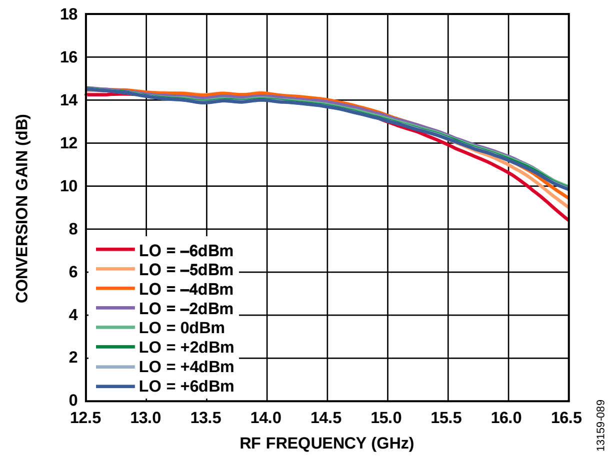

Figure 106. Conversion Gain vs. RF Frequency at Various LO Powers, V_{DLOx} = 3.3 V

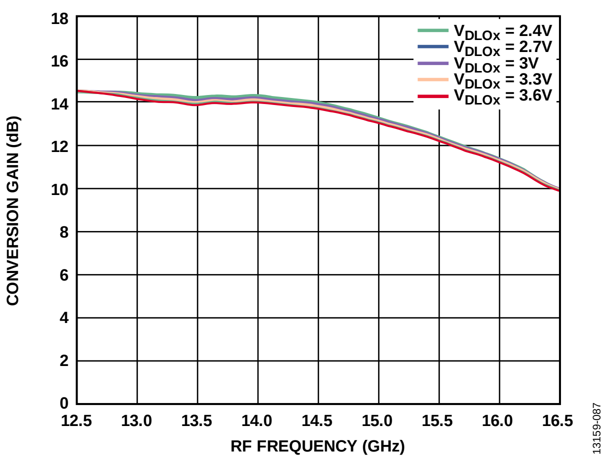

Figure 104. Conversion Gain vs. RF Frequency at Various V_{DLOx}, LO = 2 dBm

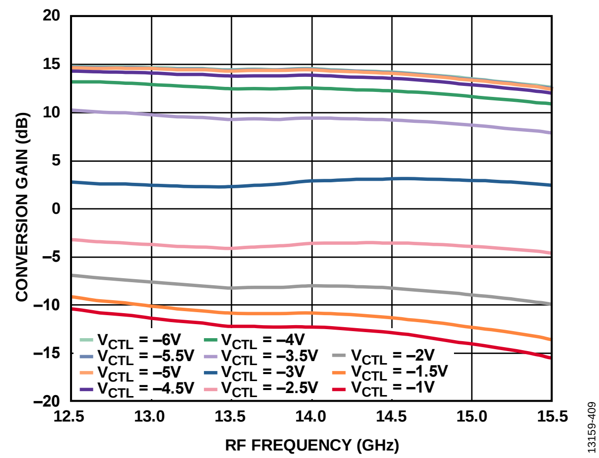

Figure 107. Conversion Gain vs. RF Frequency at Various Control Voltages, LO = 2 dBm, V_{DLOx} = 3.3 V

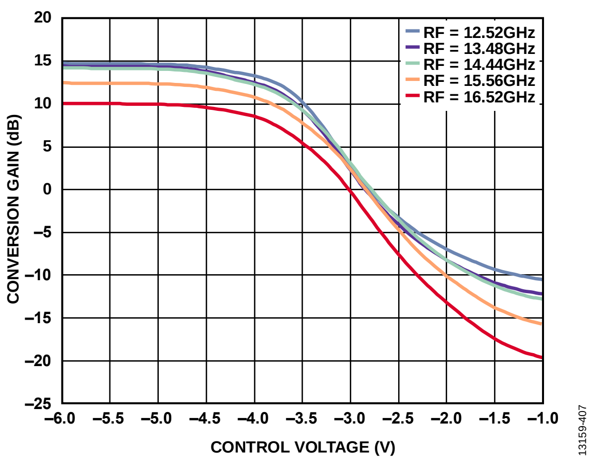

Figure 105. Conversion Gain vs. Control Voltage at Various RF Frequencies, LO = 2 dBm, V_{DLOx} = 3.3 V

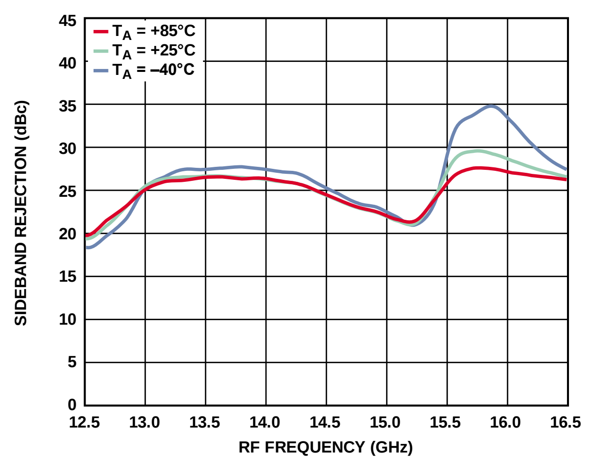

Figure 108. Sideband Rejection vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 3.3 V

Data taken as SSB upconverter with external IF 90° hybrid at the IF ports, IF = 2 GHz.

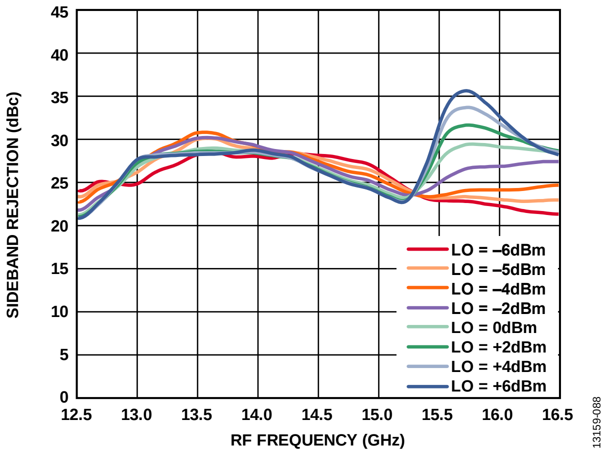

Figure 109. Sideband Rejection vs. RF Frequency at Various LO Powers, V_{DLOx} = 3.3 V

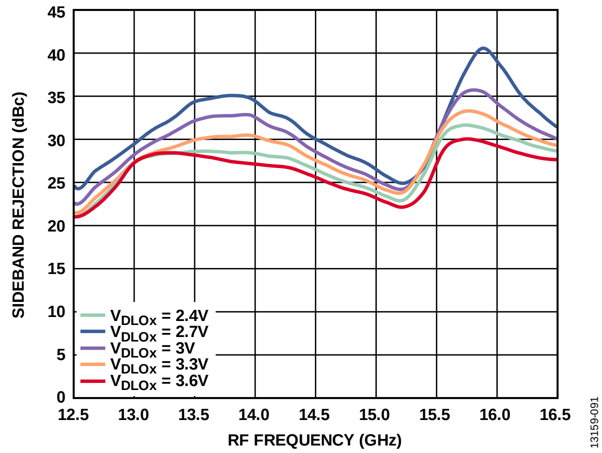

Figure 112. Sideband Rejection vs. RF Frequency at Various V_{DLOx}, LO = 2 dBm

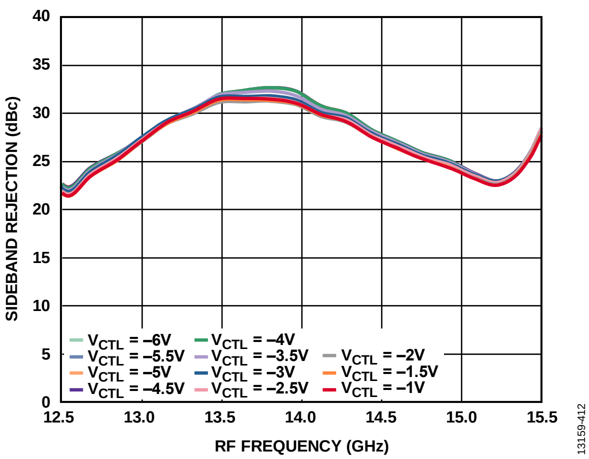

Figure 110. Sideband Rejection vs. RF Frequency at Various Control Voltages, LO = 2 dBm, V_{DLOx} = 3.3 V

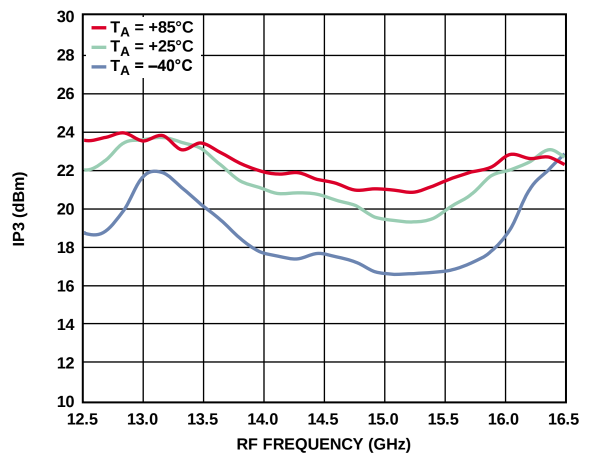

Figure 113. Input IP3 vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 3.3 V

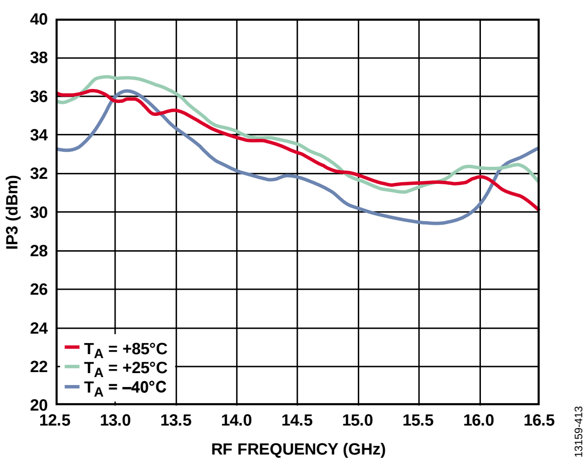

Figure 111. Output IP3 vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 3.3 V

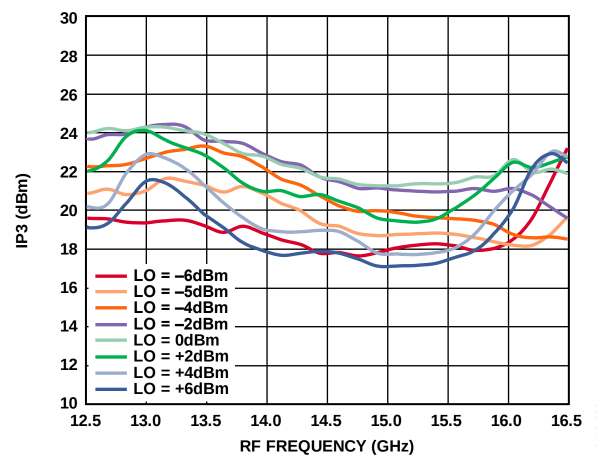

Figure 114. Input IP3 vs. RF Frequency at Various LO Powers, V_{DLOx} = 3.3 V

Data taken as SSB upconverter with external IF 90° hybrid at the IF ports, IF = 2 GHz.

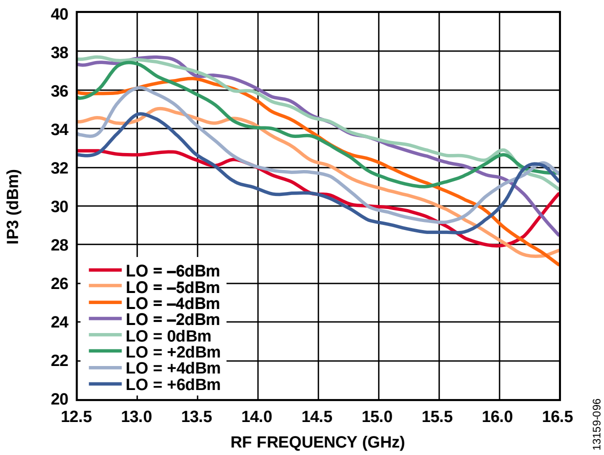

Figure 115. Output IP3 vs. RF Frequency at Various LO Powers, V_{DLOx} = 3.3 V

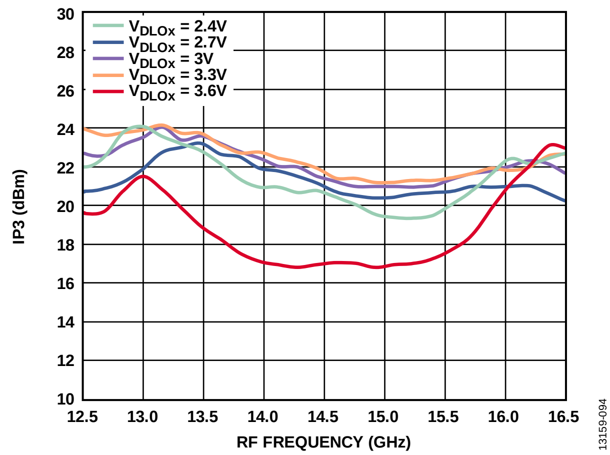

Figure 118. Input IP3 vs. RF Frequency at Various V_{DLOx}, LO = 2 dBm

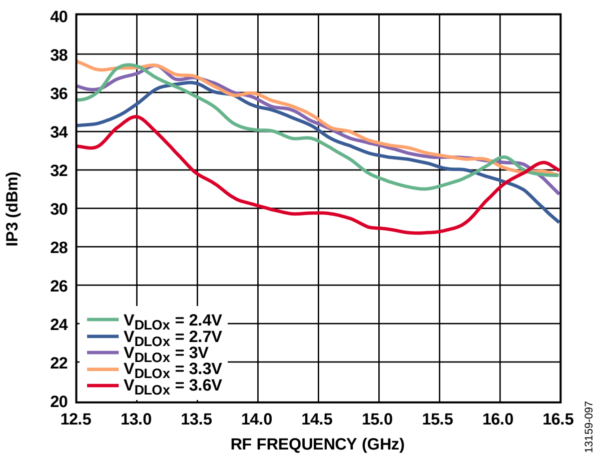

Figure 116. Output IP3 vs. RF Frequency at Various V_{DLOx}, LO = 2 dBm

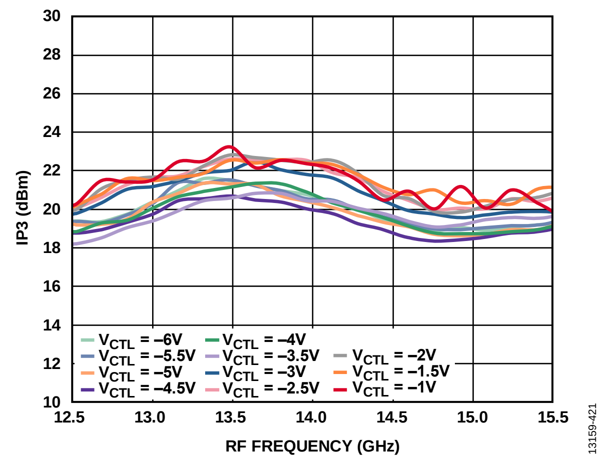

Figure 119. Input IP3 vs. RF Frequency at Various Control Voltages, LO = 2 dBm, V_{DLOx} = 3.3 V

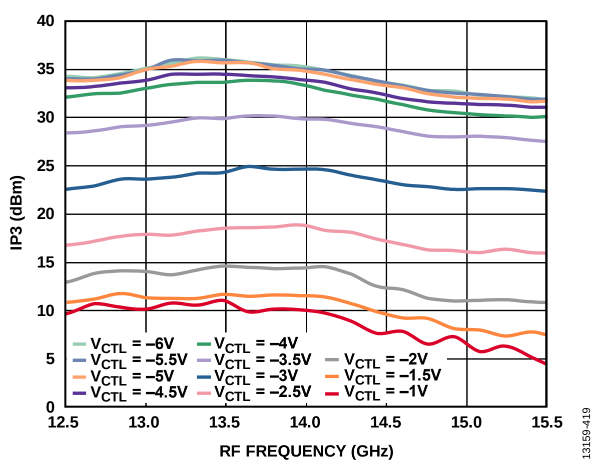

Figure 117. Output IP3 vs. RF Frequency at Various Control Voltages, LO = 2 dBm, V_{DLOx} = 3.3 V

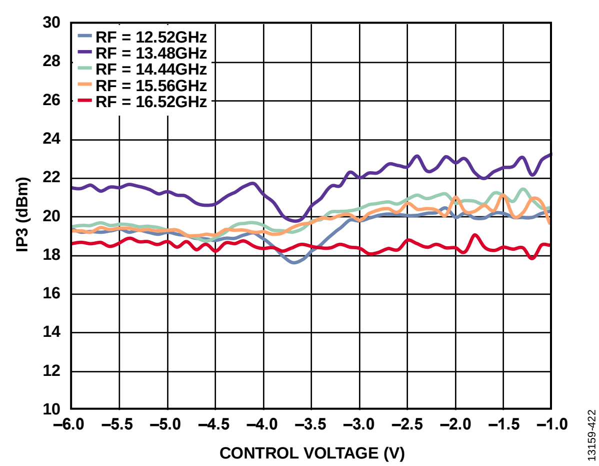

Figure 120. Input IP3 vs. Control Voltage at Various RF Frequencies, LO = 2 dBm, V_{DLOx} = 3.3 V

Data taken as SSB upconverter with external IF 90° hybrid at the IF ports, IF = 2 GHz.

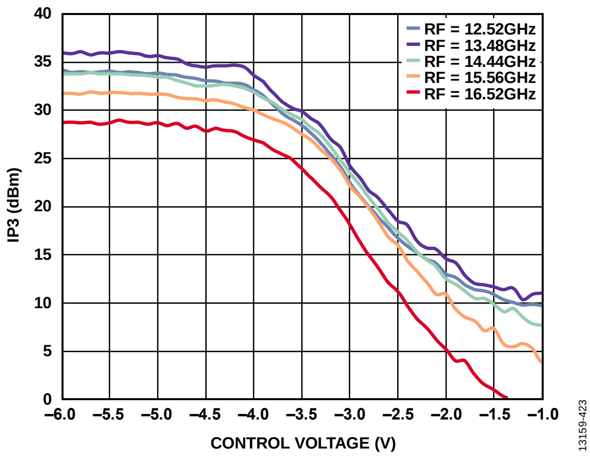

Figure 121. Output IP3 vs. Control Voltage at Various RF Frequencies, LO = 2 dBm, V_{DLOx} = 3.3 V

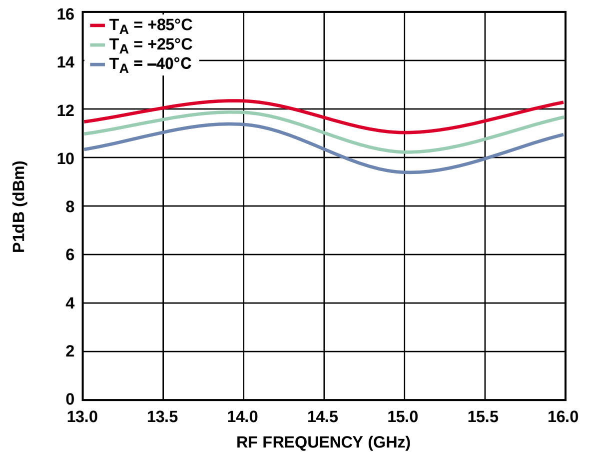

Figure 123. Input P1dB vs. RF Frequency at Various Temperatures, LO = 2 dBm

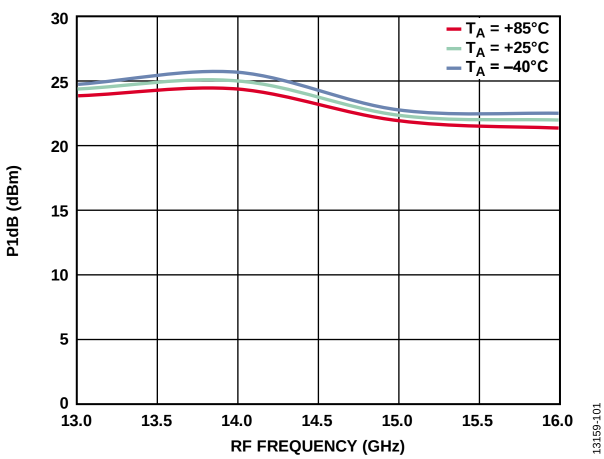

Figure 122. Output P1dB vs. RF Frequency at Various Temperatures, LO = 2 dBm

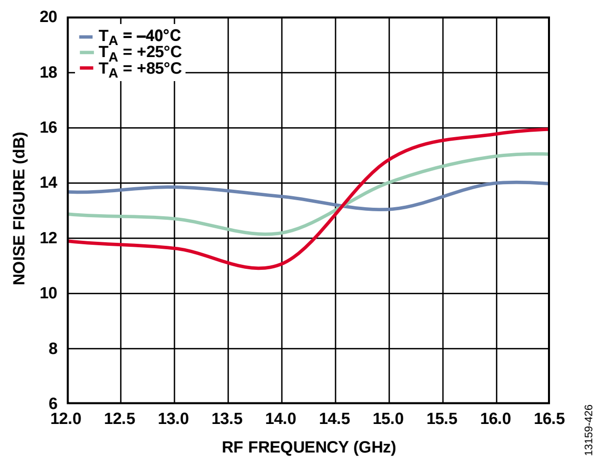

Figure 124. Noise Figure vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 3.3 V

Data taken as SSB upconverter with external IF 90° hybrid at the IF ports, IF = 3 GHz.

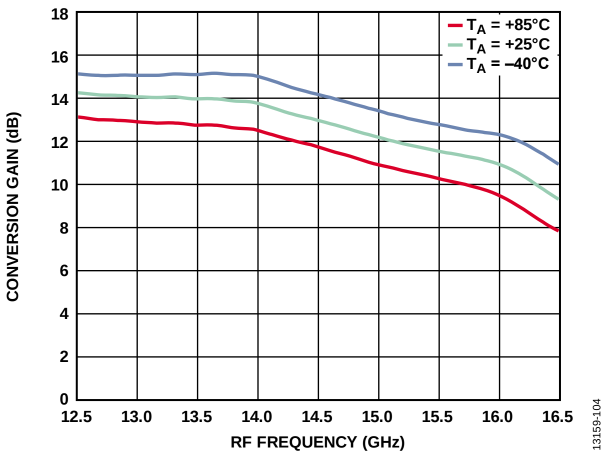

Figure 125. Conversion Gain vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLO1} = 3.3 V

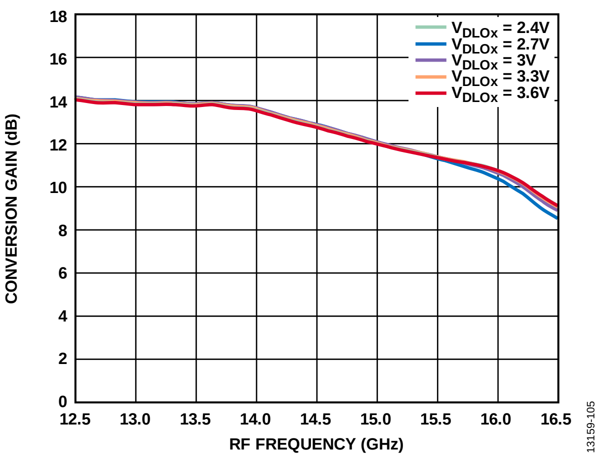

Figure 126. Conversion Gain vs. RF Frequency at Various V_{DLOx}, LO = 2 dBm

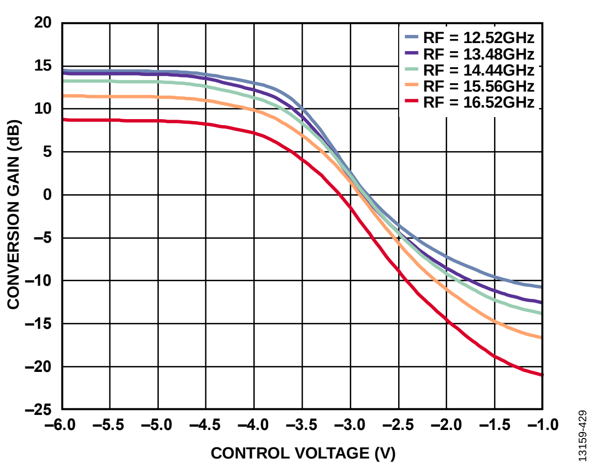

Figure 127. Conversion Gain vs. Control Voltage at Various RF Frequencies, LO = 2 dBm, V_{DLOx} = 3.3 V

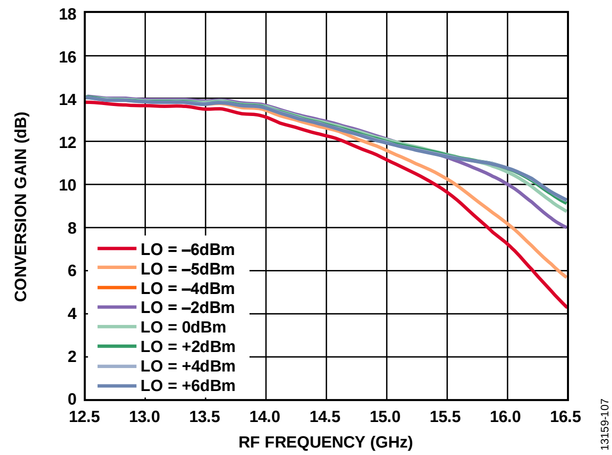

Figure 128. Conversion Gain vs. RF Frequency at Various LO Powers, V_{DLOx} = 3.3 V

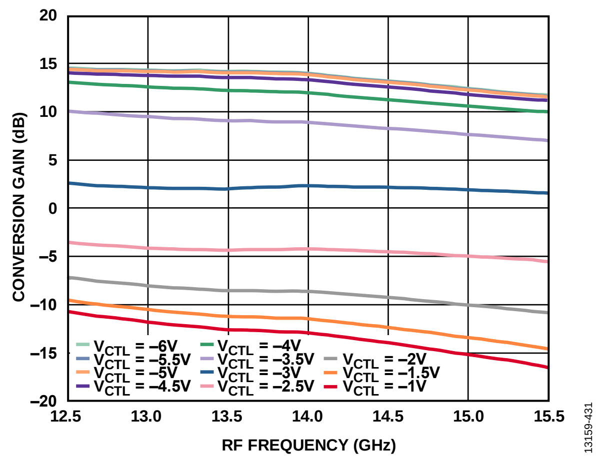

Figure 129. Conversion Gain vs. RF Frequency at Various Control Voltages, LO = 2 dBm, V_{DLOx} = 3.3 V

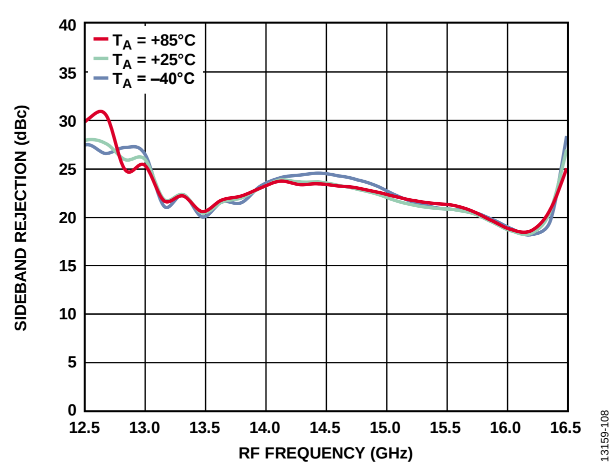

Figure 130. Sideband Rejection vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 3.3 V

Data taken as SSB upconverter with external IF 90° hybrid at the IF ports, IF = 3 GHz.

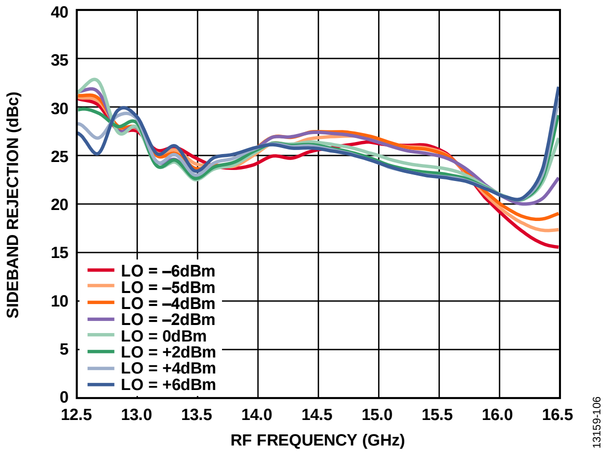

Figure 131. Sideband Rejection vs. RF Frequency at Various LO Powers, V_{DLOx} = 3.3 V

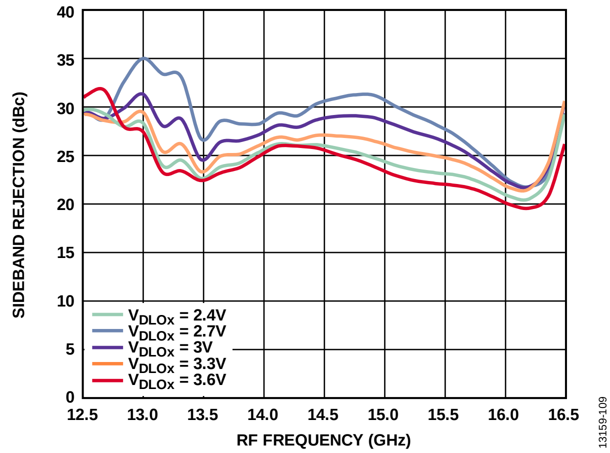

Figure 134. Sideband Rejection vs. RF Frequency at Various V_{DLOx}, LO = 2 dBm

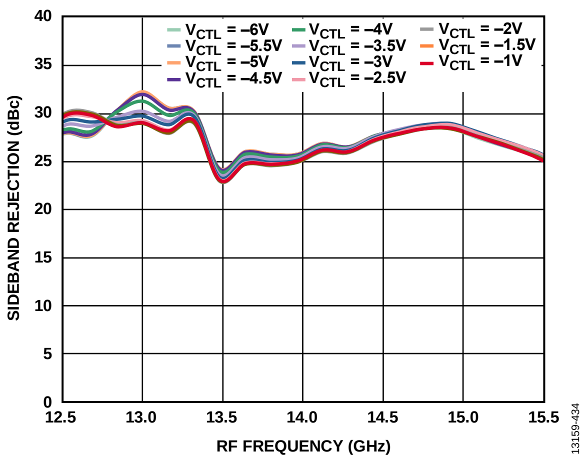

Figure 132. Sideband Rejection vs. RF Frequency at Various Control Voltages, LO = 2 dBm, V_{DLOx} = 3.3 V

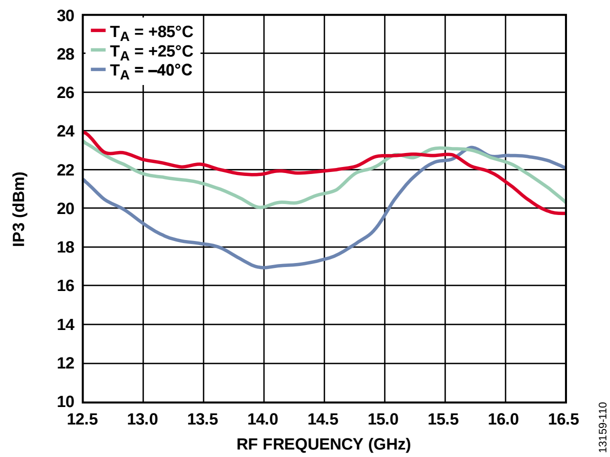

Figure 135. Input IP3 vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 3.3 V

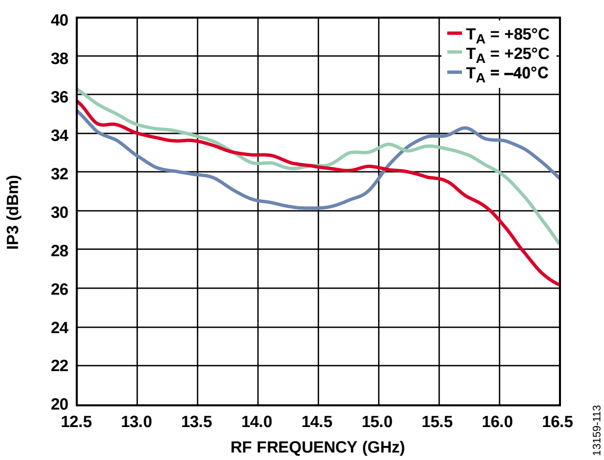

Figure 133. Output IP3 vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 3.3 V

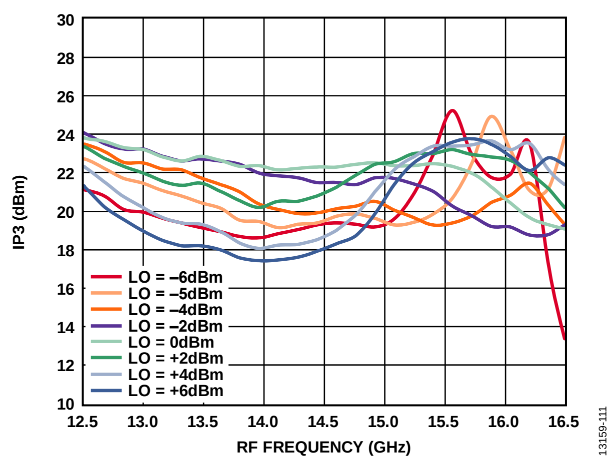

Figure 136. Input IP3 vs. RF Frequency at Various LO Powers, V_{DLOx} = 3.3 V

Data taken as SSB upconverter with external IF 90° hybrid at the IF ports, IF = 3 GHz.

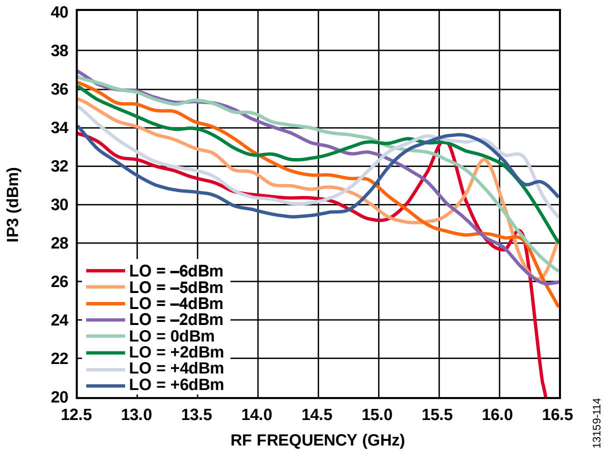

Figure 137. Output IP3 vs. RF Frequency at Various LO Powers, V_{DLOx} = 3.3 V

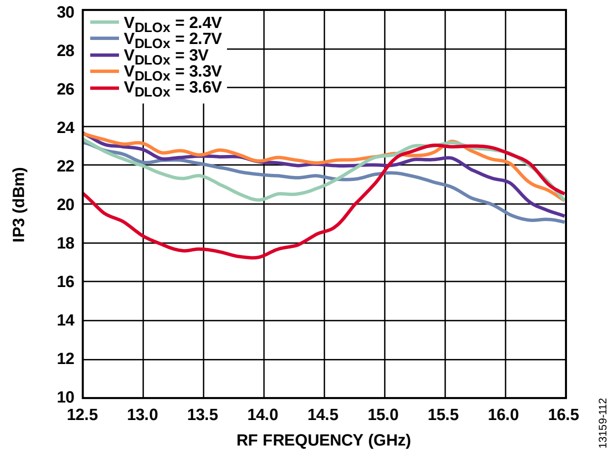

Figure 140. Input IP3 vs. RF Frequency at Various V_{DLOx}, LO = 2 dBm

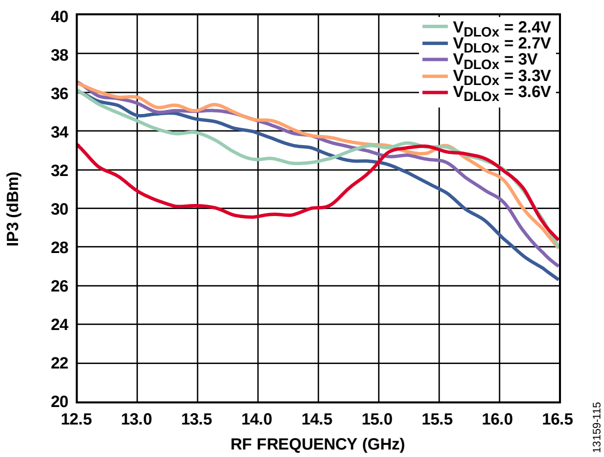

Figure 138. Output IP3 vs. RF Frequency at Various V_{DLOx}, LO = 2 dBm

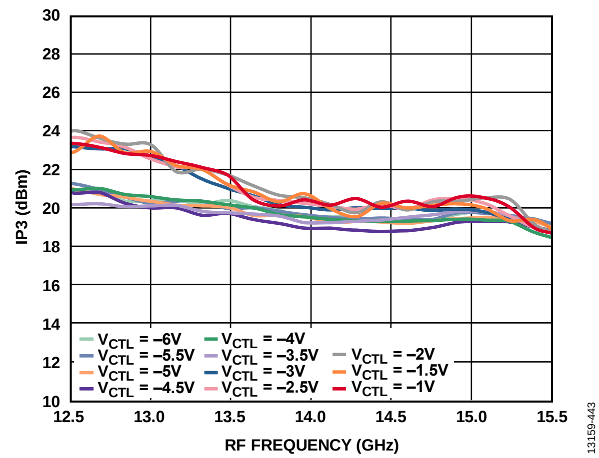

Figure 141. Input IP3 vs. RF Frequency at Various Control Voltages, LO = 2 dBm, V_{DLOx} = 3.3 V

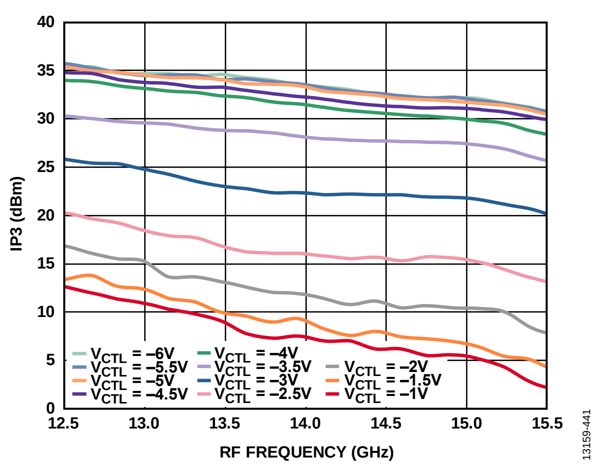

Figure 139. Output IP3 vs. RF Frequency at Various Control Voltages, LO = 2 dBm, V_{DLOx} = 3.3 V

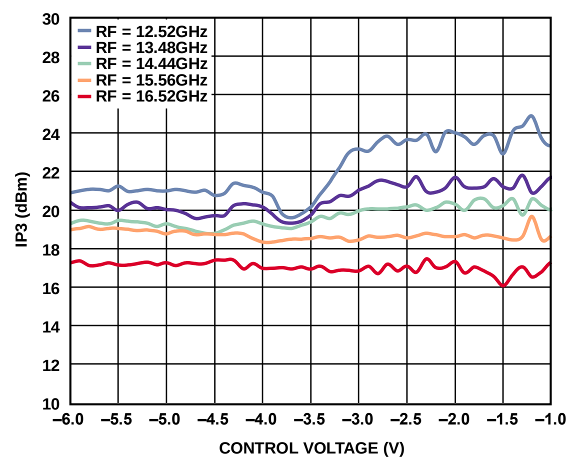

Figure 142. Input IP3 vs. Control Voltage at Various RF Frequencies, LO = 2 dBm, V_{DLOx} = 3.3 V

Data taken as SSB upconverter with external IF 90° hybrid at the IF ports, IF = 3 GHz.

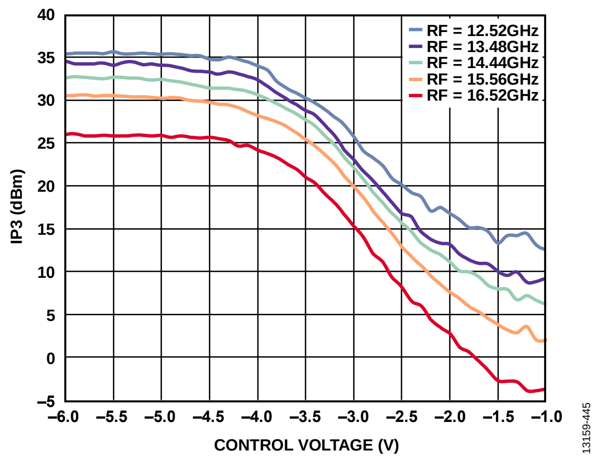

Figure 143. Output IP3 vs. Control Voltage at Various RF Frequencies, LO = 2 dBm, V_{DLOx} = 3.3 V

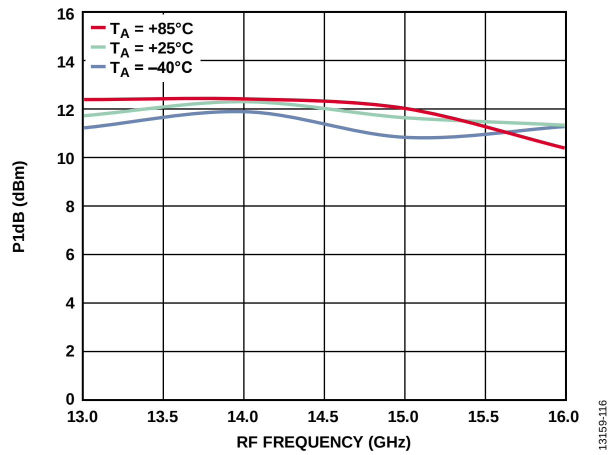

Figure 145. Input P1dB vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 3.3 V

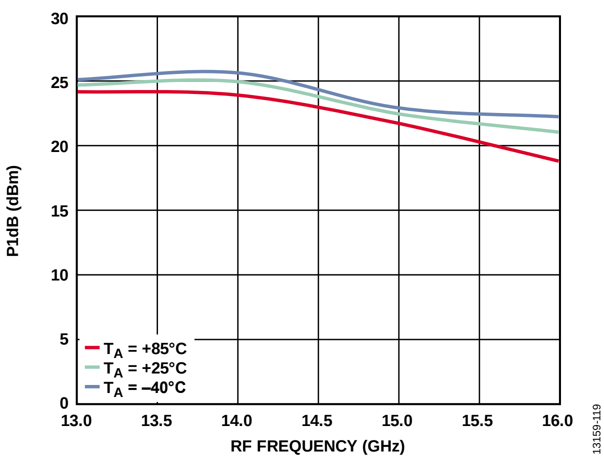

Figure 144. Output P1dB vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 3.3 V

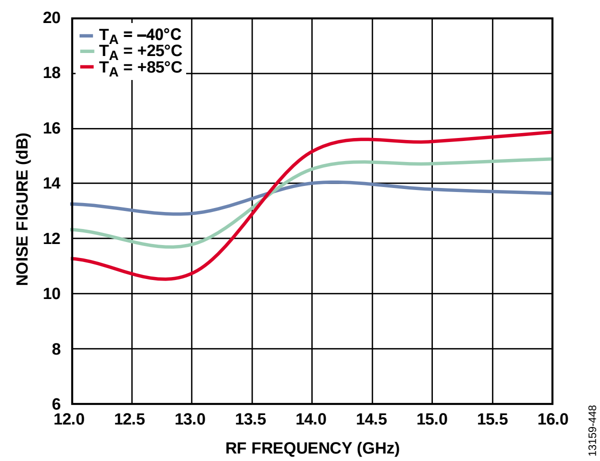

Figure 146. Noise Figure vs. RF Frequency at Various Temperatures, LO = 2 dBm, V_{DLOx} = 3.3 V

LEAKAGE PERFORMANCE

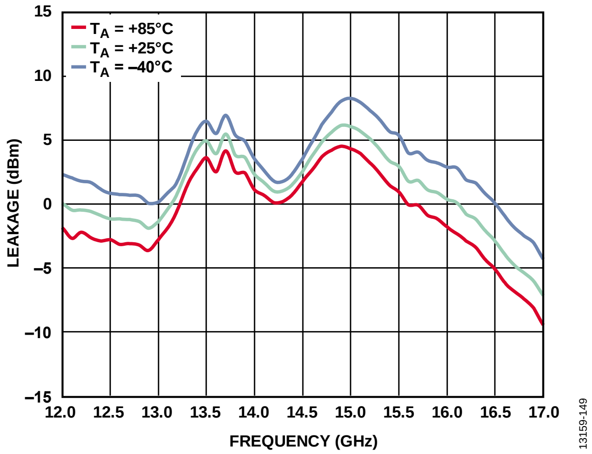

Figure 147. LO Leakage at RFOUT vs. Frequency at Various Temperatures, LO = 2 dBm

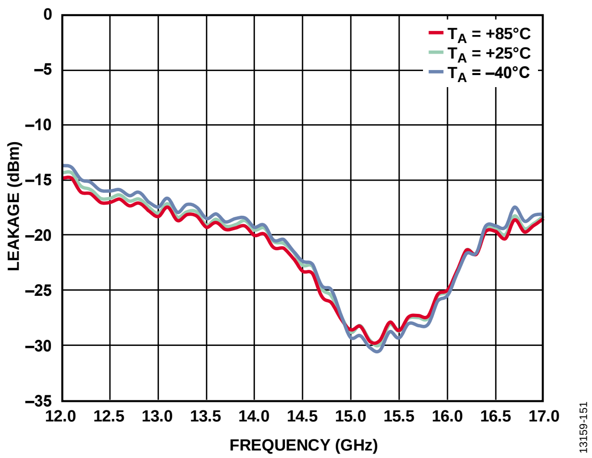

Figure 148. LO Leakage at IF1 vs. Frequency at Various Temperatures, LO = 2 dBm

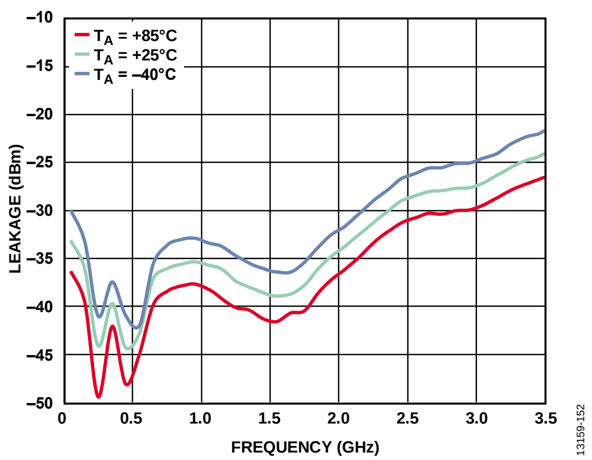

Figure 149. IF1 Leakage at RFOUT vs. Frequency at Various Temperatures, LO = 2 dBm

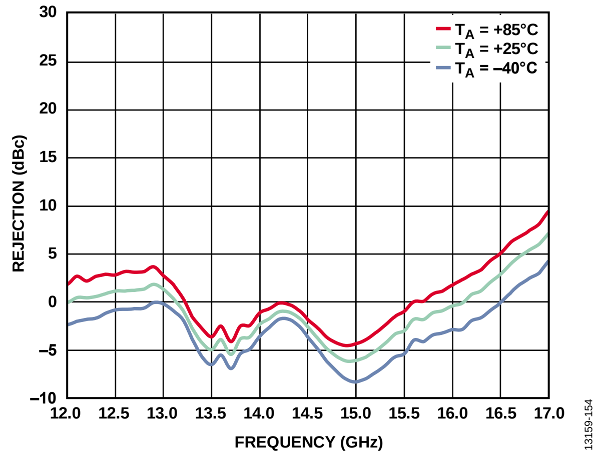

Figure 150. LO to RF Rejection vs. Frequency at Various Temperatures, LO = 2 dBm

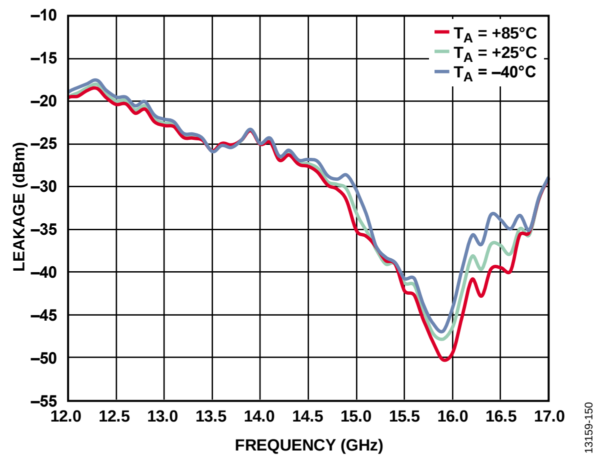

Figure 151. LO Leakage at IF2 vs. Frequency at Various Temperatures, LO = 2 dBm

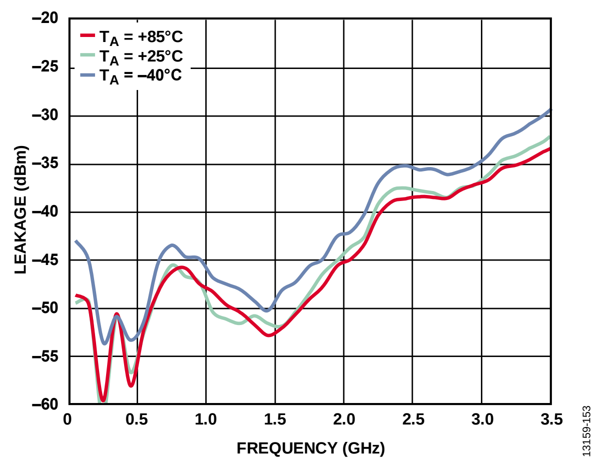

Figure 152. IF2 Leakage at RFOUT vs. Frequency at Various Temperatures, LO = 2 dBm

RETURN LOSS PERFORMANCE

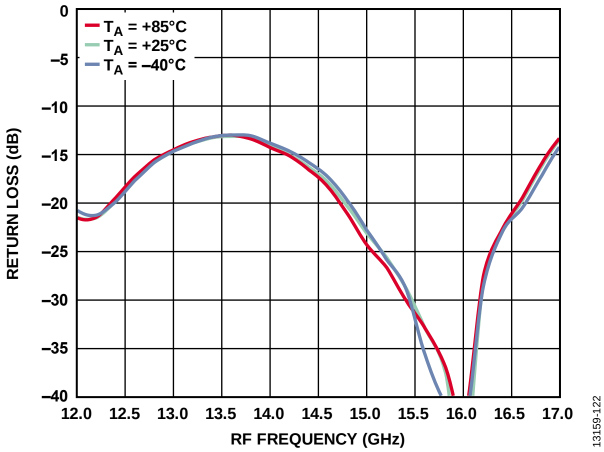

Figure 153. RF Return Loss vs. RF Frequency at Various Temperatures, LO = 2 dBm at LO = 15 GHz

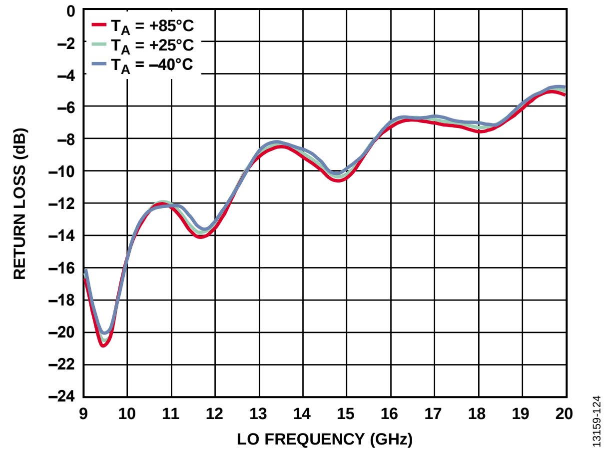

Figure 155. LO Return Loss vs. LO Frequency at Various Temperatures, LO = 2 dBm

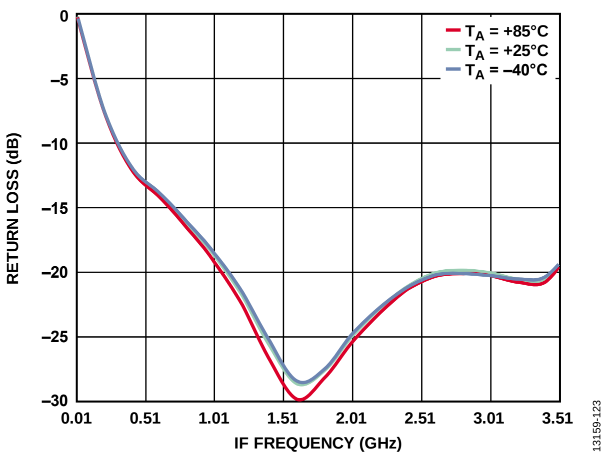

Figure 154. IF1 Return Loss vs. IF Frequency at Various Temperatures, LO = 2 dBm at LO = 15 GHz

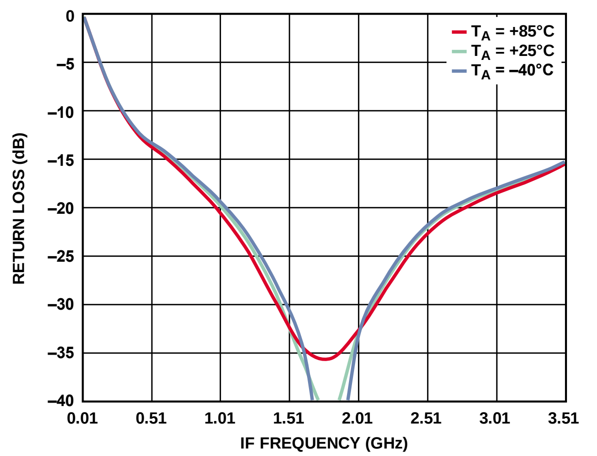

Figure 156. IF2 Return Loss vs. IF Frequency at Various Temperatures, LO = 2 dBm at LO = 15 GHz

POWER DETECTOR PERFORMANCE

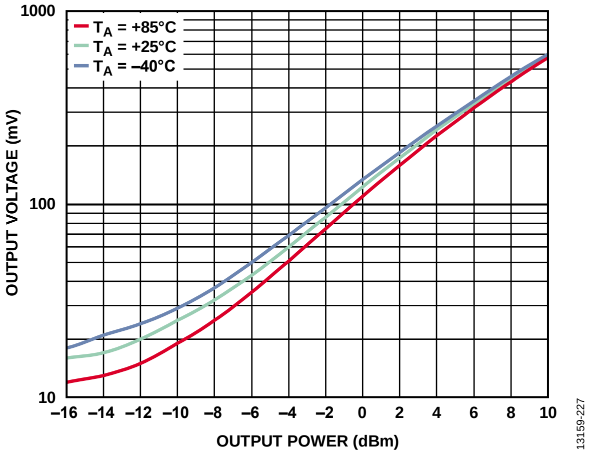

Figure 157. Detector Output Voltage (V_{REF} – V_{DET}) vs. Output Power at Various Temperatures, RF = 12 GHz

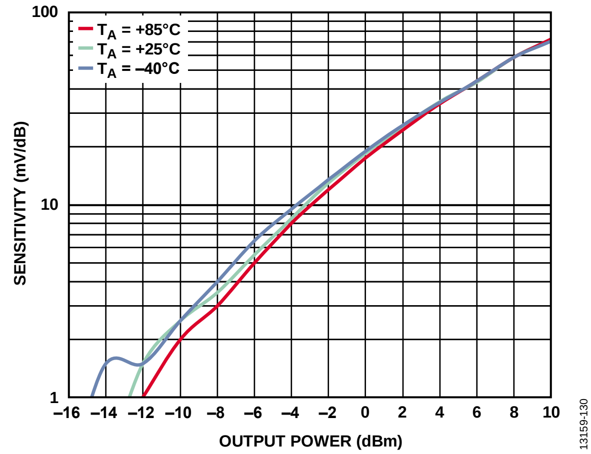

Figure 160. Detector Sensitivity vs. Output Power at Various Temperatures, RF = 12 GHz

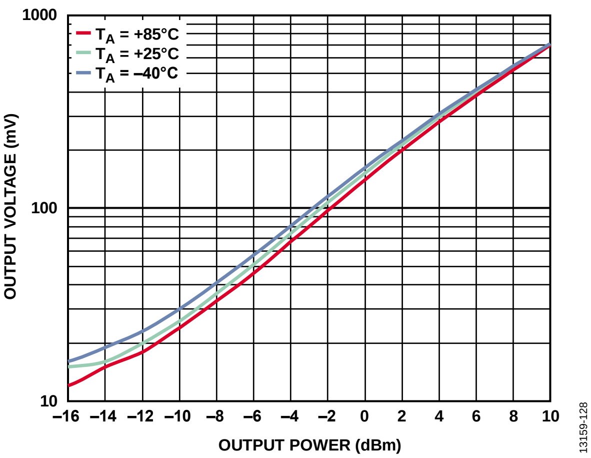

Figure 158. Detector Output Voltage (V_{REF} – V_{DET}) vs. Output Power at Various Temperatures, RF = 14 GHz

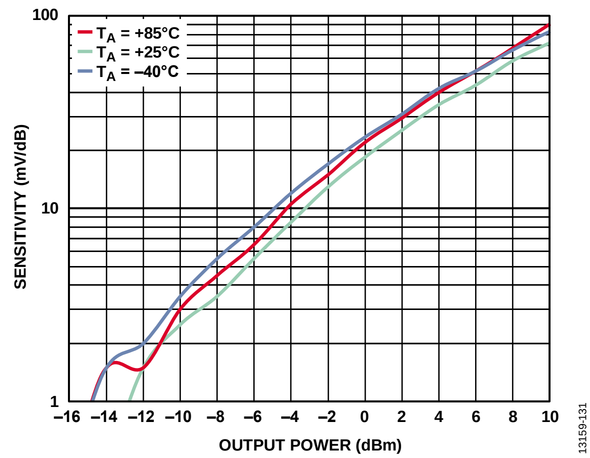

Figure 161. Detector Sensitivity vs. Output Power at Various Temperatures, RF = 14 GHz

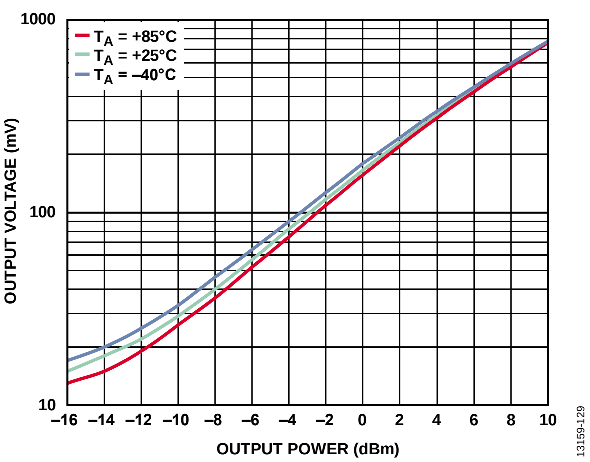

Figure 159. Detector Output Voltage (V_{REF} – V_{DET}) vs. Output Power at Various Temperatures, RF = 16 GHz

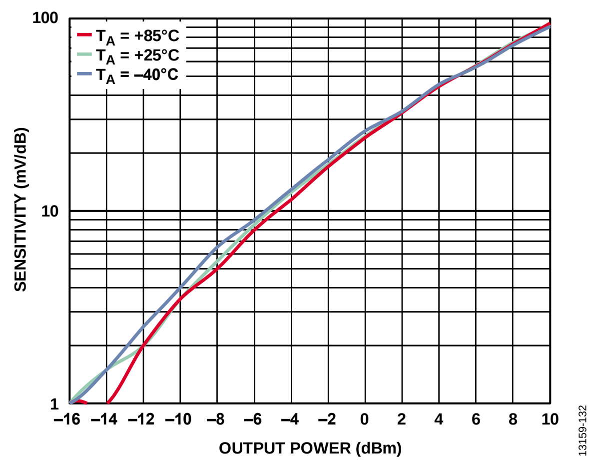

Figure 162. Detector Sensitivity vs. Output Power at Various Temperatures, RF = 16 GHz

UPPER SIDEBAND SPURIOUS PERFORMANCE

T_A = 25°C, V_{DLOx} = 2.4 V, V_{DRFx} = 5 V, V_{CC} = 5 V, V_{CTL} = −6 V, V_{ESD} = −5 V, V_{SS} = −5 V, V_{GMIX} = −0.5 V.

Mixer spurious products are measured in dBc from the RF output power level. Spur values are (M × IF) + (N × LO). N/A means not applicable.

M × N Spurious Outputs, RF = 13 GHz

IF = 1 GHz at IF input power = −6 dBm, LO frequency = 12 GHz at LO input power = 2 dBm.

		N × LO					
		0	1	2	3	4	5
M × IF	0	N/A	10	55	65	65	N/A
	1	76	0	54	71	N/A	N/A
	2	67	41	52	77	N/A	N/A
	3	96	83	84	71	N/A	N/A
	4	97	88	104	92	N/A	N/A
	5	111	102	102	99	N/A	N/A

IF = 2 GHz at IF input power = −6 dBm, LO frequency = 11 GHz at LO input power = 2 dBm.

		N × LO					
		0	1	2	3	4	5
M × IF	0	N/A	7	39	93	93	N/A
	1	48	0	50	74	N/A	N/A
	2	62	45	52	76	N/A	N/A
	3	71	78	90	71	N/A	N/A
	4	84	96	101	87	N/A	N/A
	5	109	107	103	99	N/A	N/A

IF = 3 GHz at IF input power = −6 dBm, LO frequency = 10 GHz at LO input power = 2 dBm.

		N × LO					
		0	1	2	3	4	5
M × IF	0	N/A	10	27	62	62	N/A
	1	61	0	53	74	84	N/A
	2	59	45	54	84	N/A	N/A
	3	66	82	95	75	N/A	N/A
	4	82	105	100	100	N/A	N/A
	5	104	103	99	N/A	N/A	N/A

M × N Spurious Output, RF = 16 GHz

IF = 1 GHz at IF input power = −6 dBm, LO frequency = 15 GHz at LO input power = 2 dBm.

		N × LO					
		0	1	2	3	4	5
M × IF	0	N/A	2	58	N/A	N/A	N/A
	1	76	0	57	N/A	N/A	N/A
	2	77	45	70	N/A	N/A	N/A
	3	95	76	98	N/A	N/A	N/A
	4	98	98	98	N/A	N/A	N/A
	5	109	103	96	N/A	N/A	N/A

IF = 2 GHz at IF input power = −6 dBm, LO frequency = 14 GHz at LO input power = 2 dBm.

		N × LO					
		0	1	2	3	4	5
M × IF	0	N/A	7	53	58	58	N/A
	1	57	0	65	93	N/A	N/A
	2	61	52	69	N/A	N/A	N/A
	3	85	88	99	N/A	N/A	N/A
	4	58	81	93	N/A	N/A	N/A
	5	43	80	97	N/A	N/A	N/A

IF = 3 GHz at IF input power = −6 dBm, LO frequency = 13 GHz at LO input power = 2 dBm.

		N × LO					
		0	1	2	3	4	5
M × IF	0	N/A	16	55	58	58	N/A
	1	63	0	68	84	N/A	N/A
	2	70	56	69	N/A	N/A	N/A
	3	66	93	95	N/A	N/A	N/A
	4	88	101	98	N/A	N/A	N/A
	5	105	100	96	N/A	N/A	N/A

LOWER SIDEBAND SPURIOUS PERFORMANCE

T_A = 25°C, V_{DLOx} = 3.3 V, V_{DRFx} = 5 V, V_{CC} = 5 V, V_{CTL} = −6 V, V_{ESD} = −5 V, V_{SS} = −5 V, V_{GMIX} = −0.5 V.

Mixer spurious products are measured in dBc from the RF output power level. Spur values are (M × IF) − (N × LO). N/A means not applicable.

M × N Spurious Outputs, RF = 13 GHz

IF = 1 GHz at IF input power = −6 dBm, LO frequency = 14 GHz at LO input power = 2 dBm

		N × LO					
		0	1	2	3	4	5
M × IF	0	N/A	4	52	61	N/A	N/A
	1	74	0	51	72	N/A	N/A
	2	76	46	53	72	N/A	N/A
	3	97	81	88	74	N/A	N/A
	4	106	97	105	98	N/A	N/A
	5	110	111	107	99	N/A	N/A

IF = 2 GHz at IF input power = −6 dBm, LO frequency = 15 GHz at LO input power = 2 dBm.

		N × LO					
		0	1	2	3	4	5
M × IF	0	N/A	1	60	N/A	N/A	N/A
	1	40	0	49	64	N/A	N/A
	2	66	45	52	60	N/A	N/A
	3	97	75	90	72	N/A	N/A
	4	96	103	96	93	N/A	N/A
	5	106	112	107	98	N/A	N/A

IF = 3 GHz at IF input power = −6 dBm, LO frequency = 16 GHz at LO input power = 2 dBm.

		N × LO					
		0	1	2	3	4	5
M × IF	0	N/A	7	65	N/A	N/A	N/A
	1	54	0	57	N/A	N/A	N/A
	2	65	41	53	70	N/A	N/A
	3	85	80	84	73	N/A	N/A
	4	103	110	107	95	N/A	N/A
	5	109	121	110	100	N/A	N/A

M × N Spurious Output, RF = 16 GHz

IF = 1 GHz at IF input power = −6 dBm, LO frequency = 17 GHz at LO input power = 2 dBm.

		N × LO					
		0	1	2	3	4	5
M × IF	0	N/A	19	59	N/A	N/A	N/A
	1	90	0	80	N/A	N/A	N/A
	2	71	45	68	N/A	N/A	N/A
	3	109	71	101	N/A	N/A	N/A
	4	107	96	99	N/A	N/A	N/A
	5	110	108	99	N/A	N/A	N/A

IF = 2 GHz at IF input power = −6 dBm, LO frequency = 18 GHz at LO input power = 2 dBm.

		N × LO					
		0	1	2	3	4	5
M × IF	0	N/A	26	57	N/A	N/A	N/A
	1	64	0	84	N/A	N/A	N/A
	2	67	37	69	N/A	N/A	N/A
	3	92	78	93	N/A	N/A	N/A
	4	110	86	100	N/A	N/A	N/A
	5	86	107	100	95	N/A	N/A

IF = 3 GHz at IF input power = −6 dBm, LO frequency = 19 GHz at LO input power = 2 dBm.

		N × LO					
		0	1	2	3	4	5
M × IF	0	N/A	30	62	N/A	N/A	N/A
	1	63	0	97	N/A	N/A	N/A
	2	58	35	69	N/A	N/A	N/A
	3	75	71	87	N/A	N/A	N/A
	4	106	80	100	N/A	N/A	N/A
	5	108	107	103	97	N/A	N/A

THEORY OF OPERATION

The HMC9060 is a GaAs MMIC I/Q upconverter with an integrated LO buffer that upconverts IF between dc and 3.5 GHz to RF between 12.5 GHz and 16.5 GHz. LO buffer amplifiers are included on chip to allow a LO drive level of only 2 dBm for full performance. The LO path feeds a quadrature splitter followed by on-chip baluns that drive the in-phase (I) and quadrature (Q) singly balanced cores of the passive mixers. The RF output of the I and Q mixers are then summed through an on-chip Wilkinson power combiner and relatively matched to provide a single-ended 50 Ω output signal that is amplified by RF amplifiers to produce a dc-coupled and 50 Ω matched radio frequency output signal at the RFOUT port. A voltage attenuator precedes the RF amplifiers for desired gain control.

The power detector feature provides LO cancellation capability to the level of −10 dBm. See Figure 163 for a functional block diagram of the circuit architecture.

Optimum output IP3 performance at a given LO power level is obtained when a 2.4 V power supply is used for V_{DLOx} with upper sideband selection. Alternatively, a 3.3 V V_{DLOx} is recommended for lower sideband selection for optimum performance.

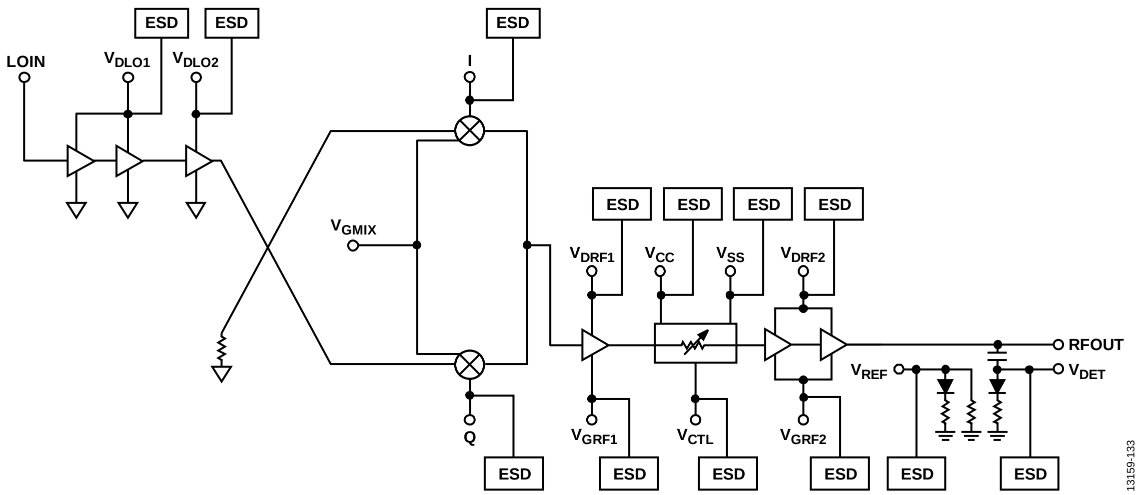

Figure 163. Upconverter Circuit Architecture

APPLICATIONS INFORMATION

A typical single-sideband upconversion circuit is shown in Figure 164. For single-sideband upconversion, an external 90° hybrid splits the IF signal into I and Q inputs. The LO to RF leakage can be improved by applying small dc offsets to the I/Q mixer cores via the IF V_{DC_IF1} and V_{DC_IF2} inputs. (V_{DC_IFx} is the dc voltage at the IFx path.) However, it is important to limit the applied dc bias to avoid sourcing or sinking more than ±3 mA of bias current. Depending on the bias sources used, it may be prudent to add series resistance to ensure the applied bias current does not exceed ±3 mA.

BIASING SEQUENCE

The HMC9060 uses buffer amplifiers in the LO and RF paths. These active stages all use depletion mode pHEMTs. To ensure transistor damage does not occur, use the following power-up bias sequence:

1. Apply a −5 V bias to Pin 32 (V_{ESD}) and Pin 19 (V_{SS}).
2. Apply a −2 V bias to Pin 23 (V_{GRF1}), and Pin 26 (V_{GRF2}) (pinched off state).
3. Apply a −0.5 V bias to Pin 1 (V_{GMIX}). This bias can be adjusted from +0.5 V to −1 V depending on the LO power and V_{DLOx} used to provide the optimum IP3 response of the mixer.
4. Apply 2.4 V or 3.3 V to Pin 9 (V_{DLO1}) and Pin 10 (V_{DLO2}) depending on the sideband selection.
5. Apply −6 V to Pin 20 (V_{CTL}). Adjust V_{CTL} between −6 V and 0 V depending on amount of attenuation desired.
6. Apply 5 V to V_{DRF1}, V_{DRF2}, and V_{CC}.
7. Adjust V_{GRF1}, V_{GRF2} between −2 V and 0 V to achieve a total amplifier quiescent drain current of 240 mA.

LOCAL OSCILLATOR NULLING

Broad LO nulling may be required to achieve optimum IP3 and LO to RF isolation performance. This performance is achieved by applying dc voltages between −0.2 V and +0.2 V to the I and Q ports to suppress the LO signal across the RF frequency band by approximately 5 dBc to 10 dBc. To suppress the Lo signal at the RF port, use the following nulling sequence:

1. Adjust the V_{DC_IF1} input between −0.2 V and +0.2 V, and monitor the LO leakage on the RF port. When the desired or maximum level of suppression is achieved, proceed to Step 2.
2. Adjust the V_{DC_IF2} input between −0.2 V and +0.2 V, and monitor the LO leakage on the RF port until either the desired or maximum level of suppression is achieved.
3. If the desired level of the LO signal on the RF port has still not been achieved, further tune each V_{DC_IF1} or V_{DC_IF2} input independently to achieve the desired LO leakage. Ensure that the voltage resolution changed on the voltage of the V_{DC_IF1} and V_{DC_IF2} inputs is in the millivolt range.

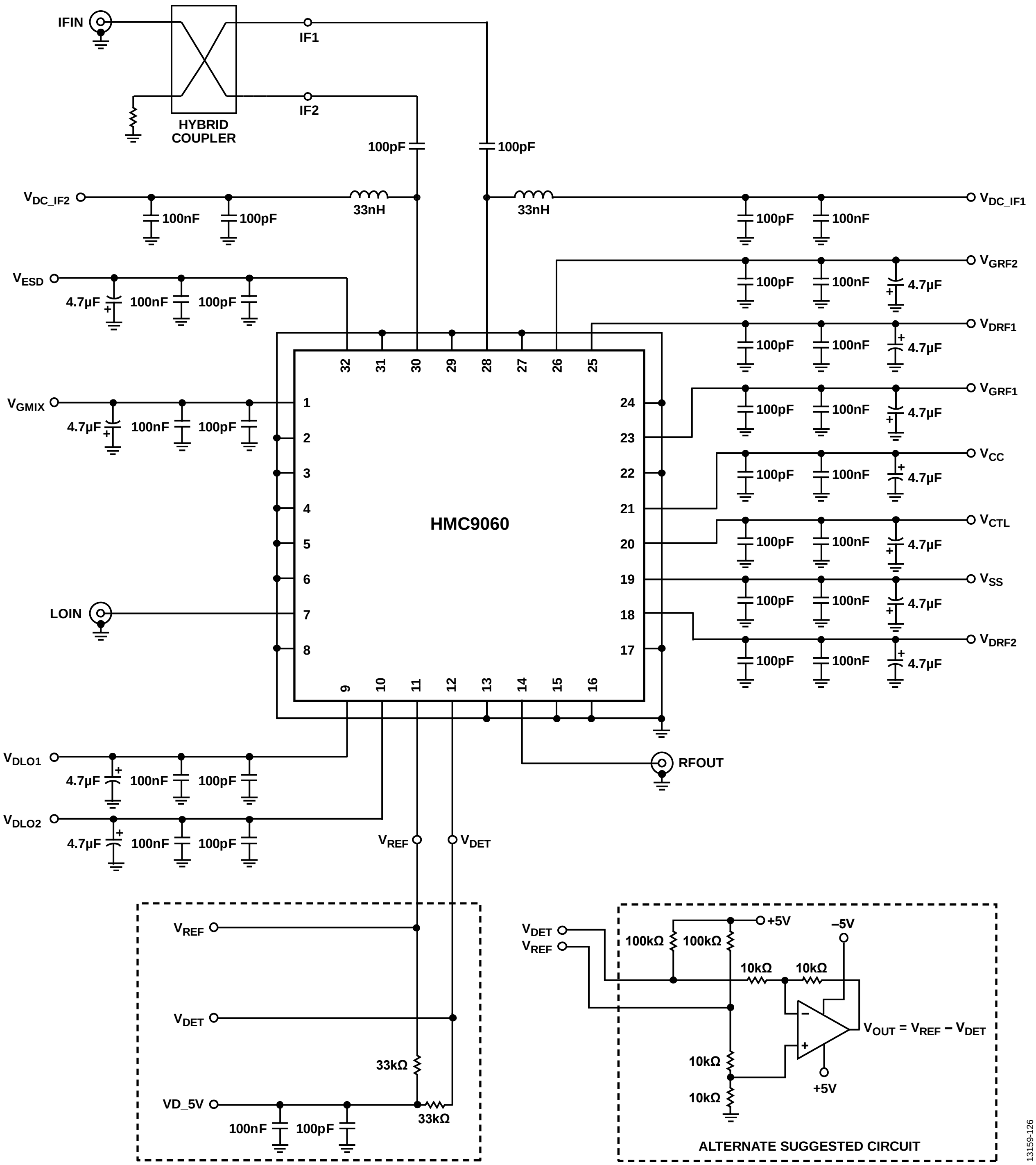

Figure 164. Typical Application Circuit

EVALUATION PRINTED CIRCUIT BOARD

For the circuit board used in the application, use RF circuit design techniques. Signal lines must have 50 Ω impedance, and the package ground leads and exposed pad must be connected directly to the ground plane similar to that shown in Figure 165.

Use a sufficient number of via holes to connect the top and bottom ground planes. The evaluation circuit board shown in Figure 165 is available from Analog Devices, Inc., upon request.

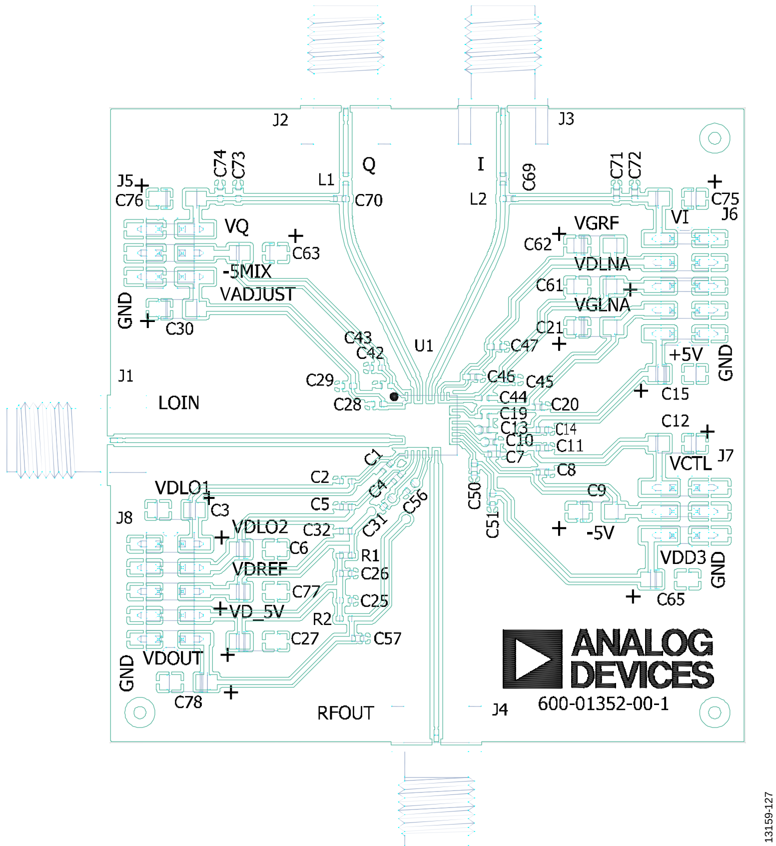

Figure 165. Evaluation Board Top Layer

OUTLINE DIMENSIONS

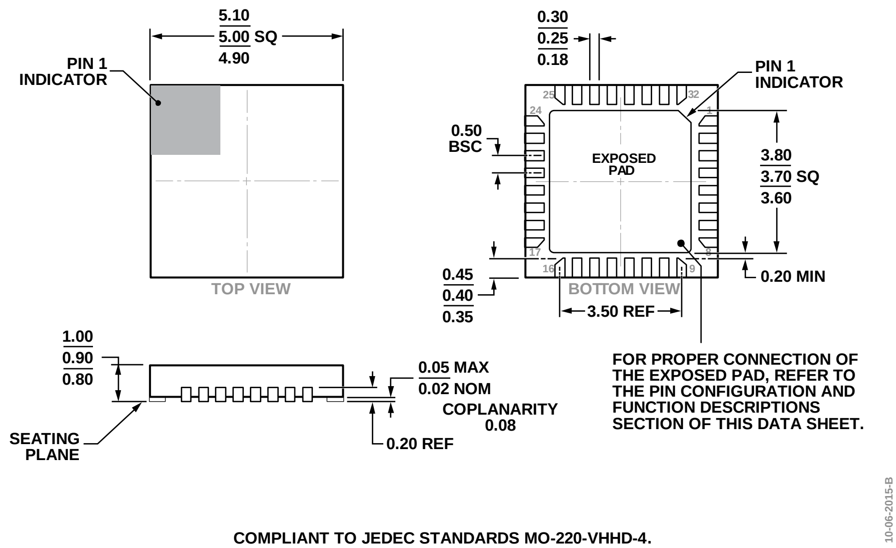

Figure 166. 32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
5 mm × 5 mm Body, Very Thin Quad
(HCP-32-2)
Dimensions shown in millimeters

PR13159-0-3/16(PrA)