

Pin Description

Pin No.	Pin Name	Pin Type	Description
1	Enable	I	Enables outputs when high and disables when low
2	NC	NA	Leave unconnected or grounded
3	NC	NA	Leave unconnected or grounded
4	GND	Power	Ground
5	FS0	I	Least significant bit for frequency selection
6	FS1	I	Middle bit for frequency selection
7	FS2	I	Most significant bit for frequency selection
8	Output1+	O	Positive HCSL Output 1
9	Output1-	O	Negative HCSL Output 1
10	Output 2-	O	Negative LVPECL Output 2
11	Output 2+	O	Positive LVPECL Output 2
12	VDD2	Power	Power Supply 2 for HCSL Output 2
13	VDD	Power	Power Supply
14	NC	NA	Leave unconnected or grounded

Operational Description

The DSC2042 is a dual oscillator with an HCSL output and an LVPECL output. The device consists of a MEMS resonator and a support PLL IC. The two outputs are generated through independent 8-bit programmable dividers from the output of the internal PLL. Two constraints are imposed on the output frequencies: 1) $f_2 = M \times f_1 / N$, where M and N are even integers between 4 and 254, 2) $1.2\text{GHz} < N \times f_2 < 1.7\text{GHz}$.

The actual frequencies output by the DSC2042 are controlled by an internal pre-programmed

memory (OTP). This memory stores all coefficients required by the PLL for up to eight different frequency combinations. Three control pins (FS0 – FS2) select the output frequency combination. Discera supports customer defined versions of the DSC2042. Standard frequency options are described in in the following sections.

When Enable (pin 1) is floated or connected to VDD, the DSC2042 is in operational mode. Driving Enable to ground will tri-state both output drivers (hi-impedance mode).

Output Clock Frequencies

Table 1 lists the standard frequency configurations and the associated ordering information to be used in conjunction with the ordering code. Customer defined combinations are available.

Table 1. Pre-programmed pin-selectable output frequency combinations

Ordering Info	Freq (MHz)	Freq Select Bits [FS2, FS1, FS0] – Default is [111]							
		000	001	010	011	100	101	110	111
M0001	f_{OUT1}	156.25	0*	0*	0*	0*	0*	0*	100
	f_{OUT2}	125	0*	0*	0*	0*	0*	0*	156.25
M0002	f_{OUT1}	100	156.25	0*	0*	0*	0*	0*	0*
	f_{OUT2}	100	156.25	0*	0*	0*	0*	0*	0*
MXXXXX	f_{OUT1}	Contact factory for additional configurations.							
	f_{OUT2}								

Frequency select bit are weakly tied high so if left unconnected the default setting will be [111] and the device will output the associated frequency highlighted in **Bold**.

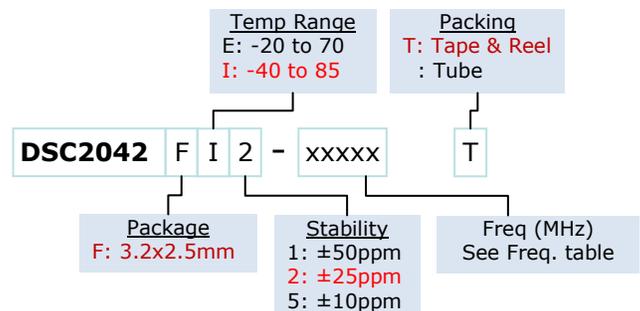
0* – denotes invalid selection, output frequency is not specified.

Absolute Maximum Ratings

Item	Min	Max	Unit	Condition
Supply Voltage	-0.3	+4.0	V	
Input Voltage	-0.3	$V_{DD}+0.3$	V	
Junction Temp	-	+150	°C	
Storage Temp	-55	+150	°C	
Soldering Temp	-	+260	°C	40sec max.
ESD	-		V	
HBM		4000		
MM		400		
CDM		1500		

Note: 1000+ years of data retention on internal memory

Ordering Code



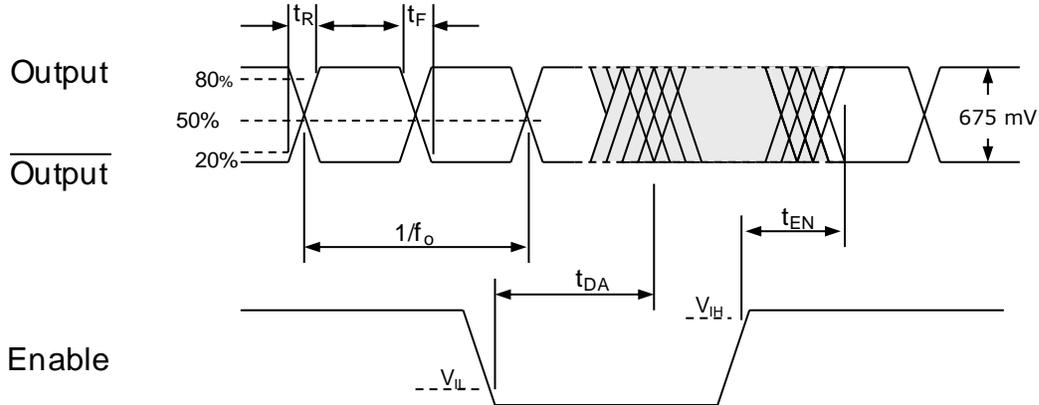
Specifications (Unless specified otherwise: T=25° C)

Parameter		Condition	Min.	Typ.	Max.	Unit
Supply Voltage ¹	V _{DD}		2.25		3.6	V
Supply Current	I _{DD}	EN pin low – outputs are disabled		21	23	mA
Supply Current ²	I _{DD}	EN pin high – outputs are enabled R _L =50Ω, F _{O1} = F _{O2} =156.25 MHz		76		mA
Frequency Stability	Δf	Includes frequency variations due to initial tolerance, temp. and power supply voltage			±10 ±25 ±50	ppm
Aging	Δf	1 year @25°C			±5	ppm
Startup Time ³	t _{SU}	T=25°C			5	ms
Input Logic Levels						
Input logic high	V _{IH}		0.75xV _{DD}		-	V
Input logic low	V _{IL}		-		0.25xV _{DD}	
Output Disable Time ⁴	t _{DA}				5	ns
Output Enable Time	t _{EN}				20	ns
Pull-Up Resistor ²		Pull-up exists on all digital IO		40		kΩ
LVPECL Outputs						
Output Logic Levels						
Output logic high	V _{OH}	R _L =50Ω	V _{DD} -1.08		-	V
Output logic low	V _{OL}		-		V _{DD} -1.55	
Pk to Pk Output Swing		Single-Ended		800		mV
Output Transition time ⁴						
Rise Time	t _R	20% to 80% R _L =50Ω		250		ps
Fall Time	t _F					
Frequency	f ₀	Single Frequency	2.3		460	MHz
Output Duty Cycle	SYM	Differential	48		52	%
Period Jitter ⁵	J _{PER}	F _{O1} =125 MHz		2.5		ps _{RMS}
Integrated Phase Noise	J _{CC}	200kHz to 20MHz @156.25MHz 100kHz to 20MHz @156.25MHz 12kHz to 20MHz @156.25MHz		0.25 0.38 1.7	2	ps _{RMS}
HCSL Outputs						
Output Logic Levels						
Output logic high	V _{OH}	R _L =50Ω	0.725		-	V
Output logic low	V _{OL}		-		0.1	
Pk to Pk Output Swing		Single-Ended		750		mV
Output Transition time ⁴						
Rise Time	t _R	20% to 80% R _L =50Ω, C _L = 2pF		200	400	ps
Fall Time	t _F					
Frequency	f ₀	Single Frequency	2.3		460	MHz
Output Duty Cycle	SYM	Differential	48		52	%
Period Jitter ⁵	J _{PER}	F _{O1} =F _{O2} =156.25 MHz		2.8		ps _{RMS}
Integrated Phase Noise	J _{PH}	200kHz to 20MHz @156.25MHz 100kHz to 20MHz @156.25MHz 12kHz to 20MHz @156.25MHz		0.25 0.37 1.7	2	ps _{RMS}

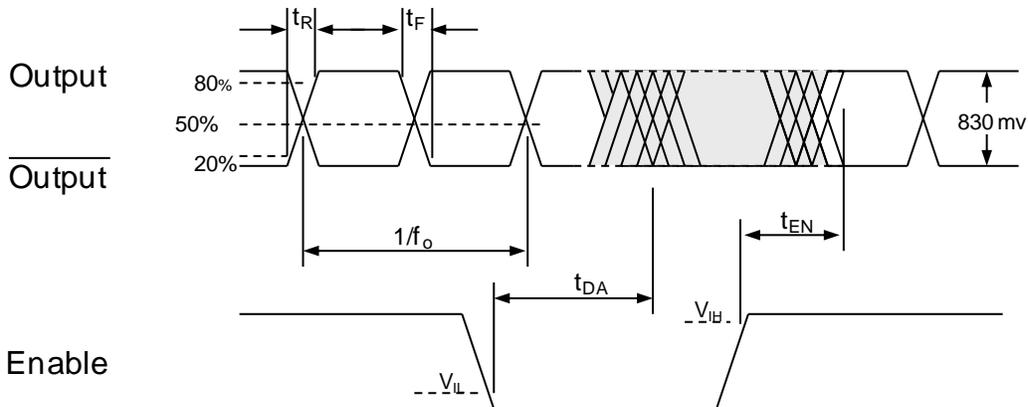
Notes:

- Pin 4 V_{DD} should be filtered with 0.01uF capacitor.
- Output is enabled if Enable pad is floated or not connected.
- t_{SU} is time to 100PPM stable output frequency after V_{DD} is applied and outputs are enabled.
- Output Waveform and Test Circuit figures below define the parameters.
- Period Jitter includes crosstalk from adjacent output.

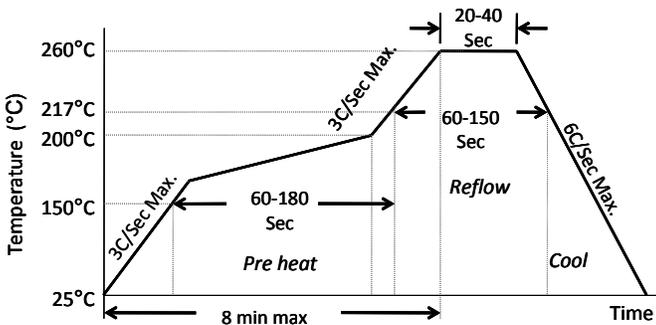
Output Waveform: HCSL



Output Waveform: LVPECL



Solder Reflow Profile



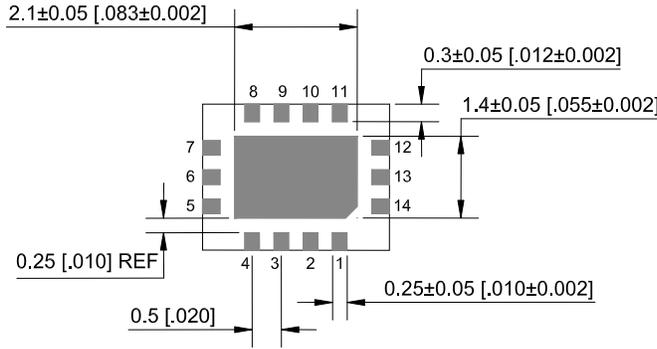
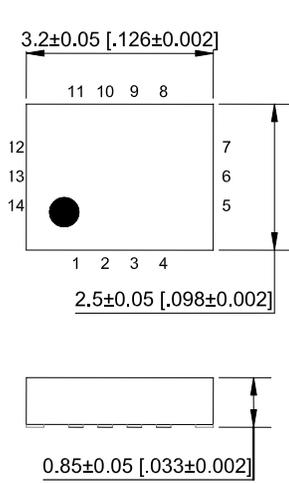
MSL 1 @ 260°C refer to JSTD-020C	
Ramp-Up Rate (200°C to Peak Temp)	3°C/Sec Max.
Preheat Time 150°C to 200°C	60-180 Sec
Time maintained above 217°C	60-150 Sec
Peak Temperature	255-260°C
Time within 5°C of actual Peak	20-40 Sec
Ramp-Down Rate	6°C/Sec Max.
Time 25°C to Peak Temperature	8 min Max.

Package Dimensions

3.2 x 2.5 mm 14 Lead Plastic Package

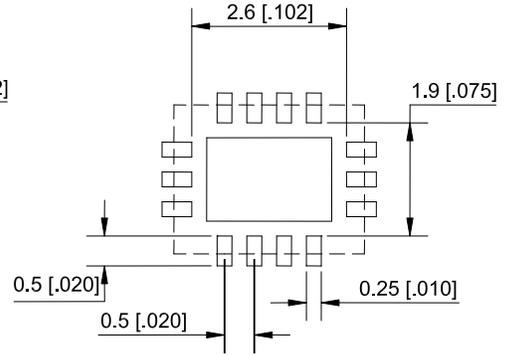
External Dimensions

units: mm[inch]



Recommended Solder Pad Layout

units: mm[inch]



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