HMC463

v11.0617

GaAs PHEMT MMIC LOW NOISE AGC AMPLIFIER, 2 - 20 GHz

Typical Applications

The HMC463 is ideal for:

- Telecom Infrastructure
- Microwave Radio & VSAT
- Military & Space
- Test Instrumentation
- Fiber Optics

Features

Gain: 14 dB

Noise Figure: 2.5 dB @ 10 GHz

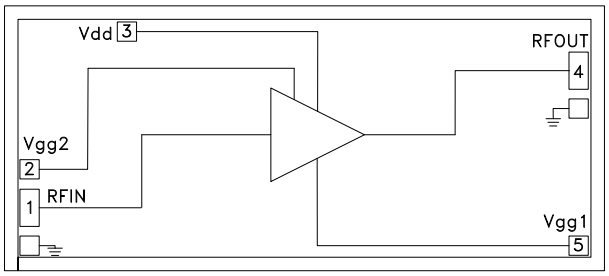
P1dB Output Power: +19 dBm @ 10 GHz

Supply Voltage: +5V @ 60 mA

50 Ohm Matched Input/Output

Die Size: 3.05 x 1.29 x 0.1 mm

Functional Diagram



Vgg2: Optional Gate Bias for AGC

General Description

The HMC463 is a GaAs MMIC PHEMT Low Noise AGC Distributed Amplifier die which operates between 2 and 20 GHz. The amplifier provides 14 dB of gain, 2.5 dB noise figure and 19 dBm of output power at 1 dB gain compression while requiring only 60 mA from a +5V supply. An optional gate bias (Vgg2) is provided to allow Adjustable Gain Control (AGC) of 10 dB typical. Gain flatness is excellent at ±0.15 dB from 6 - 18 GHz making the HMC463 ideal for EW, ECM and RADAR applications. The HMC463 amplifier can easily be integrated into Multi-Chip-Modules (MCMs) due to its small size. All data is with the chip in a 50 Ohm test fixture connected via 0.025mm (1 mil) diameter wire bonds of minimal length 0.31mm (12 mils).

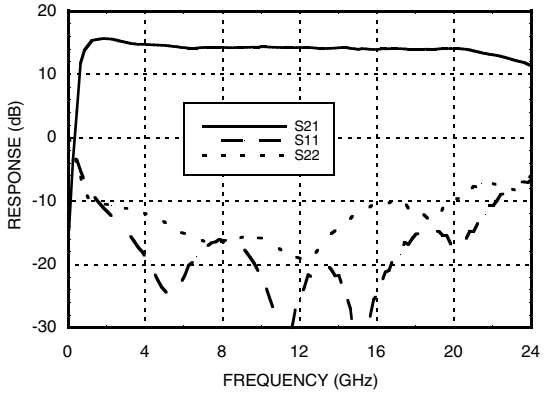
Electrical Specifications, T_A = +25° C, Vdd= 5V, Idd= 60 mA*

Parameter	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Units
Frequency Range		2.0 - 6.0			6.0 - 18.0			18.0 - 20.0		GHz
Gain	12	15		12	14		12	14		dB
Gain Flatness		±1.0			±0.15			±0.15		dB
Gain Variation Over Temperature		0.015	0.025		0.015	0.025		0.015	0.025	dB/ °C
Noise Figure		3.0	4.0		2.5	3.7		3.5	4.0	dB
Input Return Loss		12			15			14		dB
Output Return Loss		11			12			10		dB
Output Power for 1 dB Compression (P1dB)	16	19		13	16		11	14		dBm
Saturated Output Power (Psat)		21			20			19		dBm
Output Third Order Intercept (IP3)		31			28			26		dBm
Supply Current (Idd) (Vdd= 5V, Vgg1= -0.9V Typ.)		60	80		60	80		60	80	mA

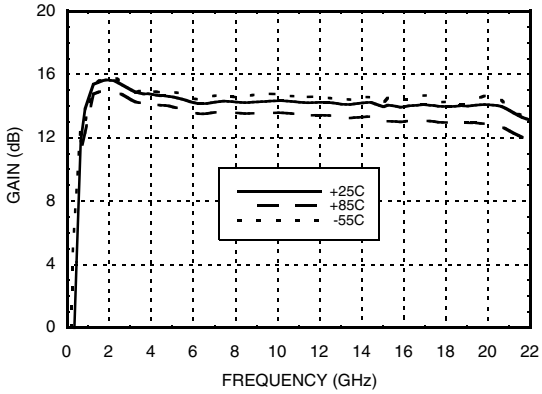
** Adjust Vgg1 between -1.5 to -0.5V to achieve Idd= 60 mA typical.*

For price, delivery, and to place orders: Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106
Phone: 781-329-4700 • Order online at www.analog.com
Application Support: Phone: 1-800-ANALOG-D

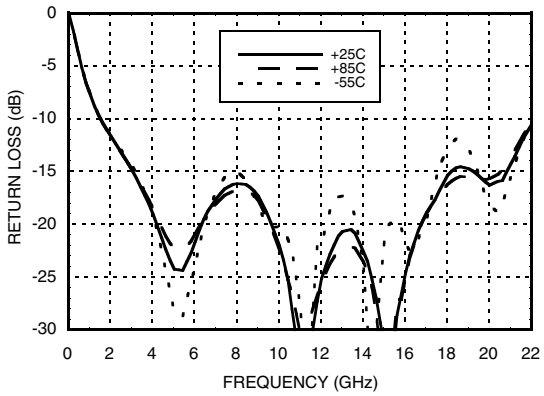
Gain & Return Loss



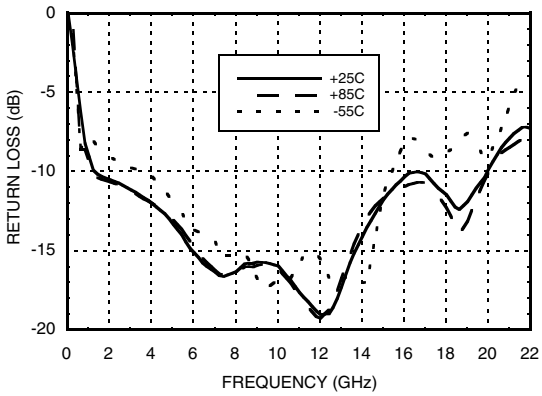
Gain vs. Temperature



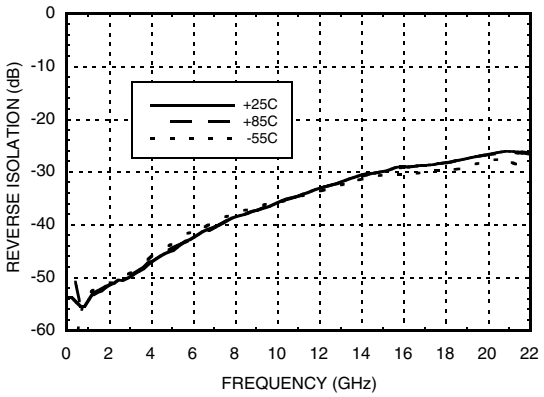
Input Return Loss vs. Temperature



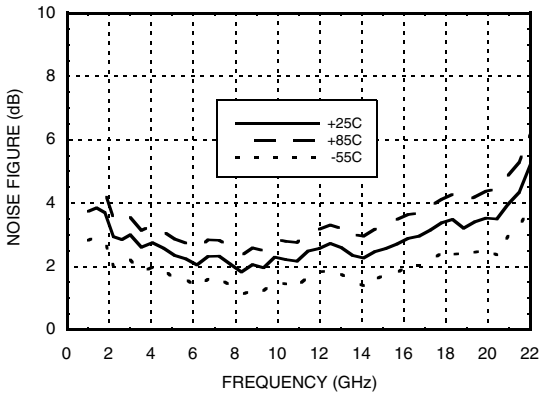
Output Return Loss vs. Temperature



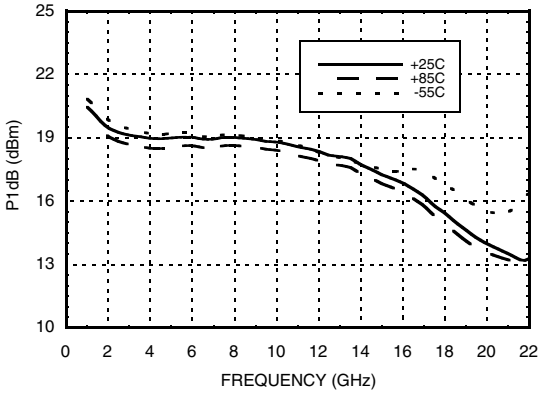
Reverse Isolation vs. Temperature



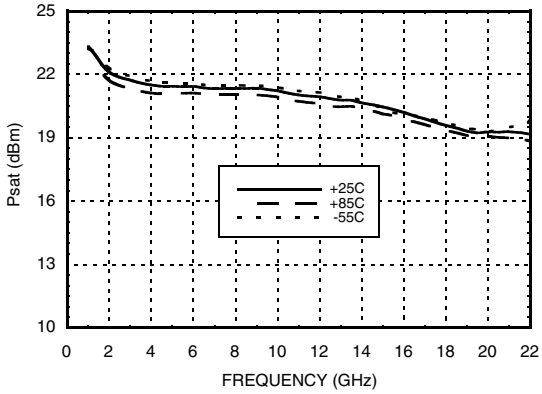
Noise Figure vs. Temperature



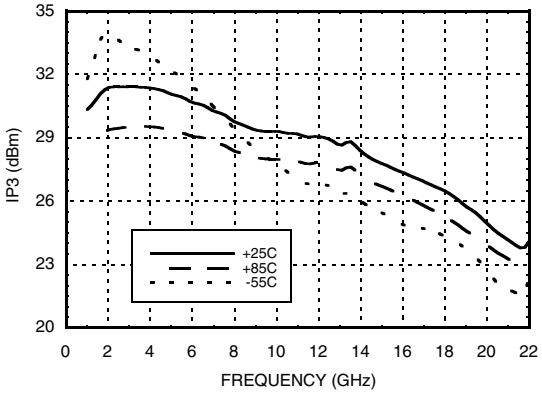
P1dB vs. Temperature



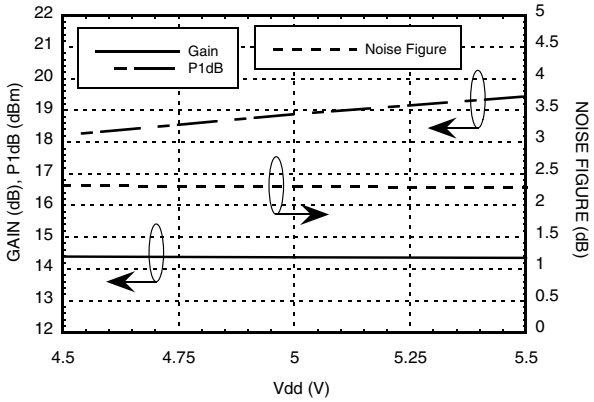
Psat vs. Temperature



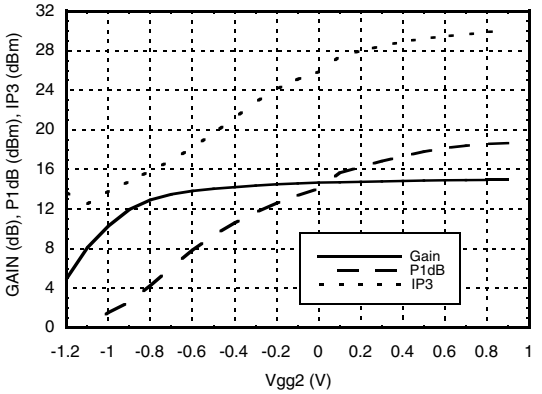
Output IP3 vs. Temperature



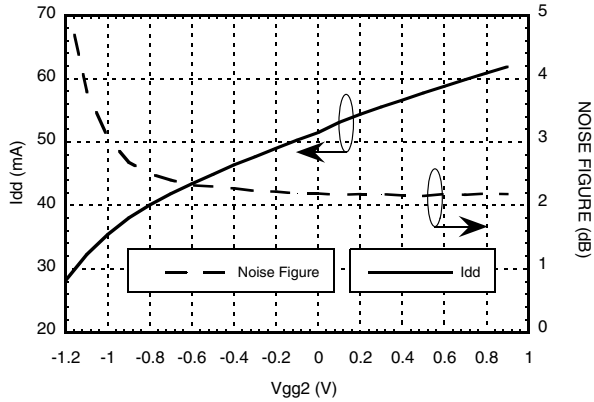
Gain, Power & Noise Figure vs. Supply Voltage @ 10 GHz, Fixed Vgg1



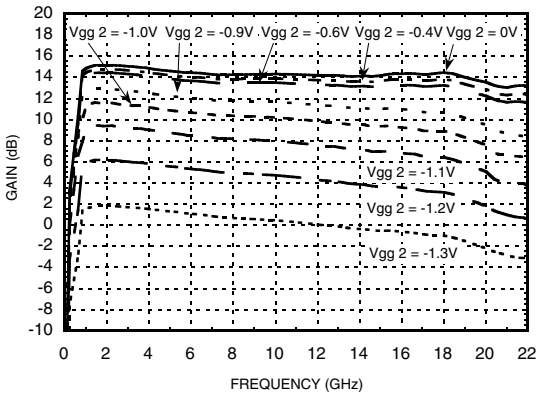
Gain, P1dB & Output IP3 vs. Control Voltage @ 10 GHz



Noise Figure & Supply Current vs. Control Voltage @ 10 GHz



Gain @ Several Control Voltages



Absolute Maximum Ratings

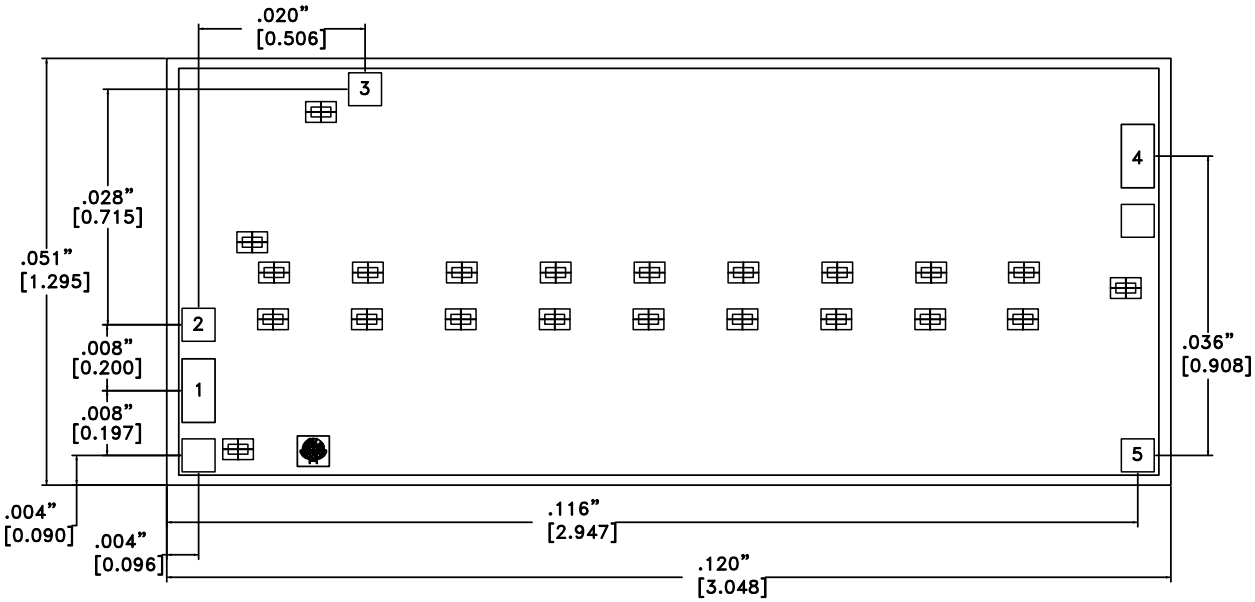
Drain Bias Voltage (Vdd)	+9 V
Gate Bias Voltage (Vgg1)	-2 to 0 Vdc
Gate Bias Current (Igg1)	2.5 mA
Gate Bias Voltage (Vgg2)(AGC)	(Vdd -9) Vdc to +2 Vdc
RF Input Power (RFIN)(Vdd = +5 V)	+18 dBm
Channel Temperature	175 °C
Continuous Pdiss (T= 85 °C) (derate 20.6 mW/°C above 85 °C)	1.85 W
Thermal Resistance (channel to die bottom)	48.6 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-55 to +85 °C
ESD Sensitivity (HBM)	Class 0B - Passed 150V

Typical Supply Current vs. Vdd

Vdd (V)	Idd (mA)
+4.5	58
+5.0	60
+5.5	62

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



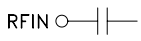
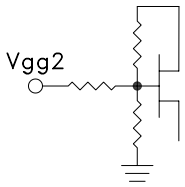
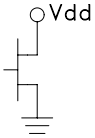
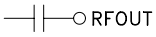
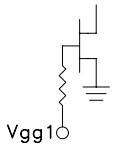
Die Packaging Information [1]

Standard	Alternate
GP-2 (Gel Pack)	[2]

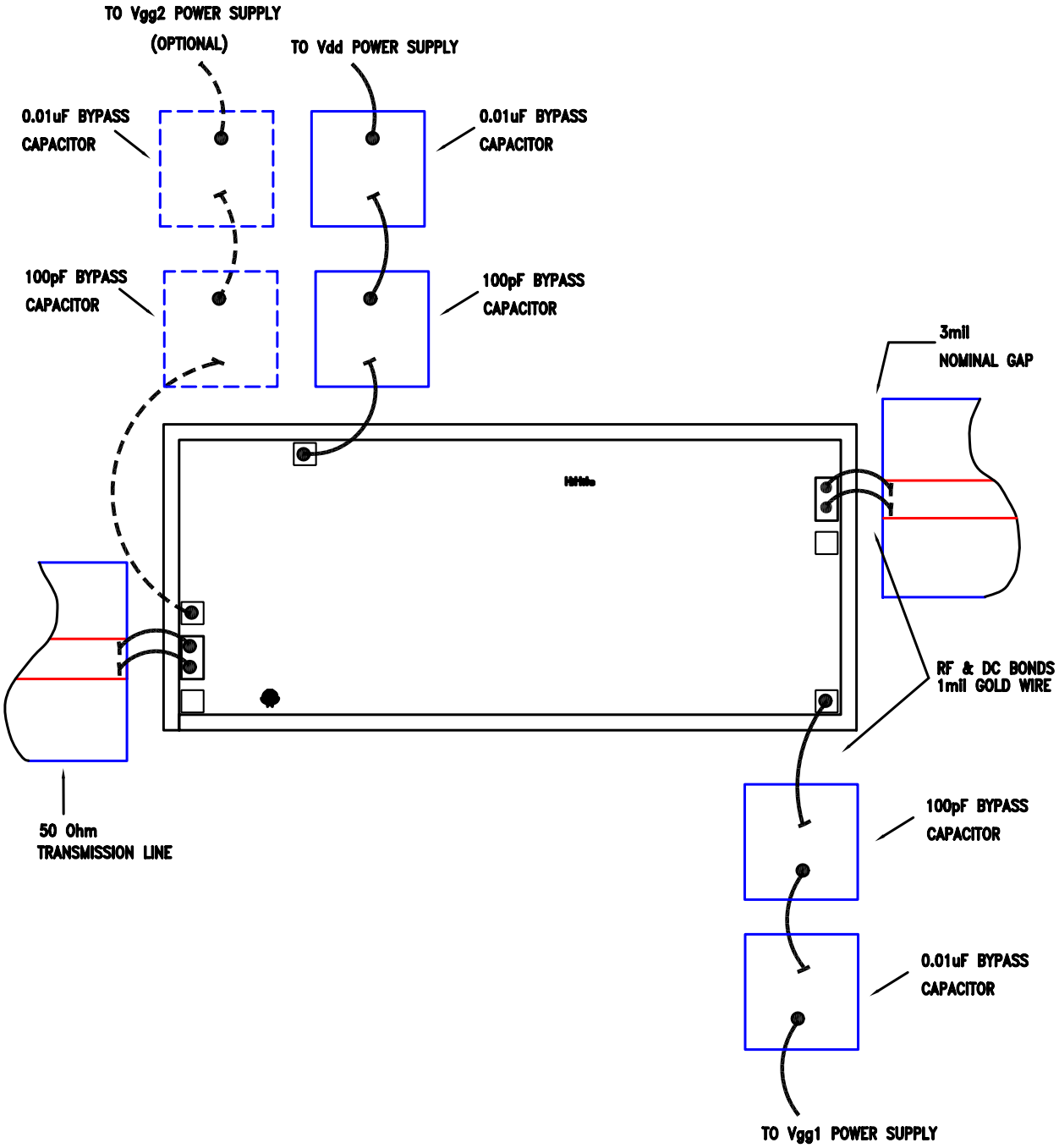
[1] Refer to the "Packaging Information" section for die packaging dimensions.
[2] For alternate packaging information contact Analog Devices, Inc.

NOTES:
1. ALL DIMENSIONS IN INCHES [MILLIMETERS]
2. NO CONNECTION REQUIRED FOR UNLABELED BOND PADS
3. DIE THICKNESS IS 0.004 (0.100)
4. TYPICAL BOND PAD IS 0.004 (0.100) SQUARE
5. BACKSIDE METALLIZATION: GOLD
6. BACKSIDE METAL IS GROUND
7. BOND PAD METALIZATION: GOLD
8. OVERALL DIE SIZE ±.002"

Pad Descriptions

Pad Number	Function	Description	Interface Schematic
1	RFIN	This pad is AC coupled and matched to 50 Ohms.	
2	Vgg2	Optional gate control if AGC is required. Leave Vgg2 open circuited if AGC is not required.	
3	Vdd	Power supply voltage for the amplifier. External bypass capacitors are required	
4	RFOUT	This pad is AC coupled and matched to 50 Ohms.	
5	Vgg1	Gate control for amplifier. Adjust to achieve Idd= 60 mA.	
Die Bottom	GND	Die bottom must be connected to RF/DC ground.	

Assembly Diagram



Mounting & Bonding Techniques for Millimeterwave GaAs MMICs

The die should be attached directly to the ground plane eutectically or with conductive epoxy (see HMC general Handling, Mounting, Bonding Note).

50 Ohm Microstrip transmission lines on 0.127mm (5 mil) thick alumina thin film substrates are recommended for bringing RF to and from the chip (Figure 1). If 0.254mm (10 mil) thick alumina thin film substrates must be used, the die should be raised 0.150mm (6 mils) so that the surface of the die is coplanar with the surface of the substrate. One way to accomplish this is to attach the 0.102mm (4 mil) thick die to a 0.150mm (6 mil) thick molybdenum heat spreader (moly-tab) which is then attached to the ground plane (Figure 2).

Microstrip substrates should brought as close to the die as possible in order to minimize bond wire length. Typical die-to-substrate spacing is 0.076mm to 0.152 mm (3 to 6 mils).

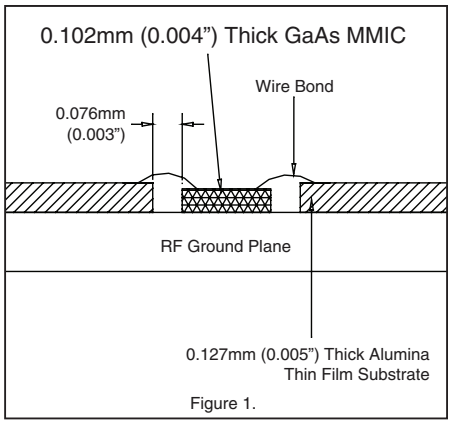


Figure 1.

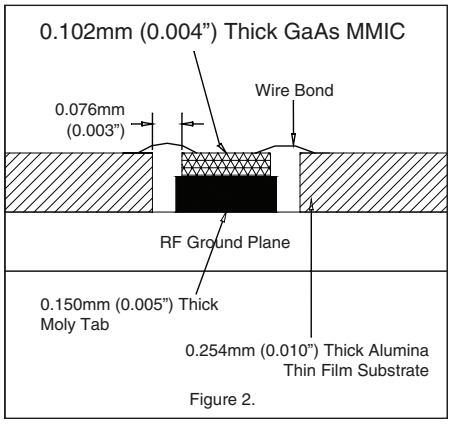


Figure 2.

Handling Precautions

Follow these precautions to avoid permanent damage.

Storage: All bare die are placed in either Waffle or Gel based ESD protective containers, and then sealed in an ESD protective bag for shipment. Once the sealed ESD protective bag has been opened, all die should be stored in a dry nitrogen environment.

Cleanliness: Handle the chips in a clean environment. DO NOT attempt to clean the chip using liquid cleaning systems.

Static Sensitivity: Follow ESD precautions to protect against ESD strikes.

Transients: Suppress instrument and bias supply transients while bias is applied. Use shielded signal and bias cables to minimize inductive pick-up.

General Handling: Handle the chip along the edges with a vacuum collet or with a sharp pair of bent tweezers. The surface of the chip has fragile air bridges and should not be touched with vacuum collet, tweezers, or fingers.

Mounting

The chip is back-metallized and can be die mounted with AuSn eutectic preforms or with electrically conductive epoxy. The mounting surface should be clean and flat.

Eutectic Die Attach: A 80/20 gold tin preform is recommended with a work surface temperature of 255 °C and a tool temperature of 265 °C. When hot 90/10 nitrogen/hydrogen gas is applied, tool tip temperature should be 290 °C. DO NOT expose the chip to a temperature greater than 320 °C for more than 20 seconds. No more than 3 seconds of scrubbing should be required for attachment.

Epoxy Die Attach: Apply a minimum amount of epoxy to the mounting surface so that a thin epoxy fillet is observed around the perimeter of the chip once it is placed into position. Cure epoxy per the manufacturer's schedule.

Wire Bonding

Ball or wedge bond with 0.025mm (1 mil) diameter pure gold wire. Thermosonic wirebonding with a nominal stage temperature of 150 °C and a ball bonding force of 40 to 50 grams or wedge bonding force of 18 to 22 grams is recommended. Use the minimum level of ultrasonic energy to achieve reliable wirebonds. Wirebonds should be started on the chip and terminated on the package or substrate. All bonds should be as short as possible <0.31mm (12 mils).