PRELIMINARY

FEMTOCLOCKS™ CRYSTAL-TO-LVPECL 350MHZ FREQUENCY SYNTHESIZER

ICS843207B-350

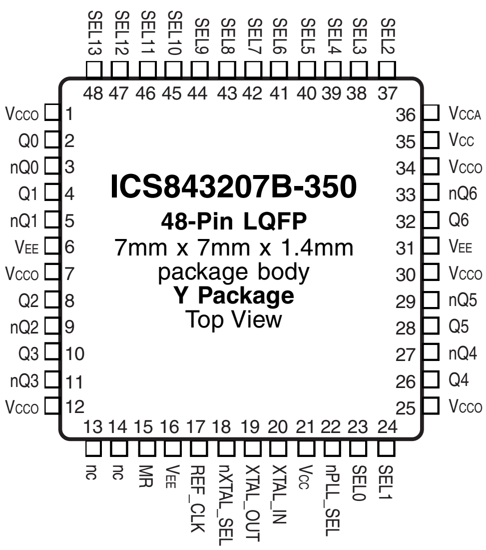
General Description

The ICS843207B-350 is a low phase-noise frequency synthesizer that targets clocking for high performance interfaces such as SPI4.2 and is a member of the HiPerClockS™ family of high performance clock solutions from IDT. In the default mode, each output can be configured individually to generate an 87.5MHz, 175MHZ or 350MHz LVPECL output clock signal from a 14MHz crystal input. The ICS843207B-350 is provided in a 48-pin LQFP package.

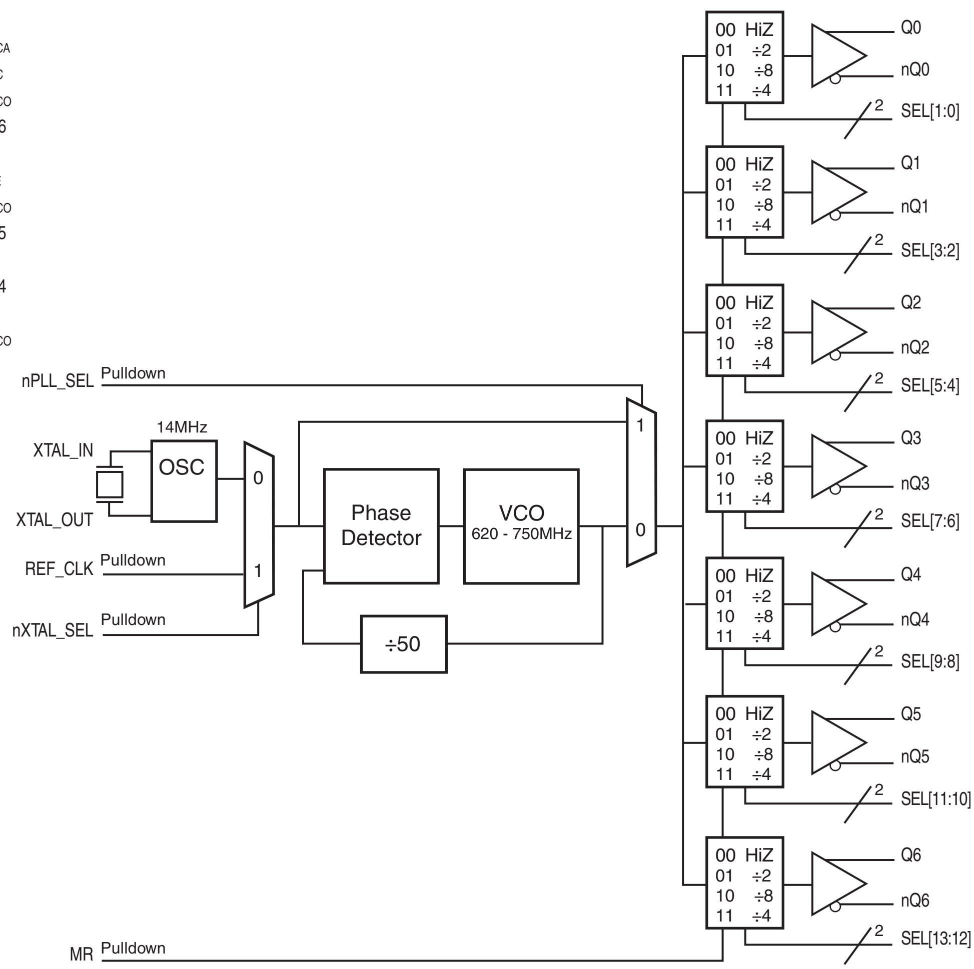
Features

- Seven independently configurable LVPECL outputs at 87.5MHz, 175MHz or 350MHz
- Individual high impedance control of each output
- Selectable crystal oscillator interface designed for 14MHz, 18pF parallel resonant crystal or LVCMOS single-ended input
- VCO range: 620MHz - 750MHz
- Full 3.3V supply mode
- 0°C to 70°C ambient operating temperature
- Available in both standard (RoHS 5) and lead-free (RoHS 6) packages

Pin Assignment



Block Diagram



The Preliminary Information presented herein represents a product in pre-production. The noted characteristics are based on initial product characterization and/or qualification. Integrated Device Technology, Incorporated (IDT) reserves the right to change any circuitry or specifications without notice.

Functional Description

The ICS843207B-350 features a fully integrated PLL and therefore requires no external components for setting the loop bandwidth. A 14MHz fundamental crystal is used as the input to the on chip oscillator. The VCO of the PLL operates over a range of 620MHz to 750MHz. The output of the M divider is also applied to the phase detector. The default mode for the ICS843207B-350 is a nominal VCO frequency of 700MHz with each output configurable to divide by 2, 4 or 8. The divider provides a 50% output duty cycle. The relationship between the crystal input frequency, the M divider, the VCO frequency and the output frequency is provided in Table 1.

Table 1. Frequency Select Function Table

XTAL (MHz)	SELx	SELx-1	VCO (MHz)	Output Divider	Output Frequency (MHz)
14	0	0	700	N/A	HiZ
14	0	1	700	2	350
14	1	0	700	8	87.5
14	1	1	700	4	175 (default)

TABLE 2. PIN DESCRIPTIONS

Number	Name	Type		Description
1, 7, 12, 25, 30, 34	V_{CCO}	Power		Output supply pins.
2, 3	Q0, nQ0	Ouput		Differential output pair. LVPECL interface levels.
4, 5	Q1, nQ1	Ouput		Differential output pair. LVPECL interface levels.
6, 16, 31	V_{EE}	Power		Negative supply pins.
8, 9	Q2, nQ2	Ouput		Differential output pair. LVPECL interface levels.
10, 11	Q3, nQ3	Ouput		Differential output pair. LVPECL interface levels.
13, 14	nc	Unused		No connect.
15	MR	Input	Pulldown	Active High Master Reset. When logic HIGH, the internal dividers are reset causing the true outputs Qx to go LOW and inverted outputs nQx to go HIGH. When logic LOW, the internal dividers and the outputs are enabled. LVCMOS/LVTTL interface levels.
17	REF_CLK	Input	Pulldown	Reference input clock. LVCMOS/LVTTL interface levels.
18	nXTAL_SEL	Input	Pulldown	Crystal select pin. Selects between the crystal and the reference clock inputs. LVCMOS/LVTTL interface levels.
19, 20	XTAL_OUT, XTAL_IN	Input		Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input.
21, 35	V_{CC}	Power		Core supply pins.
22	nPLL_SEL	Input	Pulldown	PLL select pin. When HIGH, PLL is bypassed and input is fed directly to the output dividers. When LOW, PLL is enabled. LVCMOS/LVTTL interface levels.
23, 24, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48	SEL0, SEL1, SEL2, SEL3, SEL4, SEL5, SEL6, SEL7, SEL8, SEL9, SEL10, SEL11, SEL12, SEL13	Input	Pullup	Output divider select pins. See Table 1A. LVCMOS/LVTTL interface levels.
26, 27	Q4, nQ4	Ouput		Differential output pair. LVPECL interface levels.
28, 29	Q5, nQ5	Ouput		Differential output pair. LVPECL interface levels.
32, 33	Q6, nQ6	Ouput		Differential output pair. LVPECL interface levels.
36	V_{CCA}	Power		Analog supply pin.

NOTE: *Pullup and Pulldown* refer to internal input resistors. See Table 2, Pin Characteristics, for typical values.

TABLE 3. PIN CHARACTERISTICS

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance			4		pF
$R_{PULLDOWN}$	Input Pulldown Resistor			51		kΩ
R_{PULLUP}	Input Pulldown Resistor			51		kΩ

TABLE 4A. nXTAL_SEL CONTROL INPUT FUNCTION TABLE

Input	
nXTAL_SEL	**Selected Source**
0	XTAL_IN, XTAL_OUT
1	REF_CLK

ABSOLUTE MAXIMUM RATINGS

Supply Voltage, V_{CC}	4.6V
Inputs, V_I	-0.5V to V_{CC} + 0.5V
Outputs, I_O	
Continuous Current	50mA
Surge Current	100mA
Package Thermal Impedance, θ_{JA}	65.7°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

NOTE: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics* or *AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

TABLE 5A. POWER SUPPLY DC CHARACTERISTICS, $V_{CC} = V_{CCO}$ = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{CC}	Core Supply Voltage		3.135	3.3	3.465	V
V_{CCA}	Analog Supply Voltage		V_{CC} – 0.13	3.3	V_{CC}	V
V_{CCO}	Output Supply Voltage		3.135	3.3	3.465	V
I_{EE}	Power Supply Current				210	mA
I_{CCA}	Analog Supply Current				13	mA

TABLE 5B. LVCMOS / LVTTL DC CHARACTERISTICS, $V_{CC} = V_{CCO}$ = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage		V_{CC} = 3.3V	2		V_{CC} + 0.3	V
V_{IL}	Input Low Voltage		V_{CC} = 3.3V	-0.3		0.8	V
I_{IH}	Input High Current	MR, nXTAL_SEL, REF_CLK, nPLL_SEL	$V_{CC} = V_{IN}$ = 3.465			150	µA
		SEL[0:13]	$V_{CC} = V_{IN}$ = 3.465			5	µA
I_{IL}	Input Low Current	MR, nXTAL_SEL, REF_CLK, nPLL_SEL	V_{CC} = 3.465V, V_{IN} = 0V	-5			µA
		SEL[0:13]	V_{CC} = 3.465V, V_{IN} = 0V	-150			µA
$\Delta t/\Delta v$	Input Transition Rise/Fall Rate	SEL[0:13], MODE				20	ns/V

TABLE 5C. LVPECL DC CHARACTERISTICS, $V_{CC} = V_{CCO}$ = 3.3V±5%, TA = 0°C TO 70°C

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{OH}	Output High Voltage; NOTE 1		V_{CCO} - 1.4		V_{CCO} - 0.9	V
V_{OL}	Output Low Voltage; NOTE 1		V_{CCO} - 2.0		V_{CCO} - 1.7	V
V_{SWING}	Peak-to-Peak Output Voltage Swing		0.6		1.0	V

NOTE 1: Outputs terminated with 50Ω to V_{CCO} - 2V.

TABLE 6. CRYSTAL CHARACTERISTICS

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation		Fundamental			
Frequency		12.4	14	15	MHz
Equivalent Series Resistance (ESR)				40	Ω
Shunt Capacitance				7	pF
Drive Level				300	µW

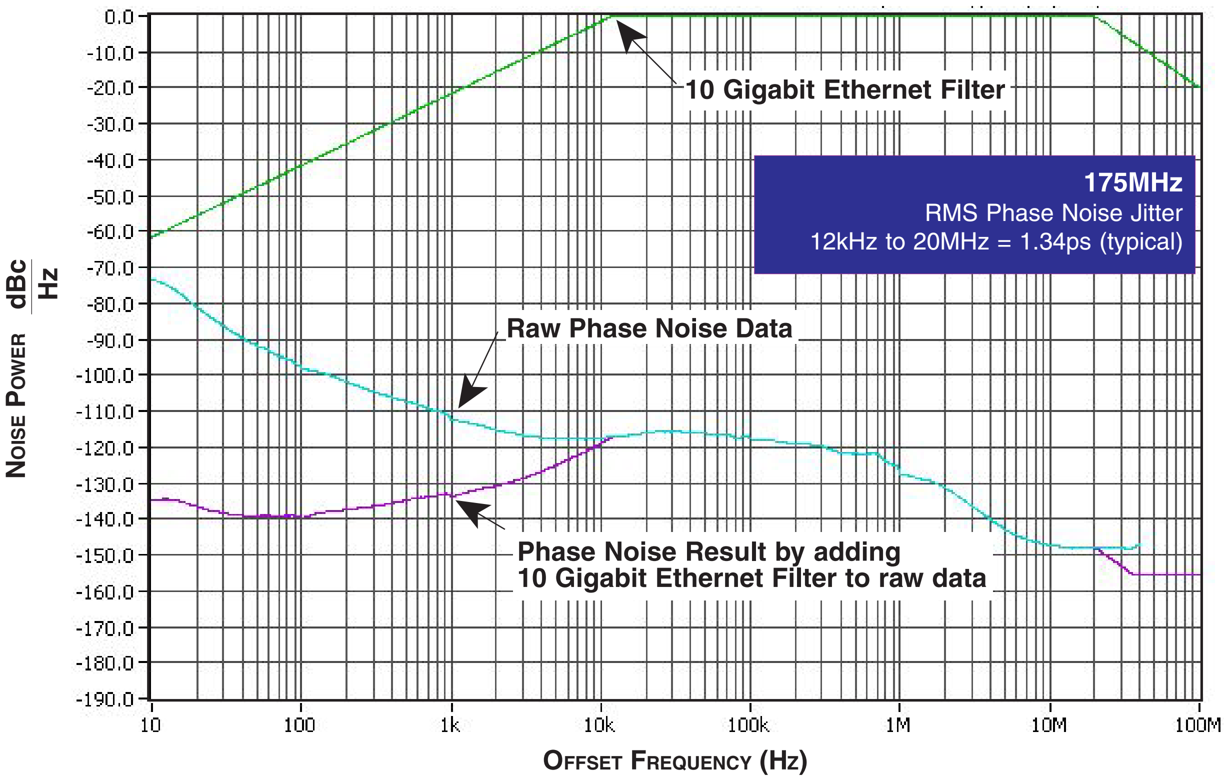
NOTE: Characterized using an 18pF parallel resonant crystal.

TABLE 7. AC CHARACTERISTICS, $V_{CC} = V_{CCO}$ = 3.3V±5%, TA = 0°C TO 70°C

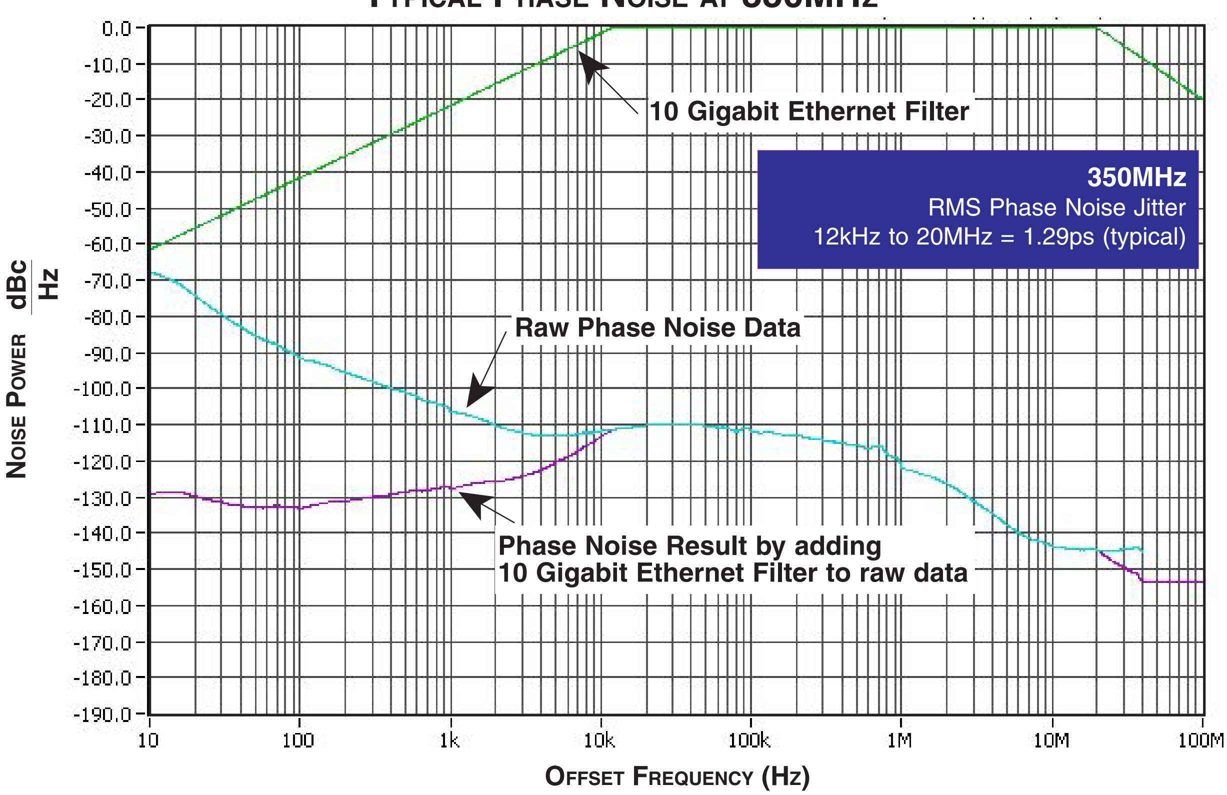
Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency		N = ÷2	310	350	375	MHz
			N = ÷4	155	175	187.5	MHz
			N = ÷8	77.5	87.5	93.75	MHz
f_{IN}	Input Frequency	REF_CLK		12.4	14	15	MHz
*t*jit(Ø)	RMS Phase Jitter, Random; NOTE 1		350MHz, (12kHz - 20MHz)		1.29		ps
			175MHz, (12kHz - 20MHz)		1.34		ps
			87.5MHz, (12kHz - 20MHz)		1.46		ps
t_R / t_F	Output Rise/Fall Time		20% to 80%	300		600	ps
odc	Output Duty Cycle		Output Divider = ÷2	42		58	%
			Output Divider = ≠2	46		54	%

NOTE 1: Characterized using a 14MHz crystal.

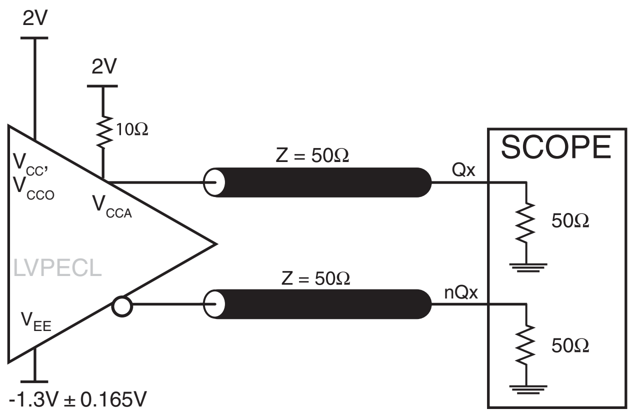
Typical Phase Noise at 175MHz



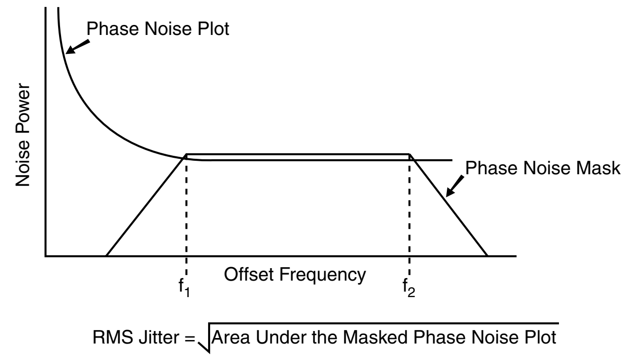
Typical Phase Noise at 350MHz



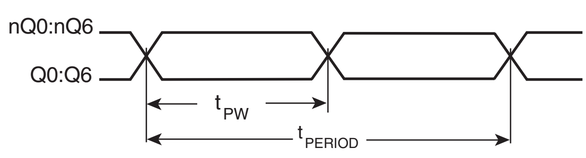
Parameter Measurement Information



3.3V Core/3.3V Output Load AC Test Circuit

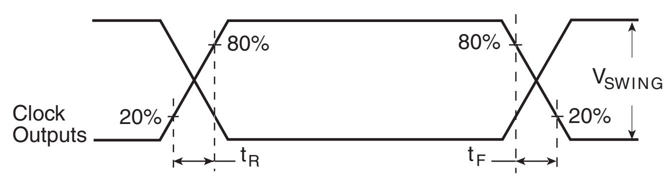


RMS Phase Jitter



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

Output Duty Cycle/Pulse Width/Period



Output Rise/Fall Time

Application Information

Power Supply Filtering Techniques

As in any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The ICS843207B-350 provides separate power supplies to isolate any high switching noise from the outputs to the internal PLL. V_{CC}, V_{CCA} and V_{CCO} should be individually connected to the power supply plane through vias, and 0.01µF bypass capacitors should be used for each pin. *Figure 1* illustrates this for a generic V_{CC} pin and also shows that V_{CCA} requires that an additional 10Ω resistor along with a 10µF bypass capacitor be connected to the V_{CCA} pin.

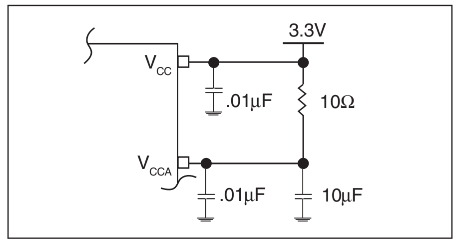


Figure 1. Power Supply Filtering

Crystal Input Interface

The ICS843207B-350 has been characterized with 18pF parallel resonant crystals. The capacitor values shown in *Figure 2* below were determined using a 14MHz, 18pF parallel resonant crystal and were chosen to minimize the ppm error.

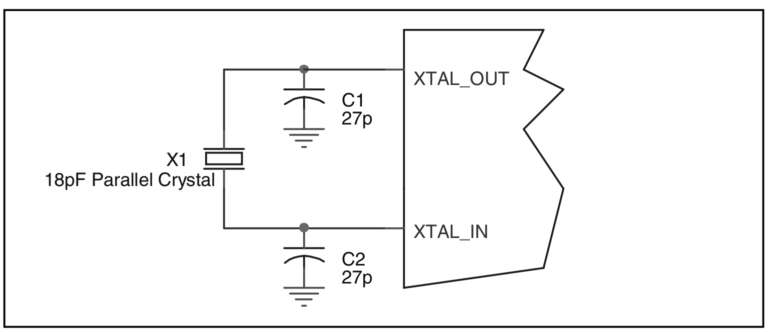


Figure 2. Crystal Input Interface

LVCMOS to XTAL Interface

The XTAL_IN input can accept a single-ended LVCMOS signal through an AC couple capacitor. A general interface diagram is shown in *Figure 3.* The XTAL_OUT pin can be left floating. The input edge rate can be as slow as 10ns. For LVCMOS inputs, it is recommended that the amplitude be reduced from full swing to half swing in order to prevent signal interference with the power rail and to reduce noise. This configuration requires that the output impedance of the driver (Ro) plus the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways. First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and making R2 50Ω.

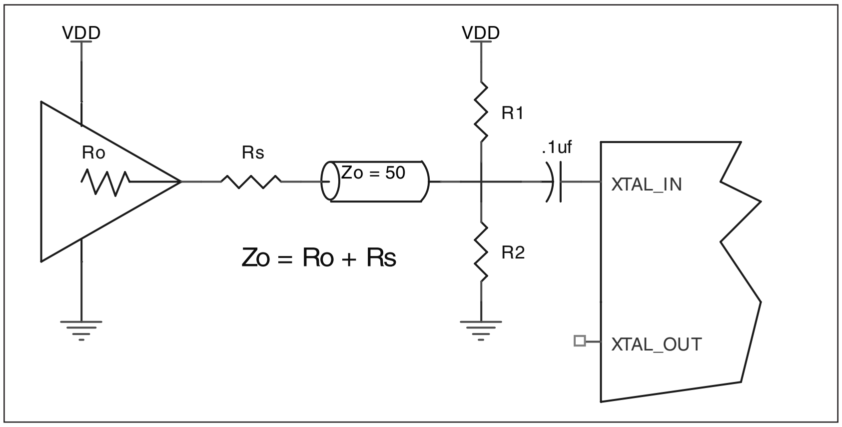


Figure 3. General Diagram for LVCMOS Driver to XTAL Input Interface

Recommendations for Unused Input and Output Pins

Inputs:

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

REF_CLK Input

For applications not requiring the use of the reference clock, it can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from the REF_CLK to ground.

LVCMOS Control Pins

All control pins have internal pull-ups or pull-downs; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Outputs:

LVPECL Outputs

All unused LVPECL outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

Termination for 3.3V LVPECL Output

The clock layout topology shown below is a typical termination for LVPECL outputs. The two different layouts mentioned are recommended only as guidelines.

FOUT and nFOUT are low impedance follower outputs that generate ECL/LVPECL compatible outputs. Therefore, terminating resistors (DC current path to ground) or current sources must be used for functionality. These outputs are designed to drive 50Ω transmission lines. Matched impedance techniques should be used to maximize operating frequency and minimize signal distortion. *Figures 4A and 4B* show two different layouts which are recommended only as guidelines. Other suitable clock layouts may exist and it would be recommended that the board designers simulate to guarantee compatibility across all printed circuit and clock component process variations.

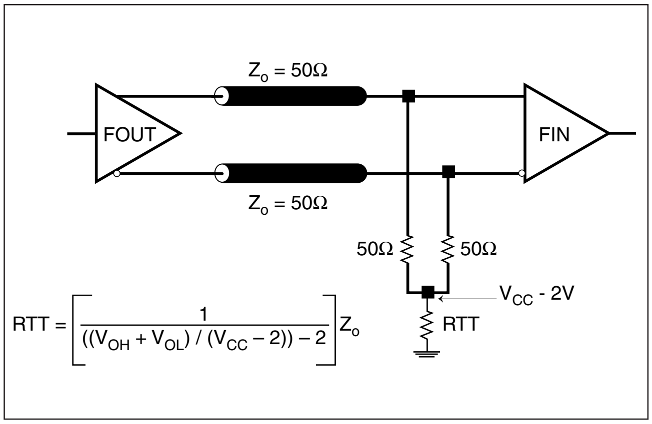


Figure 4A. LVPECL Output Termination

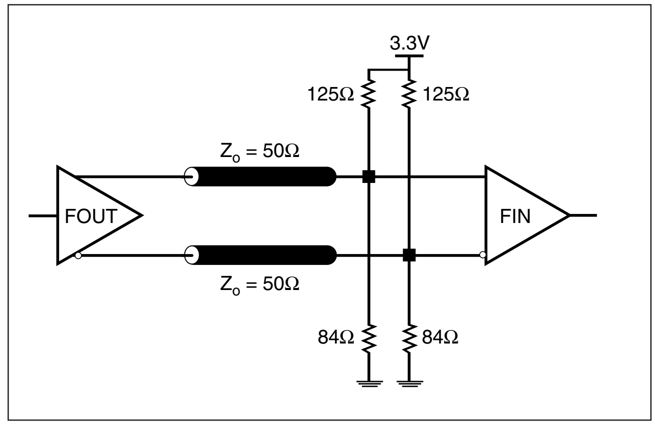


Figure 4B. LVPECL Output Termination

Schematic Example

Figure 5 shows an example of ICS843207B-350 application schematic. In this example, the device is operated at $V_{CC} = V_{CCO} = 3.3V$. The 18pF parallel resonant 14MHz crystal is used. The C1 = 27pF and C2 = 27pF are recommended for frequency accuracy. For different board layout, the C1 and C2 may be slightly adjusted for optimizing frequency accuracy. Two examples of LVPECL terminations are shown in this schematic. Additional termination approaches are shown in the LVPECL Termination Application Note.

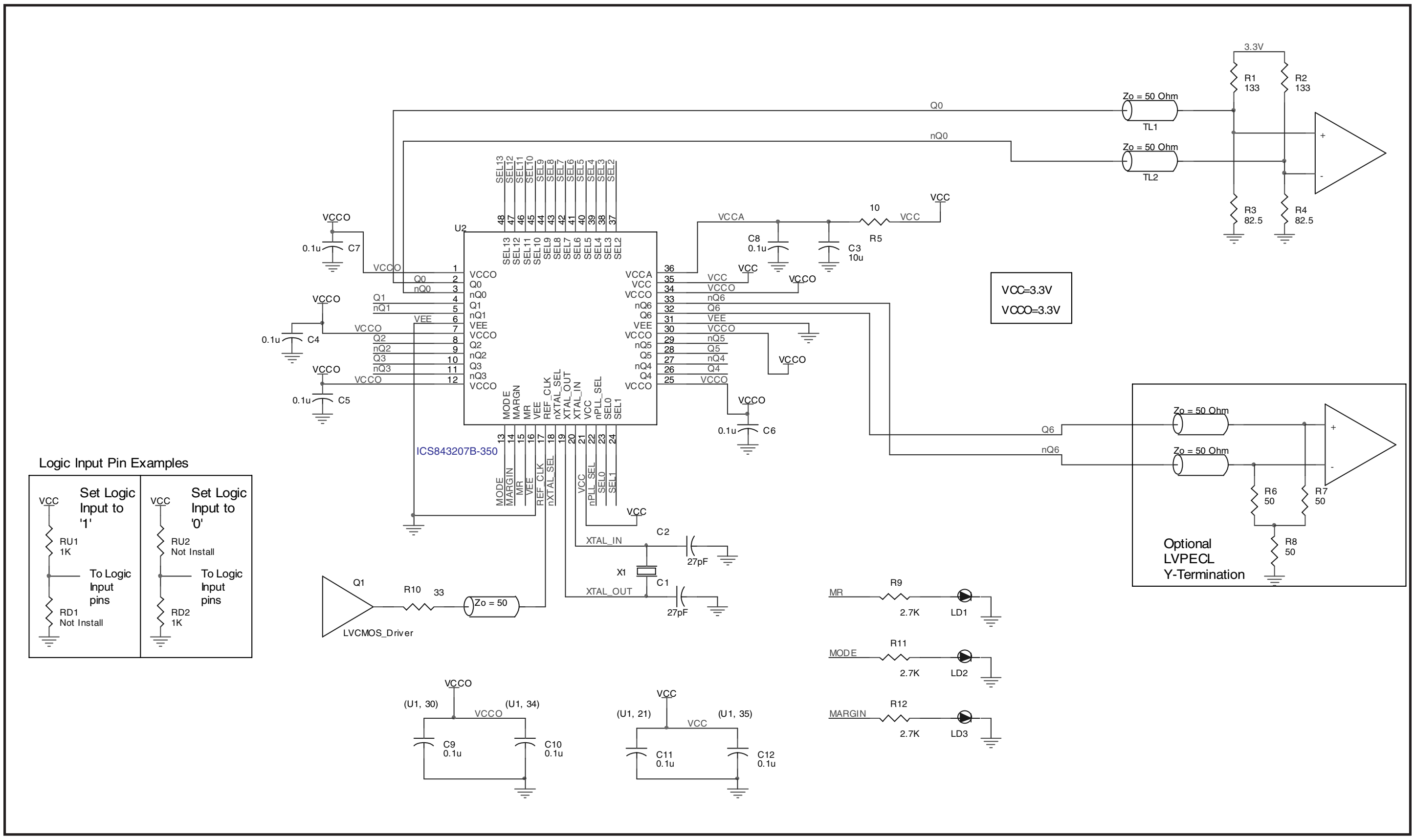


Figure 5. ICS843207B-350 Schematic Layout

Power Considerations

This section provides information on power dissipation and junction temperature for the ICS843207B-350. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the ICS843207B-350 is the sum of the core power plus the power dissipated in the load(s). The following is the power dissipation for V_{CC} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated in the load.

- Power $(core)_{MAX} = V_{CC\_MAX} * I_{EE\_MAX}$ = 3.465V * 210mA = **727.65mW**
- Power $(outputs)_{MAX}$ = **30mW/Loaded Output pair**
  If all outputs are loaded, the total power is 7 * 30mW = **210mW**

Total Power $_{\_MAX}$ (3.63V, with all outputs switching) = 727.65mW + 210mW = **937.65mW**

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad and directly affects the reliability of the device. The maximum recommended junction temperature for HiPerClockS™ devices is 125°C.

The equation for Tj is as follows: $Tj = \theta_{JA} * Pd\_total + T_A$

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming air flow at 1 meter per second and a multi-layer board, the appropriate value is 55.9°C/W per Table 8 below.

Therefore, Tj for an ambient temperature of 70°C with all outputs switching is:

70°C + 0.938W *55.9°C/W = 122.4°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow, and the type of board (single layer or multi-layer).

Table 8. Thermal Resistance θ_{JA} for 48-Pin LQFP, Forced Convection

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	65.7°C/W	55.9°C/W	52.4°C/W

3. Calculations and Equations.

The purpose of this section is to derive the power dissipated into the load.

LVPECL output driver circuit and termination are shown in *Figure 5.*

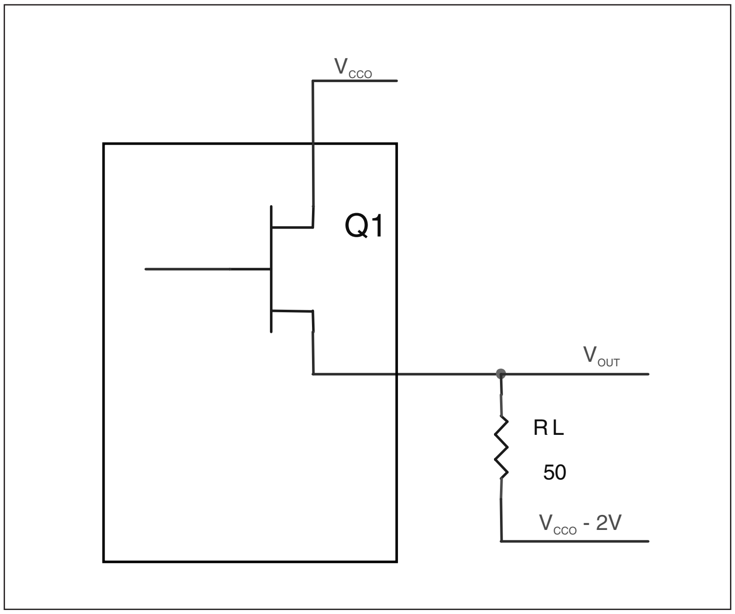


FIGURE 5. LVPECL DRIVER CIRCUIT AND TERMINATION

To calculate worst case power dissipation into the load, use the following equations which assume a 50Ω load, and a termination voltage of V_{CCO} - 2V.

- For logic high, $V_{OUT} = V_{OH\_MAX} = \mathbf{V_{CCO\_MAX} - 0.9V}$

  $(V_{CCO\_MAX} - V_{OH\_MAX}) = \mathbf{0.9V}$

- For logic low, $V_{OUT} = V_{OL\_MAX} = \mathbf{V_{CCO\_MAX} - 1.7V}$

  $(V_{CCO\_MAX} - V_{OL\_MAX}) = \mathbf{1.7V}$

Pd_H is power dissipation when the output drives high.
Pd_L is the power dissipation when the output drives low.

$Pd\_H = [(V_{OH\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OH\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OH\_MAX}) =$
$[(2V - 0.9V)/50\Omega] * 0.9V =$ **19.8mW**

$Pd\_L = [(V_{OL\_MAX} - (V_{CCO\_MAX} - 2V))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) = [(2V - (V_{CCO\_MAX} - V_{OL\_MAX}))/R_L] * (V_{CCO\_MAX} - V_{OL\_MAX}) =$
$[(2V - 1.7V)/50\Omega] * 1.7V =$ **10.2mW**

Total Power Dissipation per output pair = Pd_H + Pd_L = **30mW**

Reliability Information

Table 9. θ_{JA} vs. Air Flow Table for 48 Lead LQFP

θ_{JA} by Velocity (Meters per Second)			
	0	**1**	**2.5**
Multi-Layer PCB, JEDEC Standard Test Boards	65.7°C/W	55.9°C/W	52.4°C/W

Transistor Count

The transistor count for ICS843207B-350 is: 4380

Package Outline - Y Suffix for 48 Lead LQFP

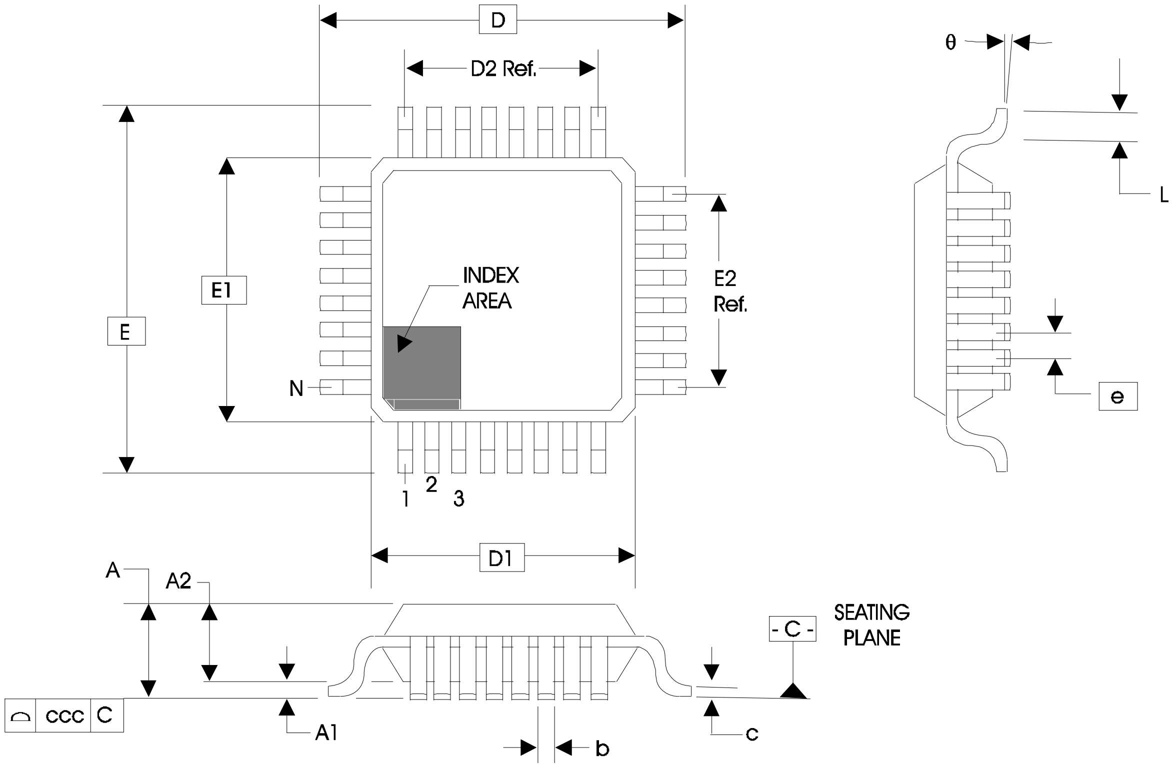


Table 10. Package Dimensions

JEDEC VARIATION ALL DIMENSIONS IN MILLIMETERS			
SYMBOL	**BBC**		
	MINIMUM	**NOMINAL**	**MAXIMUM**
N		48	
A	--	--	1.60
A1	0.05	--	0.15
A2	1.35	1.40	1.45
b	0.17	0.22	0.27
c	0.09	--	0.20
D		9.00 BASIC	
D1		7.00 BASIC	
D2		5.50 Ref.	
E		9.00 BASIC	
E1		7.00 BASIC	
E2		5.50 Ref.	
e		0.50 BASIC	
L	0.45	0.60	0.75
θ	0°	--	7°
ccc	--	--	0.08

Reference Document: JEDEC Publication 95, MS-026

TABLE 11. ORDERING INFORMATION

Part/Order Number	Marking	Package	Shipping Packaging	Temperature
843207BY-350	43207B350	48 Lead LQFP	tray	0°C to 70°C
843207BY-350T	43207B350	48 Lead LQFP	1000 tape & reel	0°C to 70°C
843207BY-350LF	3207B350L	48 Lead "Lead-Free" LQFP	tray	0°C to 70°C
843207BY-350LFT	3207B350L	48 Lead "Lead-Free" LQFP	1000 tape & reel	0°C to 70°C

NOTE: Parts that are ordered with an "LF" suffix to the part number are the Pb-Free configuration and are RoHS compliant.

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